High-proportion Reactive Power Compensation Control for Delta-connected High-voltage Transformerless Battery Energy Storage System via Optimal Zero-sequence Current Injection

Xiaoping Zhou, *Member*, *IEEE*, Yizhen Hu, Lerong Hong, Qianming Xu, *Member*, *IEEE*, Fenfen Zhu, Lingfeng Deng, Lei Zhang, Hanting Peng, Zhen Zhang, Le Li, and Ruotong Wang

***Abstract*—The structural configuration of delta-connected high-voltage transformerless battery energy storage system (D-HVT-BESS) inherently introduces second-order ripple currents (SORCs) into the battery cells. Under low power factor conditions, the SORCs exhibit frequent zero-crossing, which accelerates battery aging and compromises the accuracy of state monitoring. Therefore, a high-proportion reactive power compensation control method for D-HVT-BESS via optimal zero-sequence current injection is proposed. The key to the proposed method is to use zero-sequence current to adjust the reactive-to-active power ratio of each phase leg. This adjustment enhances the power factor per phase, thereby eliminating the zero-crossing of SORCs. Furthermore, an optimization model is formulated to minimize the system power loss induced by zero-sequence current. The optimization model achieves this by optimizing the amplitude and phase angle of zero-sequence current. Additionally, to mitigate the inter-phase state of charge (SOC) imbalance caused by the zero-sequence current, an inter-phase SOC balancing control strategy based on an absolute phase selector is developed, enabling real-time optimization of the absolute phase of zero-sequence current to achieve dynamic SOC equalization among phases. Finally, a 380 V/100 kW/50 kWh experimental prototype is constructed for validation. Experimental results verify the effectiveness and operational feasibility of the proposed method.**

***Index Terms*—Reactive power compensation control, battery energy storage system, battery cell, second-order ripple current (SORC), power loss, zero-sequence current, power factor, state of charge (SOC).**

I. Introduction

THE ongoing consumption of fossil fuels and the resulting environmental pollution have driven the development of renewable energy sources. Projections indicate that the penetration of renewable energy in power systems is expected to reach 86% by 2050 [1], [2]. However, renewable energy generation, especially from wind and solar power, is characterized by unpredictability and intermittency [3], posing risks to the safe and stable operation of the power grid [4]. In this context, battery energy storage systems (BESSs) with their flexible power regulation capabilities have become essential for enabling the high-proportion integration of renewable energy [5], [6].

Among various BESS configurations, the high-voltage transformerless BESS (HVT-BESS) utilizes a cascaded H-bridge converter for power conversion. This architecture offers significant advantages over traditional low-voltage topologies, including modular design, high efficiency, large single-unit capacity, and rapid dynamic response [7]. Furthermore, the batteries are distributed across the submodules of HVT-BESS, with individual battery clusters serving as the basic units. This distributed configuration effectively mitigates battery circulating current, thereby reducing cycle loss and enhancing the overall safety of the system [8], [9]. Consequently, HVT-BESS has been widely deployed in applications such as renewable energy integration, and grid support functions such as peak shaving and valley filling. Moreover, by fully exploiting its inherent reactive power compensation capabilities, the HVT-BESS can potentially replace traditional compensation devices. Therefore, the overall investment cost of the power grid can be further reduced.

Additionally, existing research establishes the superior performance of the delta-connected HVT-BESS (D-HVT-BESS) over the star-connected HVT-BESS (Y-HVT-BESS) under imbalanced conditions. Specifically, the D-HVT-BESS dem-

Manuscript received: June 5, 2025; revised: October 6, 2025; accepted: January 5, 2026. Date of CrossCheck: January 5, 2026. Date of online publication: February 2, 2026.

This work was supported in part by the National Key Research and Development Program of China (No. 2024YFB2409300), in part by the National Natural Science Foundation of China (No. 52377182), in part by the science and technology innovation Program of Hunan Province (No. 2024RC3113), and in part by the Natural Science Excellent Youth Science Foundation Project of Hunan Province (No. 2023JJ20012).

X. Zhou, Y. Hu, L. Hong (corresponding author), Q. Xu, L. Zhang, H. Peng, Z. Zhang, L. Li, and R. Wang are with the State Key Laboratory of High-efficiency and High-quality Conversion for Electric Power, College of Electrical and Information Engineering, Hunan University, Changsha 410082, China (e-mail: zxp2011@hnu. edu. cn; huyizhen168@126. com; hlr0908@163. com; xqm@hnu. edu. cn; zl1192157465@163. com; penghanting_hnu@163. com; allenzhang@hnu. edu.cn; 2502608070@qq.com; wrtmlx@126.com).

F. Zhu is with the State Grid Wuhu Electric Power Supply Company, Wuhu 241000, China (e-mail: zhuff2000@163.com).

L. Deng is with the School of Electrical Engineering, China University of Mining and Technology, Xuzhou 221116, China (e-mail: 18361228606@163. com).

DOI: 10.35833/MPCE.2025.000516

onstrates enhanced capability to adapt to inter-phase power imbalance [10] and provides more effective compensation [11]. Therefore, the D-HVT-BESS is more attractive for practical applications, particularly in scenarios involving significant grid or load imbalance.

However, the absence of a common bus in the D-HVT-BESS leads to the generation of a second-order ripple current (SORC) flowing through the batteries. A critical problem arises under low power factor conditions, where the SORC causes repeated zero-crossing events in the battery current waveforms. These events substantially increase the accumulated charge throughput of the batteries, which accelerates battery aging and reduces the accuracy of battery state monitoring [12], [13]. In response to these challenges, four main categories of methods have been proposed in recent studies: active power decoupling method [14] - [17], virtual impedance method using DC-DC converter [18], [19], passive filtering method [20], [21], and harmonic current injection method [22]-[24].

In the active power decoupling method, a DC-DC converter is typically connected in parallel with the DC bus of each submodule of the HVT-BESS. This configuration diverts fluctuating power to the converter, thereby reducing the ripple power transferred to the battery. For example, a buck-boost decoupling circuit is introduced in [15], while a composite control integrating a repetitive controller with a proportional-integral (PI) controller is further presented in [16] to achieve precise capacitor voltage regulation. Additionally, a buck-reuse totempole power decoupling circuit is proposed in [17] to improve the control accuracy and reduce cost.

Similarly, within the domain of virtual impedance method, based on the voltage and current double closed-loop control of DC-DC converter, an AC output current feedforward control based on Notch filter is introduced in [18]. In contrast, [19] proposes a composite virtual impedance control, which involves inserting a virtual impedance in the series branch of the DC-DC converter to suppress the SORC, while an additional virtual impedance is applied in the parallel branch across the DC bus to improve the dynamic response.

Despite their effectiveness, both types of methods require integrating a DC-DC converter into each submodule of the HVT-BESS. This requirement significantly increases the system cost and control complexity while reducing the power density, which limits their feasibility in practical engineering applications.

In contrast, the passive filtering method requires only an inductor-capacitor (LC) filter connected in series between the battery and the DC terminal of the submodule to effectively filter harmonic components in the battery current. Increasing the filter capacitance is the most direct way to enhance the suppression capability of the SORC [20]. However, this inevitably increases the system volume and cost. Therefore, the LC parameters should be co-designed according to the voltage and current ripple requirements at the battery terminals [21].

Based on the design, the harmonic current injection method introduces targeted harmonic components into the Y-HVT-BESS to actively compensate for power fluctuations, thereby suppressing SORC [22]. In [23], a D-HVT-BESS is considered, in which LC resonant filters are connected in parallel to the AC side of each phase converter and the DC side of each submodule, respectively. Concurrently, the 3rd, 5th, and 7th harmonic currents are injected to reduce the amplitudes of power fluctuations.

Existing SORC suppression methods mainly aim to reduce the amplitude of the SORC. Although decreasing the ripple amplitude can reduce the probability of double-frequency charging and discharging, these methods face significant practical limitations. They are often costly, and under low power factor conditions, the average battery current may be lower than the SORC amplitude. Consequently, it still results in the zero-crossing of battery current, which poses a significant threat to the battery lifespan.

Therefore, to overcome the limitations mentioned above, a high-proportion reactive power compensation control (HPRPCC) method for D-HVT-BESS via optimal zero-sequence current injection is proposed, which is based on minimizing the system power loss. The proposed method aims to mitigate the zero-crossing of SORC under low power factor conditions. In addition, to mitigate the inter-phase state-of-charge (SOC) imbalance induced by zero-sequence current, an inter-phase SOC balancing control strategy based on an absolute phase selector is proposed. Under low power factor conditions, zero-crossing points of the battery current can be completely avoided using the proposed method, while maintaining the minimal incremental system power loss. Moreover, it incurs no additional hardware cost.

The remainder of this paper is organized as follows. In Section II, the configuration of the D-HVT-BESS is introduced. Then, the operating characteristics under low power factor conditions are analyzed. In Section III, the proposed method via optimal zero-sequence current injection is presented, where the zero-sequence current is optimized to minimize the system power loss. Furthermore, the inter-phase SOC balancing control strategy is proposed in Section IV based on an absolute phase selector. Section V presents the experimental verification of the proposed method. Finally, Section VI concludes this paper.

II. Configuration of D-HVT-BESS and Operating Characteristics Under Low Power Factor Conditions

A. Configuration of D-HVT-BESS

Figure 1 shows the main circuit diagram of the D-HVT-BESS, and a cascaded H-bridge power conversion system is adopted. Furthermore, each phase leg comprises N low-voltage submodules (denoted by SM_{x1}-SM_{xN} in Fig. 1), while each submodule integrates a single-phase H-bridge converter, an LC low-pass filter, and a battery cluster. Three phase legs are connected in a delta configuration. Given the large number of cascaded submodules, an output AC voltage with multiple levels can be achieved. Consequently, the D-HVT-BESS can be directly interfaced with the high-voltage power grid via a simple filter inductor without a line frequency transformer.

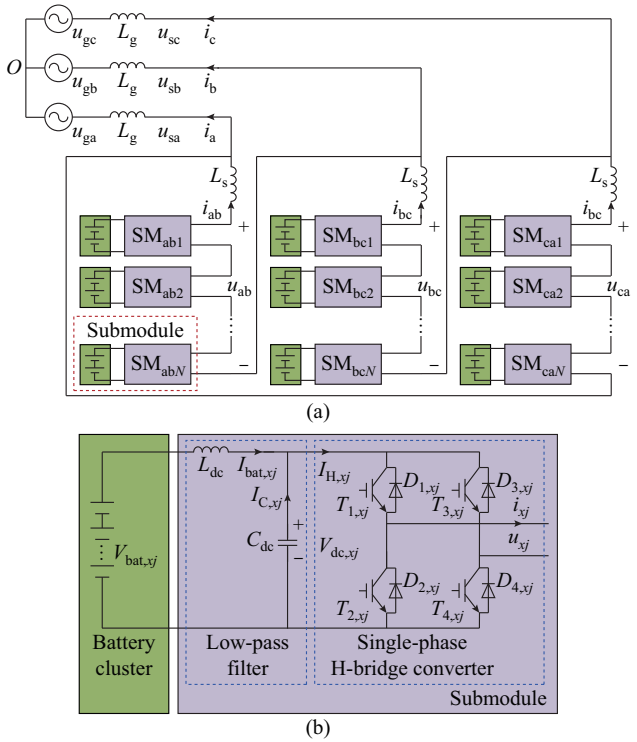

Fig. 1. Main circuit diagram of D-HVT-BESS. (a) D-HVT-BESS. (b) Submodule.

In Fig. 1, subscript $y \in \{a, b, c\}$ represents the phase on the grid side; u_{gy} and u_{sy} are the grid voltage and the voltage at the point of common coupling (PCC), respectively; i_y is the grid current flowing through the grid-side inductance L_g; subscript $x \in \{ab, bc, ca\}$ represents the line-to-line phase on the D-HVT-BESS side; u_x and i_x are the phase voltage and current of the D-HVT-BESS, respectively; $j \in \{1, 2, ..., N\}$ is the index of submodules; $I_{H,xj}$, $I_{bat,xj}$, and $I_{C,xj}$ are the DC-side current of the H-bridge converter, the battery cluster current, and the capacitor current, respectively; $V_{bat,xj}$ is the battery cluster voltage; L_{dc} and C_{dc} are the inductance and capacitance of the DC-side filter, respectively; u_{xj} and i_{xj} are the AC voltage and current of each submodule, respectively, and $i_{xj} = i_x$; L_s is the AC-side filter inductor of the D-HVT-BESS; and $D_{1,xj}$-$D_{4,xj}$ and $T_{1,xj}$-$T_{4,xj}$ are the diodes and insulated gate bipolar transistors (IGBTs), respectively.

B. Operating Characteristics Under Low Power Factor Conditions

To analyze the generation mechanism of the SORC in battery cluster during four-quadrant operation of the D-HVT-BESS, a single submodule in the ab-phase, as shown in Fig. 1(b), is selected for detailed study. The phase angle of the AC voltage generated by the D-HVT-BESS is considered to be approximately equal to that of the grid line voltage, under the assumption that the voltage drop and reactive power consumption across the filter inductor are negligible. Consequently, the AC voltage and current of the submodule can be expressed as:

$$\begin{cases} u_{abj} = U_{sm} \sin(\omega t)/N \\ i_{abj} = I_m \sin(\omega t - \varphi) \end{cases} \tag{1}$$

where u_{abj} and i_{abj} are the AC voltage and current of the j^{th} submodule in the ab-phase, respectively; U_{sm} and I_m are the voltage amplitudes of the PCC line u_{sab} and the submodule current i_{abj}, respectively; ω is the angular frequency of the grid; and φ is the phase angle by which i_{abj} lags u_{abj}.

Based on (1), the instantaneous power of the submodule can be derived as:

$$p = U_{sm} I_m (\cos(\varphi) - \cos(2\omega t - \varphi))/(2N) \tag{2}$$

To simplify the analysis, the DC-side voltage of the submodule is assumed to remain constant at V_{dc}, and all internal losses are neglected. According to the energy conservation principle, the DC-side current of the H-bridge converter $I_{H,abj}$ is defined as:

$$\begin{aligned} I_{H,abj} &= U_{sm} I_m (\cos(\varphi) - \cos(2\omega t - \varphi))/(2NV_{dc}) = \\ &MI_m \cos(\varphi)/2 - MI_m \cos(2\omega t - \varphi)/2 = I_{H(0),abj} + I_{H(2),abj} \end{aligned} \tag{3}$$

where M is the modulation index defined as $M = U_{sm}/(NV_{dc})$, ranging from 0 to 1; and $I_{H(0),abj}$ and $I_{H(2),abj}$ are the DC component and the SORC component of $I_{H,abj}$, respectively.

Based on (3), the H-bridge converter can be equivalently modeled as two parallel controlled current sources, i. e., $I_{H(0),abj}$ and $I_{H(2),abj}$. Therefore, the circuit in Fig. 1(b) can be further simplified to the equivalent circuit shown in Fig. 2, where R_b and V_b are the internal resistance of the battery and the ideal voltage source, respectively. According to the superposition theorem, the resulting battery current $I_{bat,abj}$ is obtained as:

$$\begin{aligned} I_{bat,abj} &= MI_m \cos(\varphi)/2 - \frac{MI_m \cos(2\omega t - \theta)}{2\sqrt{(1 - 4\omega^2 L_{dc} C_{dc})^2 + (2\omega R_b C_{dc})^2}} = \\ &I_{bat(0),abj} + I_{bat(2),abj} \end{aligned} \tag{4}$$

where $I_{bat(0),abj}$ and $I_{bat(2),abj}$ are the DC component and the SORC component of the battery current, respectively; and $\theta = \varphi + \arctan(2\omega R_b C_{dc}/(1 - 4\omega^2 L_{dc} C_{dc}))$.

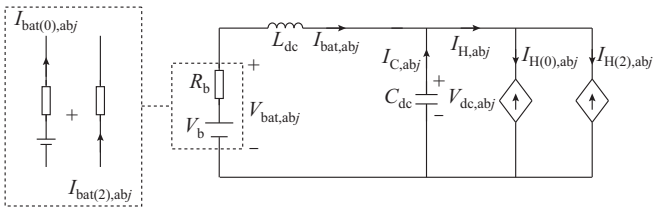

Fig. 2. Equivalent circuit of submodule.

As indicated by (3) and (4), the battery current retains an SORC even after LC low-pass filtering, although its amplitude is reduced. Furthermore, (4) indicates that when the reactive power component of the system is relatively large, i.e., the power factor $|\cos(\varphi)|$ satisfies (5), the DC current of battery $I_{bat(0),abj}$ is smaller than the amplitude of $I_{bat(2),abj}$.

$$|\cos(\varphi)| < \frac{1}{\sqrt{(1 - 4\omega^2 L_{dc} C_{dc})^2 + (2\omega R_b C_{dc})^2}} = \gamma \tag{5}$$

where γ is the critical power factor.

Consequently, the battery current undergoes zero-crossing at a frequency of 2ω. This may significantly reduce the battery lifespan, impair the accuracy of SOC estimation, and limit the four-quadrant operation capability of system.

As shown in Fig. 3, the battery currents of three conditions are synthesized from their DC and SORC components under three distinct conditions. As depicted, the current $I_{\text{bat},abj1}$ is the sum of the DC component $I_{\text{bat}(0),abj1}$ and the SORC component $I_{\text{bat}(2),abj}$. Similarly, $I_{\text{bat},abj2}$ and $I_{\text{bat},abj3}$ are formed by combining their respective DC components ($I_{\text{bat}(0),abj2}$ and $I_{\text{bat}(0),abj3}$) with the same SORC components. ① Condition 1 ($|\cos(\varphi)|>\gamma$): the DC component of the battery current exceeds the SORC amplitude, and in this case, the resultant current $I_{\text{bat},abj1}$ exhibits no zero-crossing points. ② Condition 2 ($|\cos(\varphi)|=\gamma$): the DC component is equal to the SORC amplitude, and the battery current $I_{\text{bat},abj2}$ reaches the critical zero-crossing state. ③ Condition 3 ($|\cos(\varphi)|<\gamma$): the DC component is smaller than the SORC amplitude, and therefore, the battery current $I_{\text{bat},abj3}$ exhibits zero-crossing points.

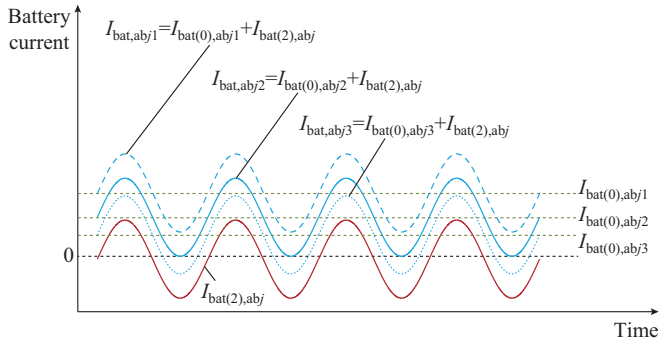

Fig. 3. Synthesis diagram of battery current.

According to (5), the critical value K for zero-crossing in the SORC can be defined as:

$$|Q_{\text{ref}}/P_{\text{ref}}|=\sqrt{(1-4\omega^2L_{\text{dc}}C_{\text{dc}})^2+(2R_{\text{b}}\omega C_{\text{dc}})^2-1}=K \quad (6)$$

where P_{ref} and Q_{ref} are the single-phase active and reactive power commands, respectively. According to (6) and the BESS capacity constraint $P_{\text{ref}}^2+Q_{\text{ref}}^2\le S_{\text{N}}$, where S_{N} is the single-phase rated apparent power, the operating range of the BESS in four quadrants is determined, as shown in Fig. 4.

In Fig. 4(a), the purple area ($|Q_{\text{ref}}/P_{\text{ref}}|\le K$) is the normal operating area, and the light blue area ($|Q_{\text{ref}}/P_{\text{ref}}|>K$) is the operating area of HPRPCC. Figure 4(b) illustrates the phasor diagram corresponding to the operation in four quadrants, where l_{mx} represents the phasor-domain boundaries between the normal operating area and the operating area of HPRPCC in quadrant m ($m\in${I, II, III, IV}). The three line-to-line phases ab, bc, and ca are indicated in red, yellow, and blue colors, respectively.

III. Proposed Method via Optimal Zero-sequence Current Injection

A. Principle of Proposed Method via Optimal Zero-sequence Current Injection

Based on the analysis in Section II, an HPRPCC method via optimal zero-sequence current injection is proposed. The following analysis focuses on a case where the initial operating point lies in quadrant I.

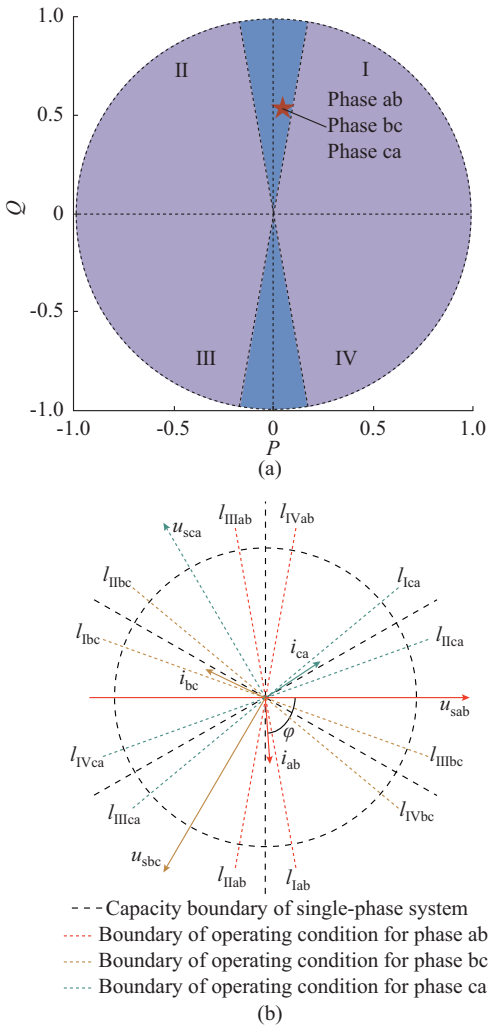

Fig. 4. Power and phasor diagrams in four quadrants. (a) Power diagram. (b) Phasor diagram.

Assume that the PCC voltage u_{sx}, the BESS phase current i_x, and the zero-sequence current i_0 are given as:

$$\begin{cases} u_{sx}=U_{\text{sm}}\sin(\omega t-2n\pi/3) \\ i_x=I_{\text{m}}\sin(\omega t-\varphi-2n\pi/3) \\ i_0=I_0\sin(\omega t-\theta_0) \end{cases} \quad (7a)$$

$$n=\begin{cases} 0 & x=\text{ab} \\ 1 & x=\text{bc} \\ -1 & x=\text{ca} \end{cases} \quad (7b)$$

where I_0 and θ_0 are the amplitude and phase of the zero-sequence current i_0, respectively.

The active and reactive power generated by i_0 in three phases can be expressed as:

$$\begin{cases} P_{0sx}=U_{\text{sm}}I_0\cos(\theta_0-2n\pi/3)/2 \\ Q_{0sx}=U_{\text{sm}}I_0\sin(\theta_0-2n\pi/3)/2 \end{cases} \quad (8)$$

Obviously, the amplitudes of the three-phase active power generated by the zero-sequence current are equal, and so are amplitudes of the three-phase reactive power. As shown in Fig. 5(a), the zero-sequence complex power phasors $S_{0\text{ab}}$, $S_{0\text{bc}}$, and $S_{0\text{ca}}$ exhibit a successive phase lag of $2\pi/3$ between each con-

secutive pair. Thus, the sum of the three complex power phasors is zero. This means the zero-sequence current does not change the net power delivered to the grid, but only redistributes the power among the three phases.

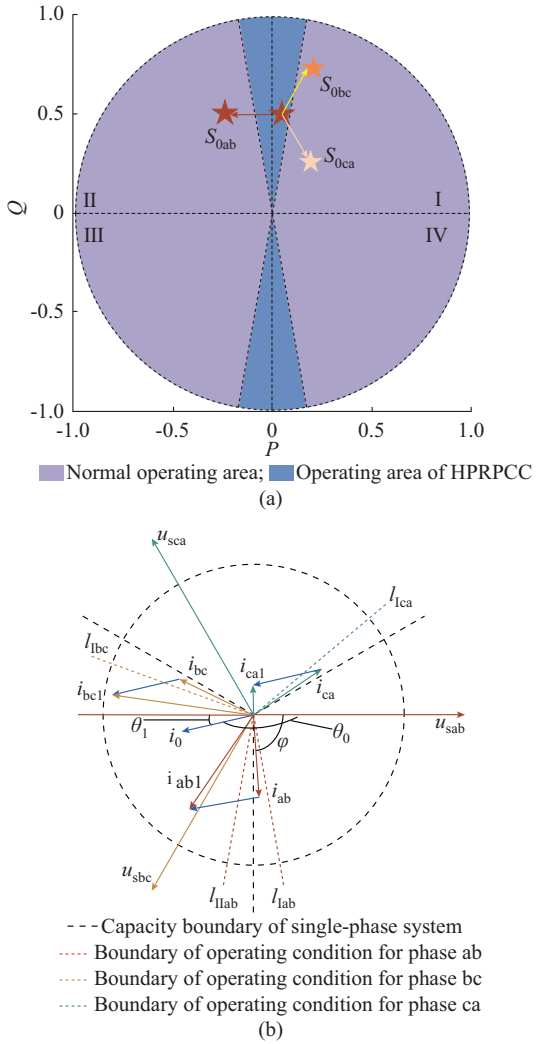

Fig. 5. Principle of proposed method based on zero-sequence current injection. (a) Power diagram. (b) Phasor diagram.

In Fig. 5, the initial operating points of the three-phase legs are in the operating area of HPRPCC in quadrant I, with the ab-phase selected as the reference phase. θ_1 is defined as the relative phase angle of the zero-sequence current, which represents the angle between i_0 and the reverse extension line of u_{sab}. When i_0 leads this reverse extended line, θ_1 is a positive value ($\theta_1 > 0$); otherwise, θ_1 is a negative value ($\theta_1 < 0$). Moreover, $\theta_0 = \pi - \theta_1$.

An example where θ_1 of the zero-sequence current is set to be 0 is presented in Fig. 5(a). In this example, the operating point of the ab-phase leg is shifted to the normal operation area of quadrant II, while the operating points of both the bc-phase and ca-phase legs are shifted to the normal operation area of quadrant I. The injection of the zero-sequence current i_0 induces the following adjustments in the per-phase power flows:

1) For the ab-phase leg, the absorbed active power increases.

2) For the bc-phase leg, both the delivered active power and reactive power increase.

3) For the ca-phase leg, the delivered active power increases, while the delivered reactive power decreases.

As shown in Fig. 5(b), when $\theta_1 > \pi/6$, the phase angle by which the phasor of i_0 leads the phasor of u_{sca} exceeds $\pi/2$. This condition leads to a reduction in both the active and reactive power delivered by the ca-phase leg. Consequently, it becomes ineffective in adjusting the operating point of the ca-phase leg into the normal operating area in quadrant I. Conversely, when $\theta_1 < -\pi/6$, the operating point of bc-phase leg cannot be effectively adjusted into the normal operation area in quadrant I. Therefore, the range of θ_1 is $[-\pi/6, \pi/6]$, and the corresponding range of θ_0 is $[5\pi/6, 7\pi/6]$.

In summary, the analysis begins with the initial operating points of three-phase legs situated within the operating area of HPRPCC in quadrant I, with the ab-phase designated as the reference phase. Upon the injection of a zero-sequence current, the operating point of ab-phase leg is shifted into the normal operating area in quadrant II. In contrast, the operating points of the bc- and ca-phase legs can only be adjusted to the normal operating area of quadrant I. Moreover, the similar conclusion can be extended to cases where the initial operating point lies in the operating area in quadrant II, III or IV. The corresponding results are summarized in Table I.

TABLE I
RESULTS OF STATE TRANSITION OF OPERATION

Reference phase	Initial quadrant of three legs	New quadrant of ab-phase leg	New quadrant of bc-phase leg	New quadrant of ca-phase leg
ab-phase	I	II	I	I
	II	I	II	II
	III	IV	III	III
	IV	III	IV	IV
bc-phase	I	I	II	I
	II	II	I	II
	III	III	IV	III
	IV	IV	III	IV
ca-phase	I	I	I	II
	II	II	II	I
	III	III	III	IV
	IV	IV	IV	III

B. Calculation of System Power Loss

1) Conduction Loss of Power Devices

Figure 6 depicts the switching modes of the submodule. The fundamental frequency cycle of operation of the submodule is divided into four operating stages based on the phase relationship between its AC voltage and current. Within each stage, the system follows a cyclic mode transition sequence: ①→②→③→②→①. The mode transition sequences ①, ②, and ③ are expressed by green, red, and blue arrows, respectively; and u and i are the voltage and current of the submodule, respectively.

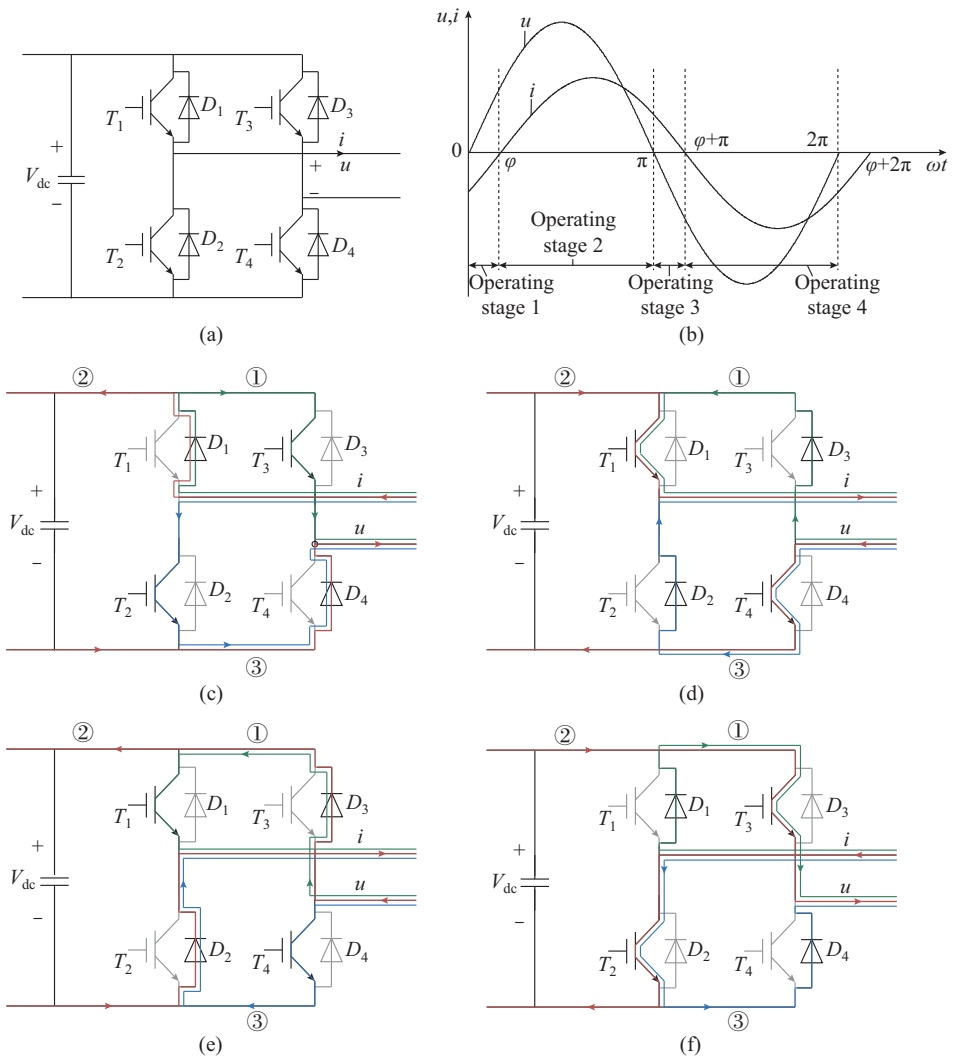

Fig. 6. Switching modes of submodule. (a) Topology of submodule. (b) Voltage and current waveforms of submodule. (c) Switching mode in operating stage 1. (d) Switching mode in operating stage 2. (e) Switching mode in operating stage 3. (f) Switching mode in operating stage 4.

To simplify the symbol, the subscripts denoting phase and module numbers are omitted in the following derivations. Based on the voltage and current expressions given in (1) and the operating modes shown in Fig. 6, the modulation signals for each power semiconductor device within a submodule of the ab-phase leg can be formulated as:

$$\begin{cases} m_{\mathrm{T1}} = m_{\mathrm{D1}} = (1 + M\sin(\omega t))/2 \\ m_{\mathrm{T2}} = m_{\mathrm{D2}} = 1 - m_{\mathrm{T1}} = (1 - M\sin(\omega t))/2 \\ m_{\mathrm{T3}} = m_{\mathrm{D3}} = (1 - M\sin(\omega t))/2 \\ m_{\mathrm{T4}} = m_{\mathrm{D4}} = 1 - m_{\mathrm{T3}} = (1 + M\sin(\omega t))/2 \end{cases} \tag{9}$$

where $m_{\mathrm{T}k}$ and $m_{\mathrm{D}k}$ are the modulation signals of the IGBTs and diodes, respectively, with $k \in \{1, 2, 3, 4\}$.

According to the conduction loss calculation method described in [25] and [26], the conduction loss of the IGBTs and diodes are calculated as:

$$\begin{cases} P_{\mathrm{conT}k} = V_{\mathrm{ce0,IGBT}} I_{\mathrm{aveT}k} + R_{\mathrm{0,IGBT}} I_{\mathrm{rmsT}k}^2 \\ P_{\mathrm{conD}k} = V_{\mathrm{F0,Diode}} I_{\mathrm{aveD}k} + R_{\mathrm{0,Diode}} I_{\mathrm{rmsD}k}^2 \end{cases} \tag{10}$$

where $V_{\mathrm{ce0,IGBT}}$ and $R_{\mathrm{0,IGBT}}$ are the on-state voltage drop and equivalent on-state resistance of the IGBT, respectively; $I_{\mathrm{aveT}k}$ and $I_{\mathrm{rmsT}k}$ are the average and root-mean-square (RMS) currents through IGBT, respectively; $V_{\mathrm{F0,Diode}}$ and $R_{\mathrm{0,Diode}}$ are the forward voltage drop and equivalent on-state resistance of the diode, respectively; and $I_{\mathrm{aveD}k}$ and $I_{\mathrm{rmsD}k}$ are the average and RMS currents through the diode, respectively. Note that $V_{\mathrm{ce0,IGBT}}$, $R_{\mathrm{0,IGBT}}$, $V_{\mathrm{F0,Diode}}$, and $R_{\mathrm{0,Diode}}$ are the parameters obtained from the device datasheets.

The average currents $I_{\mathrm{aveT}k}$ and $I_{\mathrm{aveD}k}$ can be given as [25], [27]:

$$\begin{cases} I_{\mathrm{aveT1}} = \dfrac{1}{2\pi}\displaystyle\int_{\varphi}^{\varphi+\pi} m_{\mathrm{T1}} i \mathrm{d}\omega t \\ I_{\mathrm{aveT2}} = -\dfrac{1}{2\pi}\left(\displaystyle\int_{0}^{\varphi} m_{\mathrm{T2}} i \mathrm{d}\omega t + \int_{\varphi+\pi}^{2\pi} m_{\mathrm{T2}} i \mathrm{d}\omega t\right) \\ I_{\mathrm{aveT3}} = I_{\mathrm{aveT2}} \\ I_{\mathrm{aveT4}} = I_{\mathrm{aveT1}} \end{cases} \tag{11}$$

$$\begin{cases} I_{\text{aveD1}} = -\dfrac{1}{2\pi}\left(\displaystyle\int_0^{\varphi} m_{\text{D1}} i \,\mathrm{d}\omega t + \int_{\varphi+\pi}^{2\pi} m_{\text{D1}} i \,\mathrm{d}\omega t\right) \\ I_{\text{aveD2}} = \dfrac{1}{2\pi}\displaystyle\int_{\varphi}^{\varphi+\pi} m_{\text{D2}} i \,\mathrm{d}\omega t \\ I_{\text{aveD3}} = I_{\text{aveD2}} \\ I_{\text{aveD4}} = I_{\text{aveD1}} \end{cases} \tag{12}$$

The squared values of RMS currents $I^2_{\text{rmsT}k}$ and $I^2_{\text{rmsD}k}$ are given as:

$$\begin{cases} I^2_{\text{rmsT1}} = \dfrac{1}{2\pi}\displaystyle\int_{\varphi}^{\varphi+\pi} m_{\text{T1}} i^2 \,\mathrm{d}\omega t \\ I^2_{\text{rmsT2}} = \dfrac{1}{2\pi}\left(\displaystyle\int_0^{\varphi} m_{\text{T2}} i^2 \,\mathrm{d}\omega t + \int_{\varphi+\pi}^{2\pi} m_{\text{T2}} i^2 \,\mathrm{d}\omega t\right) \\ I^2_{\text{rmsT3}} = I^2_{\text{rmsT2}} \\ I^2_{\text{rmsT4}} = I^2_{\text{rmsT1}} \end{cases} \tag{13}$$

$$\begin{cases} I^2_{\text{rmsD1}} = \dfrac{1}{2\pi}\left(\displaystyle\int_0^{\varphi} m_{\text{D1}} i^2 \,\mathrm{d}\omega t + \int_{\varphi+\pi}^{2\pi} m_{\text{D1}} i^2 \,\mathrm{d}\omega t\right) \\ I^2_{\text{rmsD2}} = \dfrac{1}{2\pi}\displaystyle\int_{\varphi}^{\varphi+\pi} m_{\text{D2}} i^2 \,\mathrm{d}\omega t \\ I^2_{\text{rmsD3}} = I^2_{\text{rmsD2}} \\ I^2_{\text{rmsD4}} = I^2_{\text{rmsD1}} \end{cases} \tag{14}$$

Based on (11)-(14), the following relationships can be observed: $I_{\text{aveT1}} = I_{\text{aveT2}} = I_{\text{aveT3}} = I_{\text{aveT4}}$, $I_{\text{aveD1}} = I_{\text{aveD2}} = I_{\text{aveD3}} = I_{\text{aveD4}}$, $I^2_{\text{rmsT1}} = I^2_{\text{rmsT2}} = I^2_{\text{rmsT3}} = I^2_{\text{rmsT4}}$, and $I^2_{\text{rmsD1}} = I^2_{\text{rmsD2}} = I^2_{\text{rmsD3}} = I^2_{\text{rmsD4}}$. Therefore, the four IGBTs in the same submodule experience identical conduction loss, as do the four diodes. Consequently, the total conduction loss of a single submodule P_{con} can be expressed as:

$$P_{\text{con}} = 4(P_{\text{conT1}} + P_{\text{conD1}}) \tag{15}$$

2) Switching Loss of Power Devices

Figure 6 shows that in each switching cycle, there are always two turn-on events and two turn-off events of the IGBTs, as well as two reverse recovery events of the diodes [26]. Consequently, the total switching loss of a single submodule P_{sw} can be expressed as [25]:

$$\begin{cases} P_{\text{sw}} = f_0 \displaystyle\int_0^{1/f_0} 2 f_{\text{sw}} E_{\text{sw}}(i(t))(V_{\text{dc}}/V_{\text{ref}})^{K_v} \mathrm{d}t \\ E_{\text{sw}}(i(t)) = E_{\text{on}}(i) + E_{\text{off}}(i) + E_{\text{rec}}(i) \end{cases} \tag{16}$$

where f_0 and f_{sw} are the fundamental frequency and switching frequency, respectively; V_{dc} and V_{ref} are the DC voltage of the submodule and the reference blocking voltage specified in the datasheet, respectively; K_v is the voltage coefficient; $E_{\text{on}}(i)$ and $E_{\text{off}}(i)$ are the values of turn-on and turn-off energy of the IGBT, respectively; $E_{\text{rec}}(i)$ is the reverse recovery energy of the diode; $E_{\text{sw}}(i)$ is the total switching energy of a single submodule; and V_{ref}, $E_{\text{on}}(i)$, $E_{\text{off}}(i)$, and $E_{\text{rec}}(i)$ are the parameters obtained from the device datasheets.

3) Power Loss of Capacitors

The power loss of capacitors P_{cap} is related to the RMS capacitor current $I_{\text{cap,rms}}$ and the capacitor series resistance ESR_{cap}, which can be expressed by [28]:

$$P_{\text{cap}} = I^2_{\text{cap,rms}}(2\omega) \cdot ESR_{\text{cap}}(2\omega) \tag{17}$$

$$I^2_{\text{cap,rms}}(2\omega) = \frac{(MI_{\text{m}})^2[(2\omega R_{\text{b}} C_{\text{dc}})^2 + (4\omega^2 L_{\text{dc}} C_{\text{dc}})^2]}{8[(1-4\omega^2 L_{\text{dc}} C_{\text{dc}})^2 + (2\omega R_{\text{b}} C_{\text{dc}})^2]} \tag{18}$$

4) Power Loss of Inductors

The total power loss in the AC filter inductor P_{Ls} is typically composed of the winding loss P_{w} and the core loss P_{core}, expressed by $P_{\text{Ls}} = P_{\text{w}} + P_{\text{core}}$.

P_{w} is calculated from the equivalent series resistance of inductor R_{Ls} and the RMS value of inductor current $I_{\text{Ls,rms}}$ [26]:

$$P_{\text{w}} = I^2_{\text{Ls,rms}} R_{\text{Ls}} \tag{19}$$

P_{core} can be calculated using the Steinmetz equation:

$$P_{\text{core}} = C_{\text{m}} f_0^{\alpha} B^{\beta} V_{\text{e}} \tag{20}$$

where B is the amplitude of the magnetic flux density; V_{e} is the core volume; and C_{m}, α, and β are the coefficients specified in the core datasheet.

The power loss in the battery filter inductor P_{Ldc} comprises the loss due to the DC current and the loss induced by the SORC. And P_{Ldc} is also evaluated using (19) and (20), where the inductor current is derived from (4).

In summary, the total system power loss P_{loss} can be expressed as:

$$P_{\text{loss}} = 3N(P_{\text{con}} + P_{\text{sw}} + P_{\text{cap}} + P_{\text{Ldc}}) + 3P_{\text{Ls}} \tag{21}$$

Although the zero-sequence current affects the amplitudes and phases of the three-phase currents, the modulation index remains nearly constant [23]. As a result, the amplitude and phase of the zero-sequence current can be considered as independent variables for the calculation of system power loss.

Based on (21), a 3-dimensional (3D) plot depicting the system power loss as a function of the amplitude and phase of zero-sequence current is shown in Fig. 7. It can be observed that the zero-sequence current increases the overall system power loss, and its amplitude and phase both influence the loss. Therefore, it is practically important to minimize the system power loss of the proposed method via optimal zero-sequence current injection.

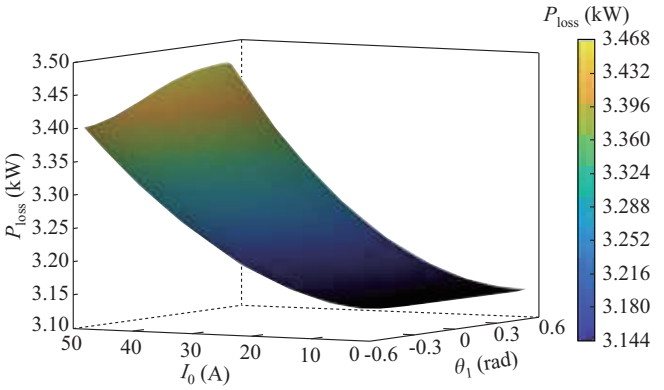

Fig. 7. 3D plot depicting system power loss.

C. Calculation of Optimal Zero-sequence Current

Based on the analysis above, the proposed method redistributes power among the three-phase legs of the D-HVT-

BESS via an appropriate zero-sequence current injection. This action shifts the operating point of each phase leg into its normal operating area. Therefore, the proposed method avoids frequent zero-crossing events of SORC of the battery and enhances the four-quadrant operational capability of the D-HVT-BESS.

Nonetheless, the zero-sequence current increases the additional system power loss. To mitigate this loss, zero-sequence current injection based on minimizing system power loss is used in the proposed method in D-HVT-BESS applications.

As shown in Fig. 8, the zero-sequence current generates zero-sequence power in all three phases, where $i_{0d,ab}$, $i_{0d,bc}$, and $i_{0d,ca}$ are the active components of the zero-sequence current in ab-, bc- and ca-phase, respectively; and $i_{0q,ab}$, $i_{0q,bc}$, and $i_{0q,ca}$ are the reactive components of the zero-sequence current in ab-, bc- and ca-phase, respectively. After the operating points are shifted into their normal areas, the reactive-to-active power ratios of the three-phase legs are expressed as:

$$|Q_{ab}/P_{ab}| = \frac{I_m \sin(\varphi) + I_0 \sin(\theta_1)}{-I_m \cos(\varphi) + I_0 \cos(\theta_1)} \tag{22}$$

$$|Q_{bc}/P_{bc}| = \frac{I_m \sin(\varphi) + I_0 \sin(\pi/3 - \theta_1)}{I_m \cos(\varphi) + I_0 \cos(\pi/3 - \theta_1)} \tag{23}$$

$$|Q_{ca}/P_{ca}| = \frac{I_m \sin(\varphi) - I_0 \sin(\pi/3 + \theta_1)}{I_m \cos(\varphi) + I_0 \cos(\pi/3 + \theta_1)} \tag{24}$$

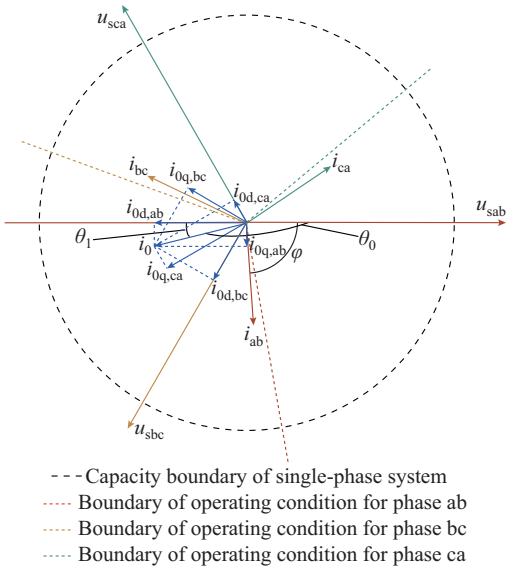

Fig. 8. Phasor diagram of zero-sequence current mapping.

To determine the optimal zero-sequence current i_0, the optimization problem is formulated as:

$$\begin{cases} \min P_{loss} \\ \text{s.t.} \quad \dfrac{|Q_x|}{|P_x|} \le K \\ \sqrt{A_x^2 + B_x^2} \le I_{max} \\ \theta_1 \in [-\pi/6, \pi/6] \end{cases} \quad x = \text{ab, bc, ca} \tag{25}$$

where A_x and B_x are the amplitudes of the active and reactive components of x-phase current after zero-sequence current injection, respectively; and I_{max} is the maximum allowable phase current. Finally, the amplitude and phase angle of the optimal zero-sequence current can be obtained by solving (25).

IV. Inter-phase SOC Balancing Control Strategy

After the zero-sequence current injection, all three-phase legs operate within their respective normal regions. However, the output power becomes unbalanced among the phases, leading to an imbalance of SOC values across the battery clusters of three phases.

Accordingly, an absolute phase selector is designed to facilitate the coordinated control between the inter-phase SOC balancing control and HPRPCC. The SOC values are defined as:

$$\begin{cases} S_x = \dfrac{1}{N}\sum_{j=1}^{N} S_{xj} \quad x = \text{ab, bc, ca} \\ S_{ave} = \dfrac{1}{3}\sum_{x=\text{ab, bc, ca}} S_x \end{cases} \tag{26}$$

where S_{xj} is the SOC value of an individual battery cluster within x-phase; S_x is the average SOC value of x-phase; and S_{ave} is the average SOC value across all three phases. The SOC deviation of x-phase is defined as $\Delta S_x = S_x - S_{ave}$.

Taking the ab-phase as the reference phase for zero-sequence current injection, the principle of the absolute phase selector is described as below.

1) When the initial operating point is located in quadrant I or IV, the zero-sequence current injection causes the ab-phase leg to shift from delivering to absorbing active power. Meanwhile, the active power delivered by the bc- and ca-phases legs increases. Consequently, S_{ab} increases, whereas S_{bc} and S_{ca} decrease.

Therefore, the absolute phase reference switches to the bc-phase under either of the following conditions: ① ΔS_{ab} exceeds its limit σ and $S_{bc} < S_{ca}$; ② ΔS_{bc} falls below $-\sigma$.

Conversely, the absolute phase reference switches to the ca-phase under either of the following conditions: ① ΔS_{ab} exceeds σ and $S_{bc} > S_{ca}$; ② ΔS_{ca} falls below $-\sigma$.

2) When the initial operating point is located in quadrant II or III, the zero-sequence current injection causes the ab-phase leg to shift from absorbing to delivering active power. Concurrently, the active power absorbed by the bc- and ca-phases legs increases. Consequently, S_{ab} decreases, whereas S_{bc} and S_{ca} increase.

Therefore, the absolute phase reference switches to the bc-phase under either of the following conditions: ① ΔS_{ab} falls below $-\sigma$ and $S_{bc} > S_{ca}$; ② ΔS_{bc} exceeds σ.

Conversely, the absolute phase reference switches to the ca-phase under either of the following conditions: ① ΔS_{ab} falls below $-\sigma$ and $S_{bc} < S_{ca}$; ② ΔS_{ca} exceeds σ.

Then, the principle of absolute phase switching is similar when zero-sequence current is injected based on the bc- or ca-phase, and it will not be discussed further.

The inter-phase SOC balancing control strategy in this paper is illustrated in Fig. 9, where θ_u is the absolute phase angle. And the conditions ①-⑥ required for absolute phase switching are summarized in Table II.

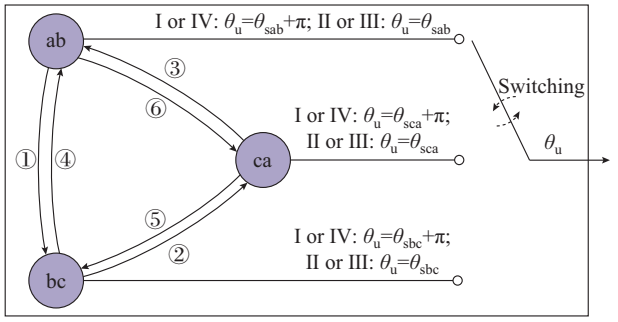

Fig. 9. Inter-phase SOC balancing control strategy.

TABLE II
DIFFERENT CONDITIONS FOR ABSOLUTE PHASE SWITCHING

Condition	Quadrant I or IV	Quadrant II or III
①	$\Delta S_{ab}>\sigma$ and $S_{bc}<S_{ca}$; or $\Delta S_{bc}<-\sigma$	$\Delta S_{ab}<-\sigma$ and $S_{bc}>S_{ca}$; or $\Delta S_{bc}>\sigma$
②	$\Delta S_{bc}>\sigma$ and $S_{ab}>S_{ca}$; or $\Delta S_{ca}<-\sigma$	$\Delta S_{bc}<-\sigma$ and $S_{ab}<S_{ca}$; or $\Delta S_{ca}>\sigma$
③	$\Delta S_{ca}>\sigma$ and $S_{ab}<S_{bc}$; or $\Delta S_{ab}<-\sigma$	$\Delta S_{ca}<-\sigma$ and $S_{ab}>S_{bc}$; or $\Delta S_{ab}>\sigma$
④	$\Delta S_{bc}>\sigma$ and $S_{ab}<S_{ca}$; or $\Delta S_{ab}<-\sigma$	$\Delta S_{bc}<-\sigma$ and $S_{ab}>S_{ca}$; or $\Delta S_{ab}>\sigma$
⑤	$\Delta S_{ca}>\sigma$ and $S_{ab}>S_{bc}$; or $\Delta S_{bc}<-\sigma$	$\Delta S_{ca}<-\sigma$ and $S_{ab}<S_{bc}$; or $\Delta S_{bc}>\sigma$
⑥	$\Delta S_{ab}>\sigma$ and $S_{bc}>S_{ca}$; or $\Delta S_{ca}<-\sigma$	$\Delta S_{ab}<-\sigma$ and $S_{bc}<S_{ca}$; or $\Delta S_{ca}>\sigma$

The overall control block diagram of the system is shown in Fig. 10. Under this configuration, the current loop utilizes a phase-separated control strategy based on a quasi-proportional resonant (QPR) controller. And carrier phase-shift sinusoidal pulse width modulation (CPS-SPWM) is adopted as the modulation scheme.

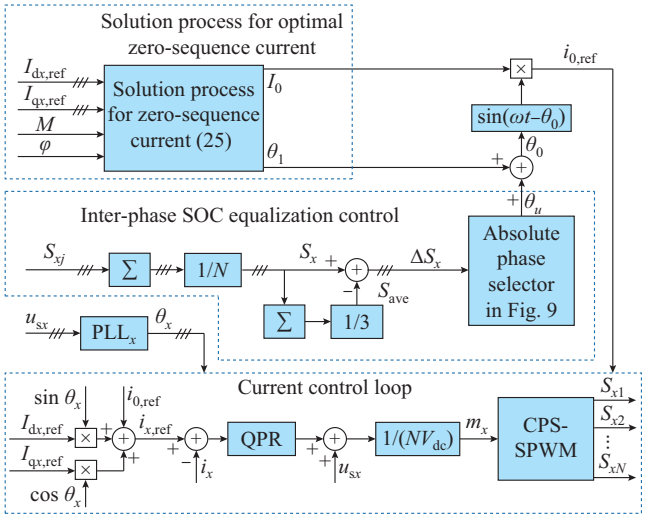

Fig. 10. Overall control block diagram of system.

V. EXPERIMENTAL VERIFICATION

A. Results of Experimental Verification

A 380 V/100 kW/50 kWh experimental prototype of the D-HVT-BESS has been developed to validate the proposed method. The setup is depicted in Supplementary Material A Fig. SA1, with system parameters detailed in Table III.

TABLE III
SYSTEM PARAMETERS

Parameter	Value
Grid line voltage u_g	380 V
Grid frequency f_0	50 Hz
Switching frequency f_{sw}	10 kHz
System capacity S	100 kW
Cascade number N	2
AC filter inductance L_s	1 mH
DC filter inductance L_{dc}	2.5 mH
DC filter capacitor C_{dc}	13160 μF
DC voltage V_{bat}	400 V
Core parameters C_m, α, and β	3.388, 1.7, and 1.9
IGBT module	FF200R06KE3

By substituting the parameters from Table III into (6), the boundary value of K for the system to enter the HPRPCC conditions is calculated as 11.95. The corresponding power factor threshold is 0.083. Therefore, when $|\cos(\varphi)|$ falls below 0.083, the system operates under the HPRPCC condition.

The effectiveness of the proposed method is validated through the following four case studies.

1) Case 1: the initial system outputs are set to be an active power of 5 kW and a reactive power of 80 kvar, resulting in a power factor $\cos(\varphi)=0.062$.

2) Case 2: the initial system outputs are set to be an active power of −5 kW and a reactive power of 80 kvar, resulting in a power factor $\cos(\varphi)=-0.062$.

3) Case 3: the initial system outputs are set to be an active power of zero and a reactive power of 80 kvar, resulting in a power factor $\cos(\varphi)=0$.

4) Case 4: the initial system outputs are set to be an active power of zero and a reactive power of −80 kvar, resulting in a power factor $\cos(\varphi)=0$.

The amplitudes and phases of the optimal zero-sequence current required in the four cases are shown in Fig. 11.

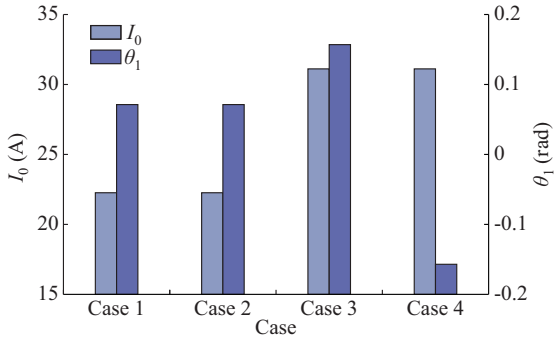

Fig. 11. Amplitudes and phases of optimal zero-sequence current required in four cases.

Figure 12 shows the overall waveforms of the three-phase battery currents $i_{bat,x}$ in the four cases. In all cases, the system operates at the initial operating point from time t_0 to t_1. At time t_1, the proposed method and the inter-phase SOC bal-

ancing control strategy are activated. As shown in Fig. 12, zero-crossing points exist in the battery currents before t_1 in all four cases, while no zero-crossing points are observed after t_1. These results demonstrate that the proposed method can effectively avoid zero-crossing battery current under HPRPCC conditions.

The waveforms of SOC deviation ΔS_x in the four cases under the inter-phase SOC balancing control strategy are present in Fig. 13. As observed in Fig. 12 and Fig. 13, ΔS_x can be constrained within the range of –0.4% to 0.4% by the inter-phase SOC balancing control strategy.

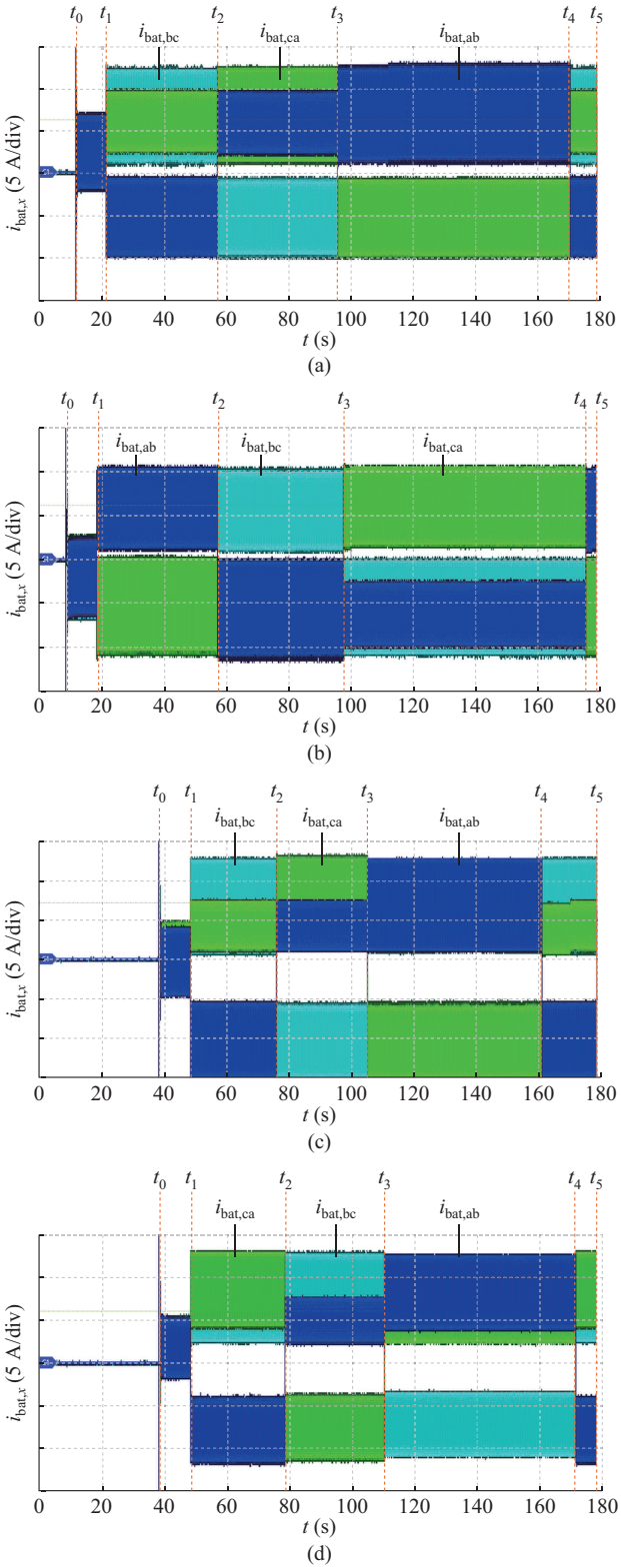

Fig. 12. Overall waveform of three-phase battery current in four cases. (a) Case 1. (b) Case 2. (c) Case 3. (d) Case 4.

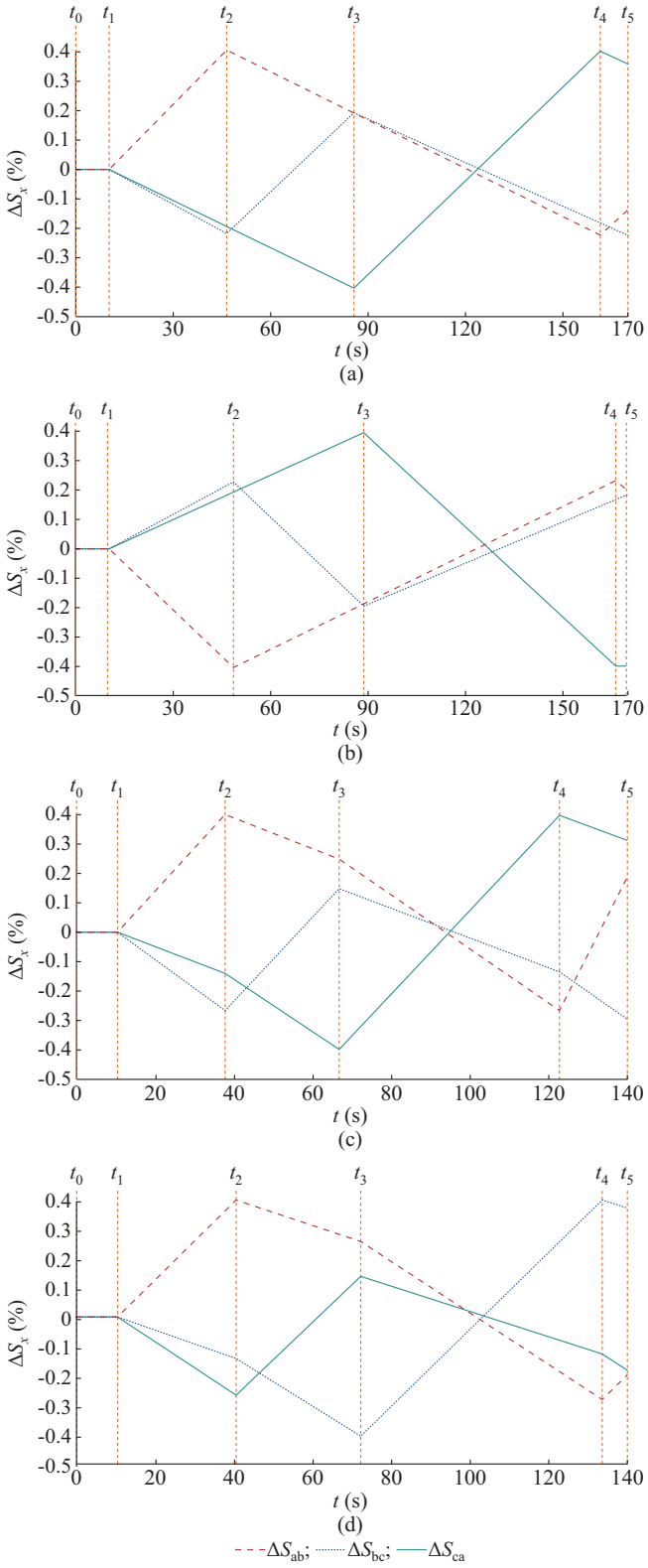

Fig. 13. Waveforms of SOC deviation in four cases. (a) Case 1. (b) Case 2. (c) Case 3. (d) Case 4.

The system power losses in the four cases before and after the zero-sequence current injection are shown in Fig. 14. It can be observed from Fig. 14 that after the zero-sequence current injection, the system efficiency decreases slightly in all the four cases: from 95.99%, 95.983%, 96.014%, and 96.072% to 95.794%, 95.787%, 95.606%, and 95.667% in Cases 1-4, respectively.

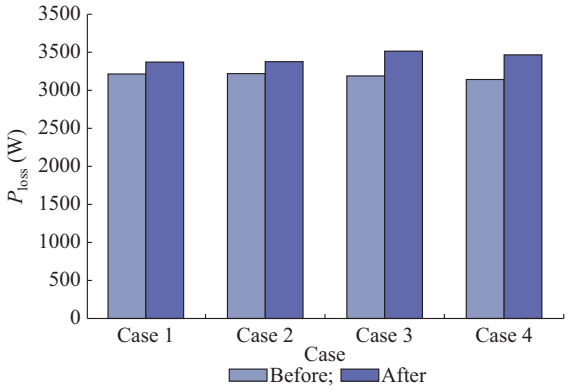

Fig. 14. System power losses in four cases before and after zero-sequence current injection.

The experimental results indicate that the system power loss is relatively small and within the acceptable range. In other words, this slight reduction in efficiency is a worthwhile trade-off for extending the lifespan of both the battery and the entire system [12], [13].

Therefore, the proposed method, which optimizes the zero-sequence current amplitude and phase to minimize the system power loss, is proven to be feasible.

The waveforms of the battery currents and phase currents in Cases 1-4 are presented in Supplementary Material B Figs. SB1-SB4, respectively, for the four time-intervals.

Then, based on Fig. 13 and Supplementary Material B Figs. SB1-SB4, it can be observed that the zero-crossing frequency of the battery current is 100 Hz during the time interval from t_0 to t_1. However, from t_1 to t_5, the three-phase system operates within its normal operating region. Therefore, during this period, there are no zero-crossing in the battery currents of the three-phase legs.

1) Case 1

As shown in Fig. 13(a) and Supplementary Material B Fig. SB1, the zero-sequence current exhibits different reference phases and absolute phase angles during each subinterval between t_1 and t_5.

During t_1-t_2, ab-phase serves as the reference, and the absolute phase angle of the zero-sequence current is given by $\theta_u = \theta_{sab} + \pi$.

During t_2-t_3, bc-phase serves as the reference, and the absolute phase angle is given by $\theta_u = \theta_{sbc} + \pi$.

During t_3-t_4, ca-phase serves as the reference, and the absolute phase angle is given by $\theta_u = \theta_{sca} + \pi$.

During t_4-t_5, the reference returns to ab-phase, and the absolute phase angle is given by $\theta_u = \theta_{sab} + \pi$.

2) Case 2

Similarly, as shown in Fig. 13(b) and Supplementary Material B Fig. SB2, the zero-sequence current exhibits different reference phases and absolute phase angles during each subinterval between t_1 and t_5.

During t_1-t_2, ab-phase serves as the reference, and the absolute phase angle of the zero-sequence current is given by $\theta_u = \theta_{sab}$.

During t_2-t_3, bc-phase serves as the reference, and the absolute phase angle is given by $\theta_u = \theta_{sbc}$.

During t_3-t_4, ca-phase serves as the reference, and the absolute phase angle is given by $\theta_u = \theta_{sca}$.

During t_4-t_5, the reference returns to ab-phase, and the absolute phase angle is given by $\theta_u = \theta_{sab}$.

3) Case 3

As shown in Fig. 13(c) and Supplementary Material B Fig. SB3, the zero-sequence current exhibits different reference phases and absolute phase angles during each subinterval between t_1 and t_5.

During t_1-t_2, ab-phase serves as the reference, and the absolute phase angle of the zero-sequence current is given by $\theta_u = \theta_{sab} + \pi$.

During t_2-t_3, bc-phase serves as the reference, and the absolute phase angle is given by $\theta_u = \theta_{sbc} + \pi$.

During t_3-t_4, ca-phase serves as the reference, and the absolute phase angle is given by $\theta_u = \theta_{sca} + \pi$.

During t_4-t_5, the reference returns to ab-phase, and the absolute phase angle is given by $\theta_u = \theta_{sab} + \pi$.

4) Case 4

As shown in Fig. 13(d) and Supplementary Material B Fig. SB4, the zero-sequence current exhibits different reference phases and absolute phase angles during each subinterval between t_1 and t_5.

During t_1-t_2, ab-phase serves as the reference, and the absolute phase angle of the zero-sequence current is given by $\theta_u = \theta_{sab} + \pi$.

During t_2-t_3, ca-phase serves as the reference, and the absolute phase angle is given by $\theta_u = \theta_{sca} + \pi$.

During t_3-t_4, bc-phase serves as the reference, and the absolute phase angle is given by $\theta_u = \theta_{sbc} + \pi$.

During t_4-t_5, the reference returns to ab-phase, and the absolute phase angle is given by $\theta_u = \theta_{sab} + \pi$.

The above four cases show that the proposed method can effectively prevent frequent zero-crossing of the SORC while maintaining a relatively small system power loss increment induced by the zero-sequence current, thereby mitigating degradation of the battery lifespan. In addition, the inter-phase SOC balancing control strategy can guarantee the inter-phase SOC dynamic balance.

B. Comparison Between Proposed Method and Traditional SORC Suppression Methods

Although the active power decoupling method [14] - [17] and the virtual impedance method based on DC-DC converter [18], [19] can effectively suppress the fluctuation amplitude of SORC, they increase the system cost and control complexity. In addition, the passive filtering method [20], [21] and the harmonic injection method [23] can also effectively suppress the SORC amplitude. While these two methods can reduce ripple amplitude and thus reduce the probability of dual-frequency charging and discharging, the latter requires additional AC-side harmonic filters, leading to in-

creased cost. Furthermore, the average battery current in both methods may still be less than the SORC amplitude under low power factor conditions. Consequently, the battery current still undergoes repeated zero-crossing, which significantly threatens the battery lifespan.

In contrast, the proposed method in this paper can avoid zero-crossing of SORC by using only passive filtering, so as to avoid SORC damage to the battery and prolong the battery lifespan without significantly increasing the hardware and software costs.

VI. Conclusion

Under low power factor conditions, the frequent zero-crossing of SORC in the D-HVT-BESS accelerates the battery degradation. To mitigate this problem, an HPRPCC method for D-HVT-BESS is proposed. The proposed method includes a zero-sequence current injection optimized to minimize the system power loss, and an inter-phase SOC balancing control strategy based on an absolute phase selector. Within the proposed method, the zero-sequence current redistributes the three-phase power distributions and shifts the operating point of three-phase legs from the operating area of HPRPCC to the normal operating area, thus avoiding the zero-crossing of SORC. Additionally, the amplitude and phase of zero-sequence current are optimized to minimize the system power loss, which is beneficial to reduce the extra system power loss. In addition, the inter-phase SOC balancing control strategy can optimize the absolute phase of zero-sequence current in real time and ensure the inter-phase SOC dynamic balance. Finally, experimental results confirm that, under HPRPCC conditions, the proposed method effectively prevents zero-crossing in the three-phase battery currents and ensures dynamic SOC balance across three phases.

References

[1] H. He, N. Zhang, C. Kang *et al.*, "Communication resources allocation for time delay reduction of frequency regulation service in high renewable penetrated power system," *CSEE Journal of Power and Energy Systems*, vol. 10, no. 2, pp. 468-480, Mar. 2024.

[2] IRENA. (2018, Apr.). Global energy transformation: a roadmap to 2050. [Online]. Available: https://www.irena.org/publications/2018/Apr/Global-Energy-Transition-A-Roadmap-to-2050

[3] H. Chen, C. Pilong, P. Rocha-Garrido *et al.*, "Grid resilience with high renewable penetration: a PJM approach," *IEEE Transactions on Sustainable Energy*, vol. 14, no. 2, pp. 1169-1177, Apr. 2023.

[4] H. Bevrani and F. Milano, "Guest editorial: special section on dynamic performance and flexibility enhancement of RES-dominated power systems with grid-forming converters," *Journal of Modern Power Systems and Clean Energy*, vol. 13, no. 1, pp. 1-2, Jan. 2025.

[5] Q. Zhang, P. R. Kumar, and L. Xie, "An average power-based planning framework of transmission expansion: a new role for energy storage," *IEEE Open Access Journal of Power and Energy*, vol. 12, pp. 122-134, Mar. 2025.

[6] Y. Riffonneau, S. Bacha, F. Barruel *et al.*, "Optimal power flow management for grid connected PV systems with batteries," *IEEE Transactions on Sustainable Energy*, vol. 2, no. 3, pp. 309-320, Jul. 2011.

[7] J. Zhang, X. Huang, J. Zhou *et al.*, "A capacity-expandable cascaded multilevel energy storage system based on laminated power modules," *IEEE Transactions on Power Electronics*, vol. 40, no. 4, pp. 5265-5278, Apr. 2025.

[8] L. Maharjan, S. Inoue, and H. Akagi, "A transformerless energy storage system based on a cascade multilevel PWM converter with star configuration," *IEEE Transactions on Industry Applications*, vol. 44, no. 5, pp. 1621-1630, Sept.-Oct. 2008.

[9] C. Liu, N. Gao, X. Cai *et al.*, "Differentiation power control of modules in second-life battery energy storage system based on cascaded H-bridge converter," *IEEE Transactions on Power Electronics*, vol. 35, no. 6, pp. 6609-6624, Jun. 2020.

[10] Y. Yu, G. Konstantinou, C. D. Townsend *et al.*, "Delta-connected cascaded H-bridge multilevel converters for large-scale photovoltaic grid integration," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 8877-8886, Nov. 2017.

[11] Z. Ji, Y. Sun, D. Li *et al.*, "Comparative analysis for unbalance compensation of cascaded H-bridge STATCOMs between star and delta configuration," *High Voltage Engineering*, vol. 41, no. 7, pp. 2435-2444, Jul. 2015.

[12] X. Hu, K. Zhang, K. Liu *et al.*, "Advanced fault diagnosis for lithium-ion battery systems: a review of fault mechanisms, fault features, and diagnosis procedures," *IEEE Industrial Electronics Magazine*, vol. 14, no. 3, pp. 65-91, Sept. 2020.

[13] K. A. Severson, P. M. Attia, N. Jin *et al.*, "Data-driven prediction of battery cycle life before capacity degradation," *Nature Energy*, vol. 4, pp. 383-391, May 2019.

[14] A. C. Kyritsis, N. P. Papanikolaou, and E. C. Tatakis, "A novel parallel active filter for current pulsation smoothing on single stage grid-connected AC-PV modules," in *Proceedings of the 2007 European Conference on Power Electronics and Applications*, Aalborg, Denmark, Sept. 2007, pp. 1-10.

[15] X. Cao, Q.-C. Zhong, and W.-L. Ming, "Ripple eliminator to smooth DC-bus voltage and reduce the total capacitance required," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 4, pp. 2224-2235, Apr. 2015.

[16] V.-T. Nguyen, J.-W. Kim, J.-W. Park *et al.*, "A modified sub-module of modular multilevel converter using active power decoupling method for reducing capacitor voltage ripple under low-frequency operation," *IET Power Electronics*, vol. 16, no. 5, pp. 868-882, Apr. 2023.

[17] X. Wang, M. Chen, B. Li *et al.*, "Multifunction control strategy for single-phase AC/DC power conversion systems with voltage-sensorless power-decoupling function," *IEEE Transactions on Power Electronics*, vol. 35, no. 12, pp. 13602-13620, Dec. 2020.

[18] G. Zhu, X. Ruan, L. Zhang *et al.*, "On the reduction of second harmonic current and improvement of dynamic response for two-stage single-phase inverter," *IEEE Transactions on Power Electronics*, vol. 30, no. 2, pp. 1028-1041, Feb. 2015.

[19] X. Huang, X. Ruan, L. Zhang *et al.*, "Second harmonic current reduction schemes for DC-DC converter in two-stage PFC converters," *IEEE Transactions on Power Electronics*, vol. 37, no. 1, pp. 332-343, Jan. 2022.

[20] Y. Sun, Y. Liu, M. Su *et al.*, "Review of active power decoupling topologies in single-phase systems," *IEEE Transactions on Power Electronics*, vol. 31, no. 7, pp. 4778-4794, Jul. 2016.

[21] C. Liu, X. Shi, R. Li *et al.*, "Main circuit's parametric optimal design counting inconsistent battery parameters and control of 35 kV large-capacity transformer-less BESS," *IEEE Transactions on Energy Conversion*, vol. 40, no. 1, pp. 16-29, Mar. 2025.

[22] X. Shi, C. Zhang, R. Li *et al.*, "Control scheme for second harmonic current elimination in single-star configuration based cascade multilevel energy storage system," *IEEE Journal of Emerging and Selected Topics in Industrial Electronics*, vol. 3, no. 4, pp. 1210-1216, Oct. 2022.

[23] Z. Li, R. Lizana, S. M. Lukic *et al.*, "Current injection methods for ripple-current suppression in delta-configured split-battery energy storage," *IEEE Transactions on Power Electronics*, vol. 34, no. 8, pp. 7411-7421, Aug. 2019.

[24] L. Deng, X. Zhou, and L. Hong, "DC secondary ripple suppression method for HCC-HVDC under asymmetric grid fault conditions," *IEEE Transactions on Power Delivery*, vol. 40, no. 3, pp. 1634-1646, Jun. 2025.

[25] H. Ding, F. Ma, R. Han *et al.*, "Loss-balancing control strategy for single-phase MMC with asymmetric phase leg structure," *IEEE Transactions on Power Electronics*, vol. 39, no. 2, pp. 2063-2075, Feb. 2024.

[26] Y. Zhang, H. Wang, Z. Wang *et al.*, "Simplified thermal modeling for IGBT modules with periodic power loss profiles in modular multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 3, pp. 2323-2332, Mar. 2019.

[27] S. Mohamadian, M. Modarres, F. Simonetti *et al.*, "Modeling of switching power losses in cascaded H-bridges with unipolar PWM," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 11, no. 3, pp. 3270-3280, Jun. 2023.

[28] Y. Zhang, H. Wang, Z. Wang *et al.*, "Mission profile-based system-lev-

el reliability prediction method for modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 35, no. 7, pp. 6916-6930, Jul. 2020.

Xiaoping Zhou received the B.S. and Ph.D. degrees in electrical engineering from Hunan University, Changsha, China, in 2013 and 2018, respectively. He is currently a Professor of Electrical Engineering with Hunan University. His research interests include high-voltage direct current (HVDC) system, distributed generation, power quality, and energy storage.

Yizhen Hu received the B.S. degree in electrical engineering from Henan University of Technology, Zhengzhou, China, in 2020. He is currently working toward the Ph.D. degree in electrical engineering with Hunan University, Changsha, China. His research interest includes power electronic converter.

Lerong Hong received the B.S. and Ph.D. degrees in electrical engineering from Hunan University, Changsha, China, in 2016 and 2021, respectively. He is currently an Associate Professor of Electrical Engineering with Hunan University. His research interests include HVDC system and power electronic converter.

Qianming Xu received the B.S. degree in electrical engineering and automation and the Ph.D. degree in electrical engineering from Hunan University, Changsha, China, in 2012 and 2017, respectively. Since 2023, he has been a Professor with the College of Electrical and Information Engineering, Hunan University. His research interests include multilevel converter, power electronic reliability monitoring, and power quality control.

Fenfen Zhu received the B.S. degree in electrical engineering from Anhui University, Hefei, China, in 2021, and the M.S. degree in electrical engineering from Hunan University, Changsha, China, in 2024. In 2024, she joined State Grid Wuhu Electric Power Supply Company, Wuhu, China. Her research interest includes power electronic converter.

Lingfeng Deng received the B.S. degree from China University of Mining and Technology, Xuzhou, China, in 2018, and the M.S. and Ph.D. degrees from Hunan University, Changsha, China, in 2021 and 2025, respectively. He is currently a Lecturer with the School of Electrical Engineering, China University of Mining and Technology. His research interests include HVDC system and application of novel power electronic device in power system.

Lei Zhang received the B.S. degree in electrical engineering from Guizhou University, Guiyang, China, in 2021. He is currently working toward the Ph.D. degree in Hunan University, Changsha, China. His research interests include power electronic converter and energy storage.

Hanting Peng received the B.S. degrees in electrical engineering from Hunan University, Changsha, China, in 2021. He is currently working toward the Ph.D. degree in Hunan University. His research interests include power electronic converter and HVDC system.

Zhen Zhang received the B.S. degree in electrical engineering from Zhengzhou University, Zhengzhou, China, in 2022. He is currently working toward the Ph.D. degree in electrical engineering in Hunan University, Changsha, China. His research interest includes power electronic converter.

Le Li received the B.S. degree in electrical engineering from East China Jiaotong University, Nanchang, China, in 2023. He is currently working toward the M.S. degree in electrical engineering in Hunan University, Changsha, China. His research interest includes power electronic converter.

Ruotong Wang received the B.S. degree in electrical engineering from China University of Mining and Technology, Xuzhou, China, in 2023. She is currently working toward the M.S. degree in electrical engineering in Hunan University, Changsha, China. Her research interest includes power electronic converter.