

Maximizing Dynamic Voltage Support Capability of LCC-HVDC Systems Under Transient Voltage Disturbances

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Abstract—The sending-end system of line-commutated converter based high-voltage direct current (LCC-HVDC) systems is vulnerable to transient voltage disturbances (TVDs), posing a significant threat to voltage stability. This paper proposes a novel strategy to maximize the dynamic voltage support (DVS) capability of LCC-HVDC systems under various TVDs. The physical mechanisms underlying DVS in LCC-HVDC systems are systematically analyzed, forming the basis for an optimization model that maximizes the DVS capability while incorporating security constraints at both the rectifier and inverter ends. To address the challenge of directly solving the model, an optimality analysis with intuitive geometric interpretations is performed. Based on these insights, a two-stage optimal DVS control strategy for LCC-HVDC systems is developed to iteratively approach the optimal solution through coordinated control of the rectifier and inverter stations. The effectiveness and superiority of the proposed strategy in supporting the sending-end system are validated through dynamic simulations, and its applicability under practical operating conditions is discussed.

Index Terms—Dynamic voltage support (DVS), line-commutated converter based high-voltage direct current (LCC-HVDC), transient voltage disturbance, sending-end system, voltage stability.

I. INTRODUCTION

DUE to the significant distances between large-scale wind farms (WFs) and major load centers, line-commutated converter based high-voltage direct current (LCC-HVDC) systems are considered the most cost-effective solution for long-distance bulk power transmission [1]. However,

the increasing penetration of WFs and LCC-HVDC lines has substantially reduced the reactive power support capability of the sending-end system, thereby heightening the risks and impacts of transient voltage disturbances (TVDs) at the sending end, which may be caused by both sending-end and receiving-end grid faults [2]–[5]. Such sending-end TVDs can trigger cascading tripping of wind turbine generators (WTGs) [6] and, in severe cases, result in voltage collapse, thereby constraining the transmission capacity of LCC-HVDC systems [7]. Numerous real-world fault events have underscored these challenges [8].

Deploying devices such as synchronous condensers is one approach to enhancing voltage stability under TVDs [9]; however, it significantly increases system costs. An alternative and more cost-effective solution involves improving the converter control strategy to provide dynamic voltage support (DVS), i.e., injecting reactive current during abnormal voltage conditions based on locally measured AC voltage [10]. Advanced control strategies have been developed to enhance the DVS capabilities of inverter-based resources (IBRs), including energy storage systems, photovoltaic systems, and WTGs [11]–[17]. These studies demonstrate the substantial benefits of DVS in improving voltage stability under various conditions.

With capacities reaching several gigawatts, LCC-HVDC systems offer considerable potential to contribute to grid voltage support, provided their operational flexibility is effectively utilized. Although previous studies have investigated voltage support under steady-state conditions [18]–[20], DVS under large disturbances like TVDs remains unaddressed in both current grid codes and existing research. The primary challenge arises from the semi-controlled nature of thyristor-based LCC-HVDC systems, in which active and reactive power controls are inherently coupled within each converter station, and the operations of the rectifier and inverter stations are mutually interdependent [21]. Consequently, their controllability under transient conditions is often considered limited [18].

Several dedicated control strategies have been proposed to address specific types of TVDs. Reference [22] introduced a constant reactive power control strategy to reduce transient overvoltages following commutation failures (CFs). Reference [23] proposed to increase reactive power absorption at

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the rectifier station to effectively mitigate transient overvoltages caused by sending-end AC faults. Reference [24] developed an improved closed-loop reactive power control strategy, which enhances transient low-voltage and suppresses overvoltages caused by CFs. While these strategies are effective for their targeted disturbances, their applicability to other fault types is limited due to the diverse nature of disturbance mechanisms. Moreover, these strategies lack optimality analysis and do not fully utilize the voltage support potential of LCC-HVDC systems.

This paper addresses these gaps by investigating the DVS capability of LCC-HVDC systems under TVDs and proposing a strategy to unlock their full potential in supporting the sending-end system. The main contributions are as follows.

1) The DVS capability of LCC-HVDC systems and the underlying physical principles are thoroughly analyzed, resulting in an optimization model that maximizes the DVS capability. An accompanying optimality analysis with intuitive geometric illustrations is also provided.

2) A practical two-stage optimal DVS control strategy for LCC-HVDC systems is proposed to iteratively approach the optimal solution under various conditions. Security constraints are managed through localized and indirect coordination of the rectifier and inverter stations, ensuring robust and feasible implementation.

The remainder of this paper is organized as follows. Section II establishes the equivalent model of the sending-end system and examines the mechanisms of various TVDs. Section III formulates the DVS problem and presents the proposed strategy. Section IV details the implementation of the proposed strategy. Section V presents the simulation results. Finally, Section VI concludes the paper.

II. EQUIVALENT MODEL OF SENDING-END SYSTEM AND MECHANISMS OF VARIOUS TVDs

This section is devoted to modeling the WF-integrated LCC-HVDC sending-end system and elucidating the mechanisms of three types of AC/DC fault-induced TVDs. Then, the potential of LCC-HVDC systems to offer DVS is demonstrated.

A. System Modeling

A typical WF-integrated LCC-HVDC sending-end system and equivalent circuit are depicted in Fig. 1. Generally, the electrical distance between WFs and the LCC-HVDC rectifier station is short, i.e., line impedance $R_w + jX_w$ is negligible. Thus, the sending-end system can be modeled as shown in Fig. 1. WFs are aggregated into a single machine represented by a current source $I_w = I_{wd} + jI_{wq}$ [25], where I_{wd} and I_{wq} are the equivalent active and reactive currents of WFs, respectively. The rest of the AC grid is equivalently represented by a Thévenin circuit [26], where \dot{E}_{sr} is the Thévenin equivalent voltage; R_r and X_r are the Thévenin equivalent resistance and reactance, respectively; P_r and Q_r are the active and reactive power provided by the AC grid, respectively; and \dot{U}_{pr} is the voltage at point of common coupling (PCC). The rectifier station is modeled as a variable load $P_{dr} + jQ_{dr}$, where P_{dr} and Q_{dr} are the DC active and reactive power, re-

spectively, while reactive power compensators (RPCs) within the station are represented by an equivalent susceptance B_c . Note that this paper focuses on the voltage-sustaining stage, occurring approximately 2-3 cycles after the fault onset, during which the voltage is predominantly determined by its fundamental component [27], [28]. Hence, quasi-static models are adopted for the analyses.

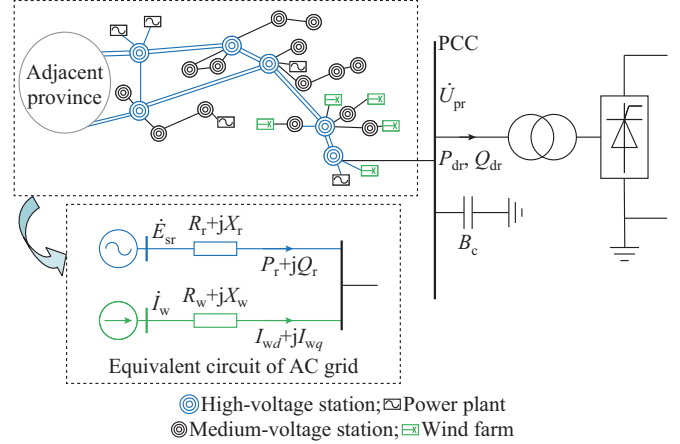


Fig. 1. Typical WF-integrated LCC-HVDC sending-end system and equivalent circuit.

Referring to Fig. 1, the following relationships hold:

$$\dot{E}_{sr} - \dot{U}_{pr} = \dot{I}_{sr} (R_r + jX_r) \quad (1)$$

$$\dot{U}_{pr} \dot{I}_{sr}^* + \dot{U}_{pr} (I_{wd} + jI_{wq})^* = P_{dr} + j(Q_{dr} - Q_{cr}) \quad (2)$$

where $*$ is the conjugate operator; \dot{I}_{sr} is the current provided by the AC system; and $Q_{cr} = B_c U_{pr}^2$ is the reactive power generated by RPCs. All parameters are per-unit values, with the base capacity set to be the rated high-voltage direct current (HVDC) power.

By combining (1) and (2) and separating the real and imaginary parts, the following expressions can be obtained:

$$E_{sr} U_{pr} \cos(\theta) - U_{pr}^2 + U_{pr} (I_{wd} R_r - I_{wq} X_r) = P_{dr} R_r + (Q_{dr} - B_c U_{pr}^2) X_r \quad (3)$$

$$E_{sr} U_{pr} \sin(\theta) - U_{pr}^2 (I_{wd} X_r + I_{wq} R_r) = -P_{dr} X_r + (Q_{dr} - B_c U_{pr}^2) R_r \quad (4)$$

where symbols without an overdot represent the magnitude of the corresponding quantity; and θ is the phase angle between \dot{E}_{sr} and \dot{U}_{pr} . Eliminating θ from (3) and (4) yields the following equation:

$$F(U_{pr}, P_{dr}, Q_{dr}, I_{wd}, I_{wq}) = aU_{pr}^4 + bU_{pr}^3 + cU_{pr}^2 + dU_{pr} + e = 0 \quad (5)$$

where $F(\cdot)$ is an algebraic function; and a , b , c , d , and e are the coefficients, with detailed coefficients provided in Supplementary Material A.

Studies in [29], [30] have demonstrated that the behaviors of I_{wd} and I_{wq} are voltage-dependent, and can be approximated using first-order polynomials:

$$\begin{cases} I_{wd} = K_{p1} U_{pr} + K_{p2} \\ I_{wq} = K_{q1} U_{pr} + K_{q2} \end{cases} \quad (6)$$

where K_{p1} , K_{p2} , K_{q1} , and K_{q2} are the coefficients that vary depending on the system operation state (normal or fault ride-through). The validity and accuracy of this equivalent

modeling approach have been confirmed through extensive simulations and large-scale field applications [29], [30].

Substituting (6) into (5), we obtain:

$$F(U_{pr}, P_{dr}, Q_{dr}) = a_2 U_{pr}^4 + b_2 U_{pr}^3 + c_2 U_{pr}^2 + d_2 U_{pr} + e = 0 \quad (7)$$

$$a_2 = 1 - 2K_{p1}R_r - 2(B_c - K_{Q1})X_r + \frac{(B_c^2 + K_{p1}^2 + K_{Q1}^2 - 2B_c K_{Q1})Z_r^2}{(B_c^2 + K_{p1}^2 + K_{Q1}^2 - 2B_c K_{Q1})Z_r^2} \quad (8a)$$

$$b_2 = 2[K_{Q2}X_r - K_{p2}R_r + (K_{p1}K_{p2} + K_{Q1}K_{Q2} - B_c K_{Q2})Z_r^2] \quad (8b)$$

$$c_2 = \frac{2(P_{dr}R_r + Q_{dr}X_r) - E_{sr}^2 + [K_{p2}^2 + K_{Q2}^2 - 2(K_{p1}P_{dr} - K_{Q1}Q_{dr} + B_c Q_{dr})]Z_r^2}{2(K_{p1}P_{dr} - K_{Q1}Q_{dr} + B_c Q_{dr})Z_r^2} \quad (8c)$$

$$d_2 = 2Z_r^2(-K_{p2}P_{dr} + K_{Q2}Q_{dr}) \quad (8d)$$

where $Z_r = \sqrt{R_r^2 + X_r^2}$ is the Thévenin equivalent impedance; and a_2 , b_2 , c_2 , and d_2 are the coefficients.

Equation (7) is a quartic polynomial with respect to U_{pr} , revealing the relationship among U_{pr} , grid parameters (E_{sr} , R_r , X_r), and converter consumed power (P_{dr} , Q_{dr}), while accounting for the impact of WFs. Unlike simpler cases involving only HVDC or WFs, all five coefficients (a_2 , b_2 , c_2 , d_2 , e) exist here, making it challenging to derive an explicit analytical expression for $U_{pr}(P_{dr}, Q_{dr})$ from (7) for theoretical studies.

B. Mechanisms of Various TVDs

In LCC-HVDC projects, TVDs at the sending end can be triggered by faults occurring at either the sending or receiving end. This paper focuses on three representative types of TVDs: voltage sag caused by sending-end AC faults, voltage swell resulting from reactive power surplus, and the “first decrease and then increase” TVD induced by CFs, which is typically caused by receiving-end faults. Although it is challenging to derive an explicit expression for $U_{pr}(P_{dr}, Q_{dr})$, the mechanisms of TVDs can be analyzed using (7) by visualizing the relationships among U_{pr} , P_{dr} , and Q_{dr} through numerical calculations.

The P_{dr} - Q_{dr} - U_{pr} surfaces with different E_{sr} are shown in Fig. 2, with parameters used in the numerical calculations provided in Supplementary Material A.

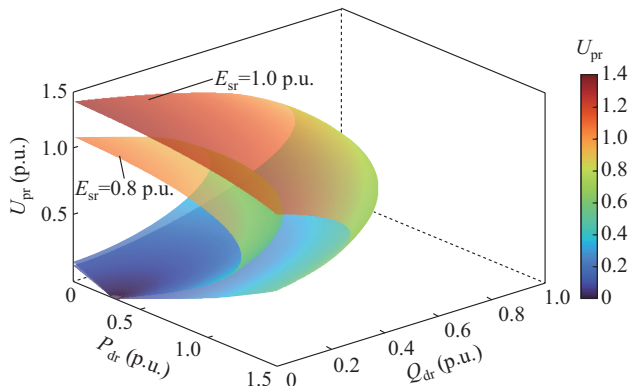


Fig. 2. P_{dr} - Q_{dr} - U_{pr} surfaces with different E_{sr} .

As depicted in Fig. 2, the causes of TVDs can be broadly categorized as follows.

1) Changes in grid parameters: variations in grid parameters alter the system equations and reshape the P_{dr} - Q_{dr} - U_{pr}

surface. As a result, voltage sags or swells can occur even if P_{dr} and Q_{dr} are controlled to remain constant.

2) Changes in “load” power: the P_{dr} - Q_{dr} - U_{pr} surface remains unchanged, but shifts in the operating point (P_{dr} , Q_{dr}) on the surface cause TVD.

Additionally, each P_{dr} - Q_{dr} - U_{pr} surface is divided into upper and lower regions by a curve representing saddle-node bifurcation voltage instability [31]. This paper focuses on the upper region of the surface, trying to enhance voltage profile and mitigate voltage instability through the DVS capability of the LCC-HVDC system. A brief overview of the principles underlying the three types of TVDs is provided below.

1) Voltage Sag Under Sending-end AC Fault

Sending-end AC faults typically manifest as variations in the Thévenin equivalent parameters (TEPs). For example, a short-circuit fault alters both E_{sr} and Z_r , thereby modifying the system equations and reshaping the P_{dr} - Q_{dr} - U_{pr} surface. As illustrated in Fig. 2, a reduction in E_{sr} compresses the P_{dr} - Q_{dr} - U_{pr} surface, causing a voltage sag in U_{pr} even at the same operating point (P_{dr} , Q_{dr}). In most cases, both P_{dr} and Q_{dr} decrease following grid faults, which helps alleviate the voltage drop in U_{pr} . However, as noted in [32], sending-end faults may also induce CF at the inverter station, resulting in more complex and severe voltage disturbances.

2) Overvoltages Caused by Reactive Power Surplus

This type of disturbance arises from a mismatch between reactive power consumption and compensation. A typical scenario is HVDC blocking [3]. During such an event, the active and reactive power consumption at the rectifier station drops rapidly; however, mechanically switched RPCs cannot be disconnected immediately. Consequently, excess reactive power is injected into the AC grid, leading to voltage swell. HVDC blocking generally does not affect the system voltage model, as it is typically triggered by DC-side faults or inverter-side issues.

3) CF-induced Complex TVD

Receiving-end AC faults occurring hundreds of miles away can also lead to sending-end TVDs by triggering CFs in LCC-HVDC systems. Unlike sending-end faults, these disturbances do not alter the sending-end TEPs or the voltage model; instead, they change the operating point on the P_{dr} - Q_{dr} - U_{pr} surface. Consequently, U_{pr} exhibits a “first decrease and then increase” pattern [5].

This phenomenon is primarily attributed to variations in Q_{dr} . Initially, CF causes a rapid increase in DC current, leading to a rise in Q_{dr} and a transient voltage drop. Subsequently, as HVDC control reduces the DC current, Q_{dr} decreases, and surplus reactive power from RPCs is injected into the AC grid, resulting in transient overvoltage. When successive CFs occur, this process repeats, creating a series of “first decrease and then increase” patterns. Compared with single voltage sag or swell, such “continuous” TVDs pose a more severe threat to the safe operation of WTGs [6].

Accordingly, TVDs can be categorized as either TEP-related or power-imbalance-related, depending on whether the grid equivalent parameters are altered. Despite their diverse mechanisms, the above analyses reveal that changes in P_{dr} and Q_{dr} significantly influence the PCC voltage. This indi-

icates that LCC-HVDC systems have inherent potential to provide voltage support by proactively regulating P_{dr} and Q_{dr} .

III. FORMULATION OF DVS PROBLEM AND PROPOSED STRATEGY

This section investigates the physical nature of voltage support from LCC-HVDC systems, formulates the voltage support problem as an optimization model, and proposes a practical strategy to approach the optimum.

A. Physical Nature of Voltage Support from LCC-HVDC Systems

Although converter stations are typically considered as loads, the presence of RPCs (B_c) enables LCC-HVDC systems to not only absorb excessive reactive power during voltage swells but also provide substantial reactive power support during voltage sags. The physical nature of this voltage support can be understood by analyzing the sensitivities of U_{pr} with respect to P_{dr} and Q_{dr} . While deriving an explicit expression for $U_{pr}(P_{dr}, Q_{dr})$ is challenging, sensitivity analysis can be conducted using implicit function theory.

Assuming $\partial F/\partial U_{pr} \neq 0$, the sensitivities of U_{pr} with respect to P_{dr} and Q_{dr} are given by:

$$\frac{\partial U_{pr}}{\partial P_{dr}} = -\frac{\partial F/\partial P_{dr}}{\partial F/\partial U_{pr}} \quad (9)$$

$$\frac{\partial U_{pr}}{\partial Q_{dr}} = -\frac{\partial F/\partial Q_{dr}}{\partial F/\partial U_{pr}} \quad (10)$$

where the partial derivatives of the implicit function (7) with respect to U_{pr} , P_{dr} , and Q_{dr} are detailed in Supplementary Material A.

These sensitivities not only quantify the impact of P_{dr} and Q_{dr} on voltage but also serve as critical metrics for voltage stability analysis. For instance, the condition $\partial F/\partial U_{pr} = 0$, which leads to infinite sensitivities, corresponds to the saddle-node bifurcation – a voltage instability phenomenon [31].

Given the diverse mechanisms underlying different types of TVDs, the impacts of grid parameter variations and operating point changes on PCC voltage are analyzed separately. The parameters used in the numerical calculations are consistent with those described in Section II-B.

1) TEP-related TVDs

Such TVDs are induced by changes in the equivalent parameters of the sending-end system. For example, the loss of remote generators results in a dip in E_{sr} , while short-circuit AC faults can alter both E_{sr} and Z_r .

As illustrated in Fig. 2, decreasing P_{dr} and Q_{dr} can improve U_{pr} . To further explore this, the geometry of $(\partial U_{pr}/\partial Q_{dr})/(\partial U_{pr}/\partial P_{dr})$ under varying grid impedance Z_r and impedance ratio (IR) is presented in Fig. 3. The numerical results illustrate that P_{dr} and Q_{dr} influence voltage in the same direction, with the impact of Q_{dr} being more pronounced as the grid impedance and IR increase. Consequently, since $X_r \gg R_r$ in high-voltage transmission grids, subsequent analyses focus on the impact of Q_{dr} on U_{pr} .

Fixing (P_{dr}, Q_{dr}) at the rated point (1.0 p.u., 0.626 p.u.), the sensitivity $\partial U_{pr}/\partial Q_{dr}$ under varying E_{sr} and Z_r is shown

in Fig. 4. Results indicate that $\partial U_{pr}/\partial Q_{dr}$ decreases with the increase of E_{sr} , highlighting that voltage support is more significant during low-voltage conditions than during high-voltage disturbances. Additionally, $\partial U_{pr}/\partial Q_{dr}$ increases with Z_r , suggesting that voltage support is more pronounced in weak AC systems with high equivalent impedance. When E_{sr} and $1/Z_r$ decrease to critical levels, sensitivity approaches negative infinity, indicating voltage instability.

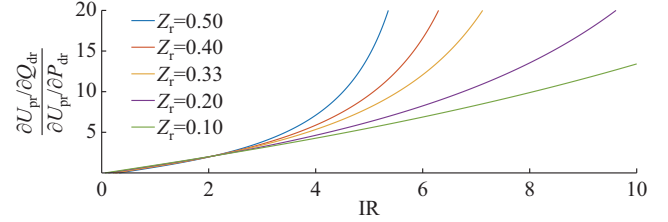


Fig. 3. $(\partial U_{pr}/\partial Q_{dr})/(\partial U_{pr}/\partial P_{dr})$ under varying Z_r and IR.

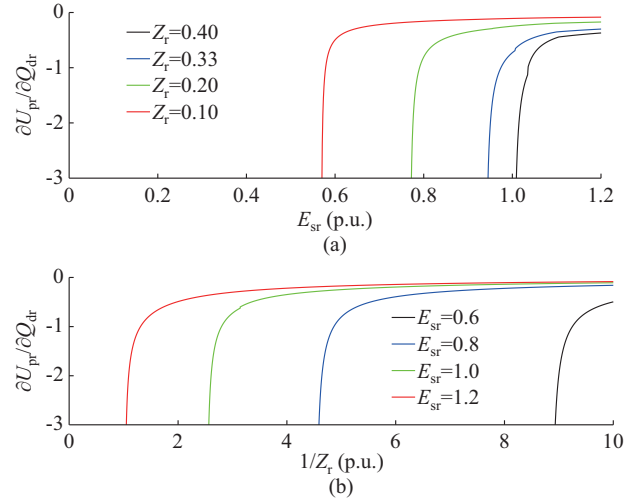


Fig. 4. $\partial U_{pr}/\partial Q_{dr}$ under varying E_{sr} and Z_r . (a) Under varying E_{sr} . (b) Under varying Z_r .

2) Power-imbalance-related TVDs

For TVDs caused by variations in P_{dr} or Q_{dr} , Fig. 5 illustrates $\partial U_{pr}/\partial Q_{dr}$ and U_{pr} with different Q_{dr} under fixed grid parameters ($Z_r = 0.4$ p.u. and $IR = 10$).

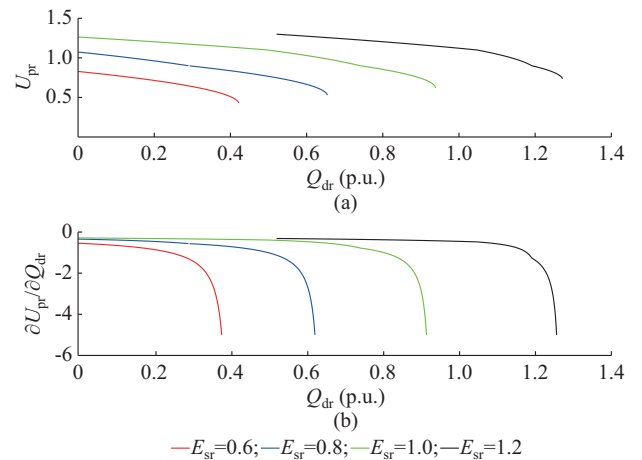


Fig. 5. $\partial U_{pr}/\partial Q_{dr}$ and U_{pr} with different Q_{dr} .

The results indicate that the increase in Q_{dr} leads to a reduction in the voltage and an increase in the sensitivity, demonstrating that larger Q_{dr} (corresponding to lower voltage) leads to greater sensitivity. Consequently, LCC-HVDC systems exhibit higher DVS potential at lower voltage levels. However, continuously increasing Q_{dr} can lead to voltage instability, and smaller equivalent voltage diminishes the voltage stability margin.

Beyond these specific observations, Figs. 4 and 5 reveal a critical finding: within the voltage stability boundary, $\partial U_{pr}/\partial Q_{dr}$ consistently remains negative, regardless of grid parameters or operating points. This characteristic forms the basis for designing the subsequent control strategy.

B. Optimal DVS from LCC-HVDC Systems

The problem of maximizing the DVS capability of LCC-HVDC systems can be formulated as the optimization model (11). The objective function (11a) aims to regulate U_{pr} toward 1.0 p.u., that is, to raise the voltage under low-voltage conditions and suppress it under overvoltage conditions. Constraint (11b) represents the voltage stability limit; (11c) and (11d) are the minimum and maximum DC current limits, respectively; (11e) is the CF constraint; and (11f) and (11g) are the inverter-side AC voltage limits.

$$\min_{P_{dr}, Q_{dr}} |U_{pr}(P_{dr}, Q_{dr}) - U_{prN}| \quad (11a)$$

s.t.

$$S(P_{dr}, Q_{dr}) \geq 0 \quad (11b)$$

$$I_{dc}(P_{dr}, Q_{dr}) \geq I_{dc, \min} \quad (11c)$$

$$I_{dc}(P_{dr}, Q_{dr}) \leq I_{dc, \max} \quad (11d)$$

$$I_{dc}(P_{dr}, Q_{dr}) \leq I_{CF} \quad (11e)$$

$$U_{pi}(P_{dr}, Q_{dr}) \geq U_{pi, \min} \quad (11f)$$

$$U_{pi}(P_{dr}, Q_{dr}) \leq U_{pi, \max} \quad (11g)$$

where U_{prN} is the rated PCC voltage; $S(\cdot)$ is the static voltage stability condition; I_{dc} is the DC current; I_{CF} is the critical DC current for avoiding CF; $I_{dc, \min}$ and $I_{dc, \max}$ are the minimum and maximum DC currents, respectively; and U_{pi} , $U_{pi, \min}$, and $U_{pi, \max}$ are the measured, minimum, and maximum inverter-side AC voltages, respectively.

In theory, solving this optimization model to determine the optimal (P_{dr}^*, Q_{dr}^*) as reference values and controlling the LCC-HVDC system accordingly should achieve optimal DVS. However, the unique characteristics of LCC-HVDC systems and uncertainties introduced by WFs make this task very challenging due to the following reasons.

1) Challenge 1: Modeling

As discussed before, the explicit expression of $U_{pr}(P_{dr}, Q_{dr})$ is complex and significantly influenced by WFs. In the fault ride-through state, the equivalent parameters of WFs are voltage-dependent due to control mode switching, causing the optimization model to evolve dynamically with changes in U_{pr} . Moreover, obtaining accurate equivalent parameters of WFs in the fault ride-through state is extremely challenging in practice.

2) Challenge 2: Solution

Even with an accurate model, solving the optimal (P_{dr}^*, Q_{dr}^*) is nontrivial due to the nonlinear and time-varying constraints of the optimization model. For example, the relationships among I_{dc} , P_{dr} , and Q_{dr} are described by (12) and (13). While these equations define $I_{dc}(P_{dr}, Q_{dr})$ as a nonlinear function, I_{dc} is further affected by U_{pr} and α . During faults, rapid variations in U_{pr} and α over time make the feasible solution space difficult to determine analytically.

$$P_{dr} = \left(\frac{3\sqrt{2}}{\pi} NT_r U_{pr} \cos(\alpha) - \frac{3}{\pi} X_{cr} NI_{dc} \right) I_{dc} \quad (12)$$

$$Q_{dr} = I_{dc} \left(\frac{18}{\pi^2} N^2 T_r^2 U_{pr}^2 \sin(\alpha^2) - \frac{9}{\pi^2} N^2 X_{cr}^2 I_{dc}^2 + \frac{18\sqrt{2}}{\pi^2} N^2 T_r U_{pr} \cos(\alpha) X_{cr} I_{dc} \right)^{\frac{1}{2}} \quad (13)$$

where U_{pr} , I_{dc} , and firing angle α are the key variables; and N , T_r , and X_{cr} are the constant parameters with definitions available in [33].

3) Challenge 3: Implementation

Unlike voltage source converters (VSCs), (P_{dr}, Q_{dr}) of the rectifier station cannot be arbitrarily adjusted. The operation of LCC-HVDC converters relies on thyristors, which have a single control variable α . The firing angle α can be indirectly controlled by adjusting quantities such as the DC current I_{dc} in constant current (CC) mode or the extinction angle γ in constant extinction angle (CEA) mode, or it can be directly set in min- α mode. Consequently, P_{dr} and Q_{dr} within a single station are inherently tightly coupled. Furthermore, achieving desired P_{dr} and Q_{dr} requires coordination with the inverter station.

For instance, in CC mode, which is the most common case for the rectifier, P_{dr} and Q_{dr} can be altered by adjusting I_{dc} . While the CC controller can track the reference current well, α is not solely determined by the rectifier but is also influenced by the inverter station through the relationship (14).

$$\alpha = \arccos \left(\frac{U_{pi} T_i}{U_{pr} T_r} \cos(\gamma) + \frac{I_d (\pi R_d + 3X_{cr} - 3X_{ci})}{3\sqrt{2} U_{pr} T_r} \right) \quad (14)$$

where T_i , X_{ci} , and R_d are the constants whose definitions are available in [33].

As a result, the rectifier-side control alone cannot accurately achieve the desired (P_{dr}^*, Q_{dr}^*) . In theory, it is possible to obtain a combination of I_{dc} and γ to realize the optimum, by solving (12)-(14) and coordinating the converter stations at two ends. However, in practice, this is challenging during transient conditions due to signal latencies in measurement and communication between the rectifier and inverter stations.

C. Optimality Analysis and Two-stage Optimal DVS Control

Although directly solving the model of the proposed strategy (11) is challenging, analyzing its geometric properties can provide valuable insights to address these challenges and in-

spire the design of a practical and implementable control strategy.

The shaded area in Fig. 6 represents the controllable range of the rectifier station, constrained by DC current (solid blue lines, corresponding to $I_{dc}=0.2, 0.8, 1.0,$ and 1.2 p.u. from left to right) and firing angle (solid green lines, with the upper and lower lines representing the maximum and minimum values, respectively). The contours of U_{pr} during a voltage sag (in this case, $E_{sr}=0.9$ p.u., $Z_r=0.4$ p.u., $IR=10$), specifically the upper half above the stability boundary, are shown as colored gradient lines. For a given U_{pr} , the trajectory forms a circular arc. The highlighted trajectory corresponding to $U_{pr}=1.0$ p.u., which minimizes the objective function (11a), is defined as the optimal trajectory.

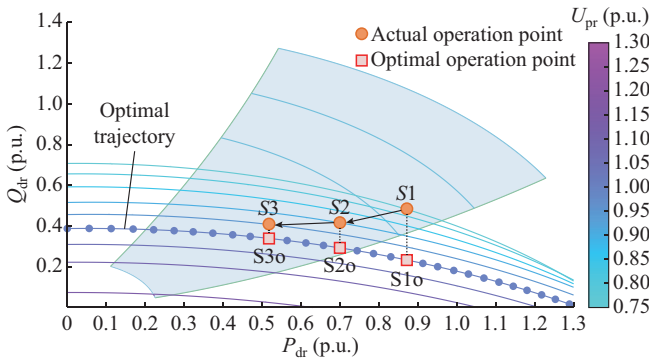


Fig. 6. Illustration of proposed strategy.

Figure 6 illustrates a specific fault case, but in practice, the geometries may vary significantly due to different faults and system parameters. For example, voltage sags and swells can cause overall downward and upward shifts in the U_{pr} trajectories. Nevertheless, several key properties inferred from the established model and sensitivity analysis remain consistent:

- 1) For a constant $U_{pr}(P_{dr}, Q_{dr})$ solution, the trajectory is a circular arc, with its center and radius dependent on the equivalent grid and WF parameters, as well as U_{pr} .
- 2) Before reaching the stability boundary, U_{pr} descends from bottom left to top right for a family of contours.
- 3) A reduction in I_{dc} leads to an increase in U_{pr} ; however, the same I_{dc} may correspond to different U_{pr} , depending on the firing angle.

These properties allow us to classify fault cases into three scenarios based on the intersection of the optimal trajectory and the controllable range.

- 1) Scenario 1: trajectory intersects with controllable range.

In this scenario, U_{pr} can be controlled to 1.0 p.u., with multiple available (P_{dr}^*, Q_{dr}^*) combinations corresponding to different I_{dc}^* values while achieving optimality. This scenario typically corresponds to mild voltage sags or swells.

- 2) Scenario 2: optimal trajectory is below the controllable range.

For severe voltage sags, U_{pr} cannot be raised to 1.0 p.u. even if P_{dr} and Q_{dr} are minimized. In this scenario, the single optimal (P_{dr}^*, Q_{dr}^*) exists on the trajectory $I_{dc}=I_{dc,min}$, with

its exact position influenced by the system IR and equivalent fault ride-through parameters of WFs.

- 3) Scenario 3: optimal trajectory is above the controllable range.

Similarly, under severe voltage swells, U_{pr} cannot be suppressed to 1.0 p.u.. The unique point minimizing U_{pr} lies on the trajectory $I_{dc}=I_{dc,max}$ and is also influenced by the system IR and equivalent fault ride-through parameters of WFs.

To address the challenges identified earlier, a practical two-stage strategy is proposed to iteratively approach the optimal DVS, leveraging insights from the geometric properties and the operational characteristics of LCC-HVDC systems.

Firstly, rather than solving for the optimal (P_{dr}^*, Q_{dr}^*) , the proposed strategy focuses on finding the optimal reference DC current I_{dc}^* to achieve DVS. Considering that the rectifier station primarily operates in CC mode, the proposed strategy addresses the intrinsic coupling between P_{dr} and Q_{dr} .

Then, the difficulty of accurately modeling WFs during fault ride-through state is mitigated through a compromise. When calculating the optimal trajectory, only the equivalent WF model within the normal operating voltage range ($0.9 \text{ p.u.} \leq U_{pr} \leq 1.1 \text{ p.u.}$) is required, as $U_{pr}=1.0$ p.u.. These parameters are practically obtainable. Therefore, for scenario 1, a suitable I_{dc}^* ensuring optimality can be analytically determined based on the measured firing angle. In cases of severe voltage sags or swells, determining the optimal point is hindered. However, considering the half-controlled nature of rectifier stations, which can only regulate the DC current, achieving the theoretical optimum is inherently unattainable. Therefore, instead of pursuing an unachievable theoretical optimum, a practical solution is to directly set I_{dc} to its maximum or minimum limit, focusing on attaining a feasible sub-optimal solution within the capability of the LCC-HVDC system. The need for an accurate equivalent model is thus eliminated.

The nonlinear and time-vary relationship among I_{dc} , P_{dr} , and Q_{dr} leads to challenge 2. To solve it, we propose a two-stage strategy to iteratively approach an optimal solution instead of one-step solving. The principle is illustrated in Fig. 6. Initially, the system operates at point S1. In the first stage of each step, an optimal reactive power command on the optimal trajectory is calculated based on the measured active power. Then in stage 2, a corresponding reference DC current is calculated using the measured α and U_{pr} . Due to the coupling between active and reactive power, the rectifier station cannot directly reach the optimal trajectory, but it gradually approaches the trajectory by moving to point S2, and so on. In scenario 1, the system converges to one of the optimal points. In scenarios 2 and 3, the results correspond to the limits of I_{dc} , achieving sub-optimality. Details of the proposed strategy are as follows.

- 1) Stage 1: calculation of optimal reactive power

In this stage, the reference reactive power $Q_{dr,ref}$ is calculated to maximize U_{pr} if $U_{pr} < 1.0$ p.u. or minimize it otherwise, for a given active power. By setting $U_{pr}=1.0$ p.u. and

neglecting R_r , $Q_{dr,ref}$ is derived as:

$$Q_{dr,ref} = \frac{-X_r + (B_{cr} - K_{Q1} - K_{Q2})X_r^2}{X_r^2} + \frac{\sqrt{E_{sr}^2 X_r^2 - (K_{P1} + K_{P2} - P_{dr})^2 X_r^4}}{X_r^2} \quad (15)$$

The critical reactive power $Q_{critical}$, which ensures voltage stability, is obtained by solving $\partial F / \partial U_{pr} = 0$. The smaller one between $Q_{dr,ref}$ and $Q_{critical}$ is selected as the reference.

2) Stage 2: calculation of reference DC current

This stage calculates a reference DC current to achieve the desired reactive power. Rearranging (13), the optimal I_{dc} is a solution of the quadratic equation:

$$a_3 I_{dc}^4 + b_3 I_{dc}^3 + c_3 I_{dc}^2 + d_3 I_{dc} + e_3 = 0 \quad (16)$$

where $e_3 = Q_{dr,ref}^2$; and other coefficients a_3 , b_3 , c_3 , and d_3 are the constants given in Supplementary Material A.

The solution is then compared with $I_{dc,min}$, $I_{dc,max}$, and other constraints in (11) to determine the optimal I_{dc} .

The convergence of the proposed strategy is crucial for practical implementation. As elaborated above, U_{pr} decreases monotonically with P_{dr} and Q_{dr} , with a higher sensitivity to Q_{dr} . It thus boils down to justifying the monotonicity of P_{dr} and Q_{dr} with respect to I_{dc} . Figure 7 shows their sensitivities derived using CIGRE benchmark parameters, where the trajectory planes from top to bottom correspond to $U_{pr} = 1.3, 1.1, 1.0, 0.8,$ and 0.6 p.u., respectively.

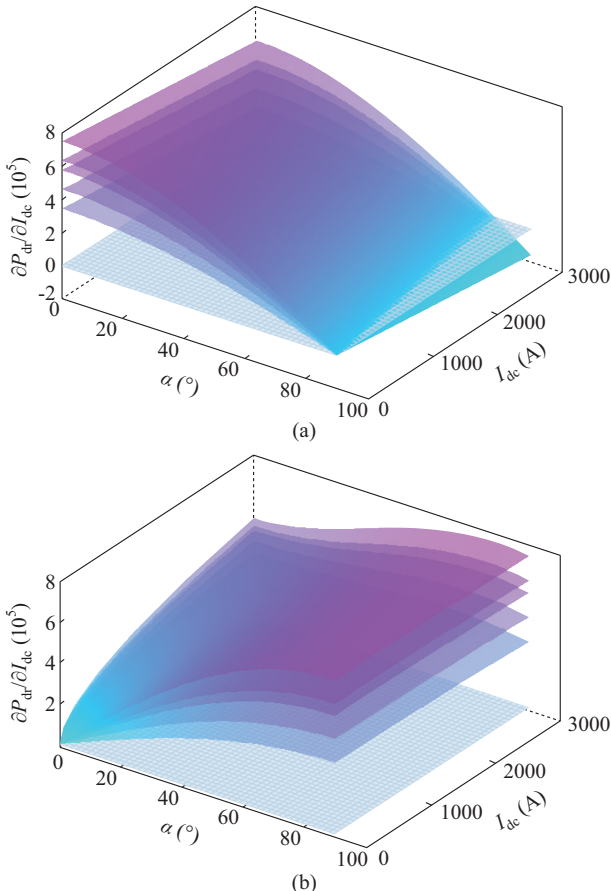


Fig. 7. Trajectories of $\partial P_{dr} / \partial I_{dc}$ and $\partial Q_{dr} / \partial I_{dc}$ under different conditions. (a) Trajectories of $\partial P_{dr} / \partial I_{dc}$. (b) Trajectories of $\partial Q_{dr} / \partial I_{dc}$.

As observed, Q_{dr} increases monotonically with I_{dc} under various operating conditions. $\partial P_{dr} / \partial I_{dc}$ is generally positive, but for a given α , it may be negative as I_{dc} increases. The numerical results show that for the cases of I_{dc} less than 3000 A (1.5 p.u.), negative sensitivity only appears when α is large ($\geq 75^\circ$), which is a rare and transient case such as the early tens of milliseconds of a CF. Therefore, P_{dr} can also be treated as increasing monotonically with I_{dc} in general.

Given this analysis, U_{pr} increases monotonically within $[I_{dc,min}, I_{dc,max}]$, and the direction of change of I_{dc} is always towards the optimal trajectory. Thus, the convergence of the proposed strategy can be guaranteed. Furthermore, this monotonicity allows the proposed strategy to compute I_{dc}^* for scenario 1 and the lower or upper limits for scenarios 2 and 3, without requiring explicit scenario differentiation.

D. Other Operating Constraints

Constraints (11b)-(11d) have been integrated into the proposed strategy on the rectifier side. To address the impact of communication delays, constraints (11e) and (11g), which originate from the inverter side, are handled locally as follows.

1) CF constraint

As validated in [34], limiting I_{dc} effectively decreases the risk of CFs on the inverter side. According to the quasi-static model of LCC-HVDC systems, the following relationship can be derived:

$$I_{dc} = \frac{\cos(\gamma) - \cos(\beta)}{\sqrt{2} X_{ci}} T_i U_{pi} \quad (17)$$

where β is the leading firing angle.

Based on (17), the maximum DC current I_{CF} that avoids CF can be determined using preset values for the minimum extinction angle γ_{min} for commutation and the maximum leading firing angle β_{max} . For instance, in [34], I_{CF} is calculated with $\gamma_{min} = 10^\circ$ and $\beta_{max} = 38^\circ$. However, this approach can be conservative; in some cases, CF may not occur even if I_{dc} exceeds the I_{CF} . This is because a slight increase in β_{max} can lead to a significant rise in I_{CF} . Thus, rather than strictly enforcing the CF constraint on I_{dc} , a more flexible approach is adopted. The inverter dynamically adjusts β based on local measurements to mitigate the risk of CFs.

2) Receiving-end AC voltage constraint

Due to the coupling between the rectifier and inverter stations, adjustments to Q_{dr} at the rectifier station inevitably affect the reactive power Q_{di} at the inverter station, leading to variations in U_{pi} . DVS at the sending end should ensure that U_{pi} remains within the acceptable range $[U_{pi,min}, U_{pi,max}]$.

Similar to (5), the following relationship can be derived for the inverter side:

$$U_{pi} (1 - 2B_{ci} X_i + Z_i^2 B_{ci}^2) - U_{pi}^2 [E_{si}^2 + 2(P_{di} R_i - Q_{di} X_i) + 2Q_{di} B_{ci} Z_i^2] + Z_i^2 (P_{di}^2 + Q_{di}^2) = 0 \quad (18)$$

where B_{ci} is the equivalent susceptance of RPCs within the inverter station; P_{di} is the inverter-side DC active power; and R_i , X_i , Z_i , and E_{si} are the Thévenin equivalent parameters of receiving-end system.

From (18), the feasible range of Q_{di} can be expressed as:

$$Q_{di} = B_{ci} U_{pi}^2 - SCR_{inv} \cdot U_{pi}^2 + \sqrt{-P_{di}^2 + E_{si}^2 \cdot SCR_{inv}^2 \cdot U_{pi}^2} \quad (19)$$

where $SCR_{inv} = 1/Z_i$ is the short-circuit ratio (SCR) on the inverter side.

Given the relatively low penetration of renewable energy sources at the receiving end [35], the receiving-end AC grid is modeled using Thévenin equivalence, and the conventional definition of SCR is adopted.

For $U_{pi,min} = 0.9$ p.u. and $U_{pi,max} = 1.1$ p.u., which represent a secure and conservative short-term operating range commonly adopted in engineering practice, the feasible range of Q_{di} can be calculated, as illustrated in Fig. 8. As can be observed, the feasible region expands with an increase in SCR_{inv} , indicating that the proposed strategy is particularly well-suited for LCC-HVDC systems characterized by a weak sending-end AC system and a strong receiving-end AC system. This configuration aligns with the typical design paradigm for most LCC-HVDC projects in China.

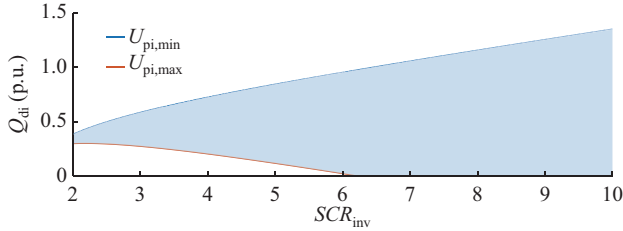


Fig. 8. Feasible region of Q_{di} with constraint of U_{pi} .

Similar to (13), for the inverter side, we can derive:

$$Q_{di} = I_{dc} \left[\frac{18}{\pi^2} N^2 T_i^2 U_{pi}^2 (1 - \cos(\gamma^2)) - \frac{9}{\pi^2} N^2 X_{ci}^2 I_{dc}^2 + \frac{18\sqrt{2}}{\pi^2} N^2 T_i U_{pi} \cos(\gamma) X_{ci} I_{dc} \right]^{\frac{1}{2}} \quad (20)$$

This reveals that adjusting γ can counteract the side effects of changing I_{dc} on U_{pi} . By substituting $U_{pi,max}$, the corresponding $Q_{di,min}$, and measured I_{dc} into (20), an appropriate γ can be calculated to maintain U_{pi} at the upper limit. Similarly, γ can be adjusted to prevent U_{pi} from falling below the lower limit $U_{pi,min}$.

IV. IMPLEMENTATION OF PROPOSED STRATEGY

The implementation of the proposed strategy is detailed in this section. The control logics for the rectifier and inverter are modified to coordinate DVS provision, relying solely on local measurements at each station.

A. Overview

Under normal conditions, the LCC-HVDC system transmits a specified active power and exhibits negligible reactive power exchange with the AC systems on both sides. When a TVD is detected, it switches to provide DVS to the sending-end system.

1) Activation and Deactivation

The optimal DVS mode activates when $|U_{pr} - 1.0| \geq 0.1$ p.u.. The flowchart of the proposed strategy is shown in

Fig. 9.

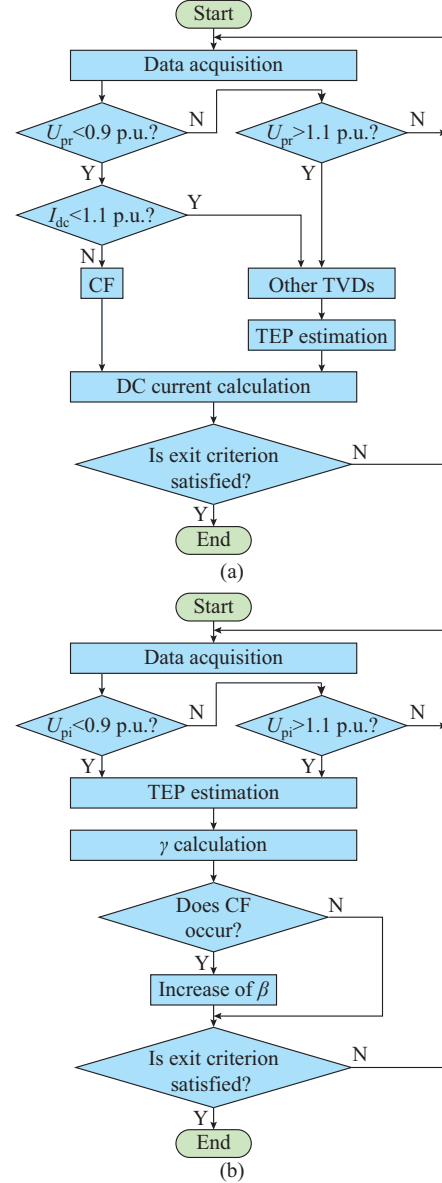


Fig. 9. Flowchart of proposed strategy. (a) Control logic for rectifier. (b) Control logic for inverter.

For TVDs accompanied by sending-end system topology changes, a delay of 3-5 cycles is applied to determine the fault TEPs. For TVDs caused by CF, the pre-fault TEPs can be used directly, with an additional condition based on (21).

$$\begin{cases} U_{pr} \leq 0.9 \text{ p.u.} \\ I_{dc} \geq 1.1 \text{ p.u.} \end{cases} \quad (21)$$

When the system reverts and maintains normal conditions (22) for a predefined duration (e.g., 50 ms), the proposed strategy opts out.

$$\begin{cases} 0.9 \text{ p.u.} \leq U_{pr} \leq 1.1 \text{ p.u.} \\ 0.9 \text{ p.u.} \leq I_{dc} \leq 1.1 \text{ p.u.} \end{cases} \quad (22)$$

2) Parameter Estimation

The proposed strategy relies on grid equivalent parameters obtained from PCC to calculate the reference current. While

the estimation of WF-integrated network equivalents under transient conditions is a complex and evolving area of research, the proposed strategy does not impose strict requirements on the equivalent parameters. For WFs, only parameters within the normal operating voltage range are needed, which are practically obtainable. For TEPs, real-time voltage and current measurements are available within the converter station, and numerous online estimation methods can provide accurate results within tens of milliseconds, as verified by both academic and industrial applications [36]-[38]. Since this study focuses on the proposed DVS strategy, parameter estimation is assumed to be available and is considered outside the scope of this paper.

B. Modified Control

The LCC-HVDC system integrated with the proposed

strategy is illustrated in Fig. 10, where colored parts indicate the modifications introduced by the proposed strategy to the CIGRE benchmark control system; PI stands for proportional-integral; $Ctrl_R$ is the signal to trigger the rectifier DVS control; $Ctrl_{CF}$ is the signal to activate the remedy control for avoiding CF; $Ctrl_I$ is the signal to trigger the inverter coordinated control; I_{DVS} is the optimal DC current command; I_{VDCOL} is the output of the voltage-dependent current order limiter (VDCOL); $I_{d,order}$ is the reference order from upper control layer; $\gamma_{i\Delta}$ and γ_{iY} are the measured extinction angles of the inverter-side delta-connected valve and star-connected valve, respectively; and γ_{ref0} is the original reference extinction angle. The system operates based on local measurements and activates the DVS function when $Ctrl_R$ switches from 0 to 1 upon detecting a TVD.

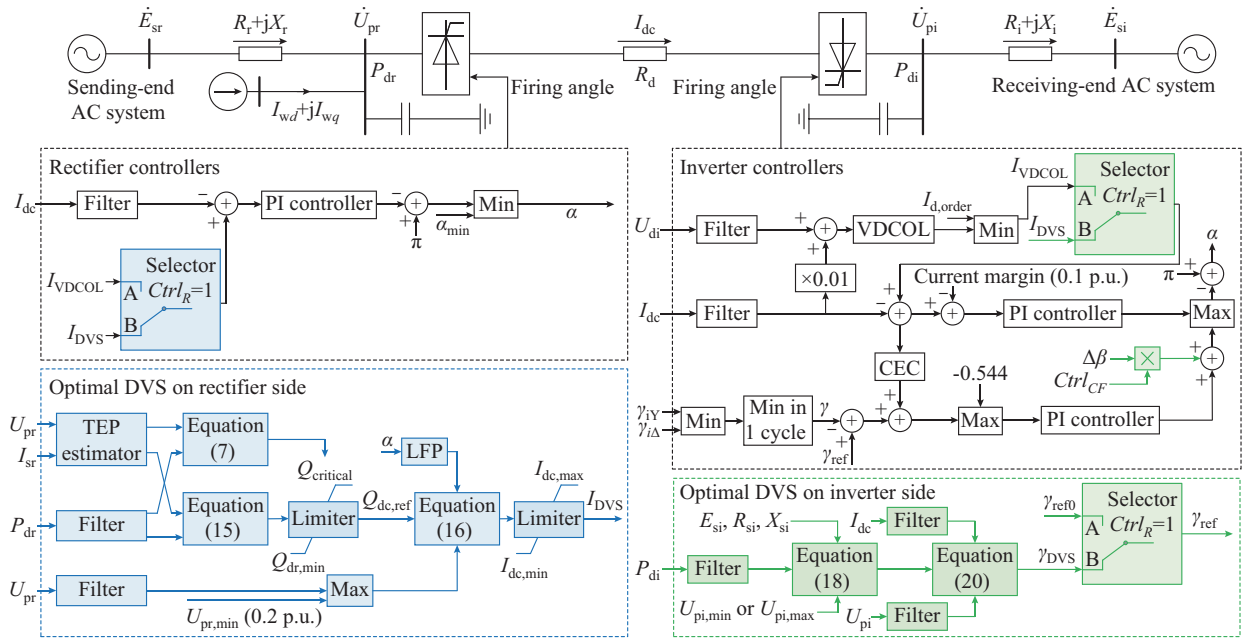


Fig. 10. LCC-HVDC system integrated with proposed strategy.

1) Rectifier Control

As shown in Fig. 9(a) and the left half of Fig. 10, the proposed strategy modifies only the reference DC current. In stage 1, the optimal reactive power is calculated using (15), with the upper limit of $Q_{dr,ref}$ set to be $Q_{critical}$, defined by the voltage stability boundary, and the lower limit constrained to zero. In stage 2, the corresponding reference DC current is computed using (16) to achieve the desired $Q_{dr,ref}$. This value is then evaluated against the constraints (11c) and (11d) to determine I_{DVS} . The final reference current for the CC controllers on two sides is determined by comparing I_{DVS} with I_{VDCOL} . The logic is as follows: when $Ctrl_R = 1$, the output of the selector is shown in (23); otherwise, the output of the selector is $I_{out} = I_{VDCOL}$.

$$I_{out} = \begin{cases} \max(I_{VDCOL}, I_{DVS}) & U_{pr} > U_{prN} \\ \min(I_{VDCOL}, I_{DVS}) & \text{otherwise} \end{cases} \quad (23)$$

2) Inverter Control

The inverter control fulfills two primary functions to coordinate

with the rectifier: maintaining U_{pi} within a safe range and preventing CF, achieved by adjusting the extinction angle and leading firing angle, as depicted in Fig. 9(b) and the right half of Fig. 10. To mitigate potential adverse effects caused by DC current mismatch, the optimal reference current computed on the rectifier side is transmitted to the inverter. When U_{pi} deviates from the safe range of [0.9, 1.1] p.u., the signal $Ctrl_I$ is triggered (set to be 1), and a new reference extinction angle γ_{DVS} is calculated using (19) and (20) to restore U_{pi} within acceptable limits. This updated γ replaces γ_{ref0} , which is 0.2618 (15°) in this paper. The logic is as follows: when $Ctrl_I = 1$, the output of the selector is shown in (24); otherwise, the output of the selector is $\gamma_{out} = \gamma_{ref0}$.

$$\gamma_{out} = \begin{cases} \max(\gamma_{ref0}, \gamma_{DVS}) & U_{pi} > U_{piN} \\ \min(\gamma_{ref0}, \gamma_{DVS}) & \text{otherwise} \end{cases} \quad (24)$$

Additionally, upon detection of the first CF event, the signal $Ctrl_{CF}$ switches from 0 to 1, and an extra term ($\Delta\beta =$

0.1745) is added to increase β , thereby reducing the risk of subsequent CFs. The deactivation logic of the inverter controller is similar to that described in (22) and is thus omitted here.

V. SIMULATION RESULTS

A WF-integrated LCC-HVDC sending-end system, as shown in Fig. 10, is established in PSCAD/EMTDC to test the proposed strategy. The 1000 MW LCC-HVDC system is modeled based on the CIGRE HVDC benchmark, and the 300 MW permanent magnet synchronous generator (PMSG) based WF is represented by an aggregated single machine.

Detailed system parameters are provided in Supplementary Material B. The simulation results for three typical fault cases are compared against the conventional VDCOL strategy, the closed-loop reactive power control (CLRPC) strategy from [24], and the new recovery strategy (NRS) from [21].

A. Case 1: Voltage Sag Caused by Sending-end AC Fault

A short-circuit fault with a fault inductance of 0.4 H is applied to the sending-end AC bus at $t=5.0$ s and is cleared at $t=5.5$ s. Simulation results are shown in Fig. 11(a), where the grey dashed line (corresponds to $\gamma=5^\circ$) is used to identify the occurrence of CF.

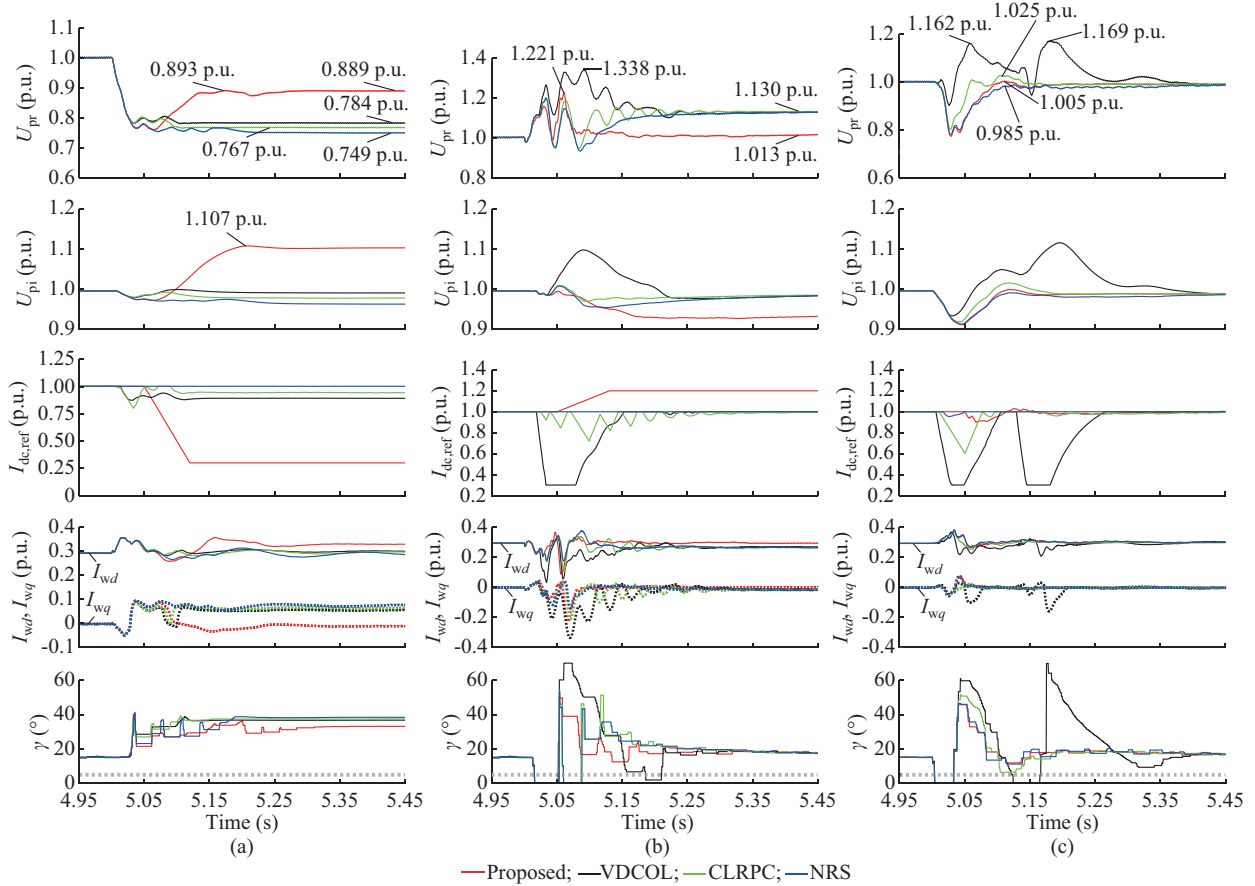


Fig. 11. Simulation results under different cases. (a) Case 1. (b) Case 2. (c) Case 3.

With the conventional VDCOL strategy, U_{pr} falls to 0.784 p.u., indicating this strategy fails to provide voltage support. The CLRPC strategy, designed to maintain zero reactive power exchange at the sending end, similarly maintains U_{pr} at 0.767 p.u.. The NRS, focusing on maintaining zero reactive power exchange at the receiving end, results in an even lower U_{pr} of 0.749 p.u.. In contrast, the proposed strategy reduces I_{dc} to its lower limit, raising U_{pr} to 0.893 p.u., demonstrating significant superiority in voltage support.

However, the improvement in DVS at the sending end negatively impacts the performance at the receiving end, as previously discussed. Once U_{pi} exceeds 1.1 p.u., the inverter control with the proposed strategy increases γ to enforce U_{pi} at the predefined upper limit, thereby confirming the accuracy of the proposed strategy. This adjustment slightly weak-

ens the DVS at the sending end, resulting in a reduction of U_{pr} to 0.889 p.u., even though I_{dc} remains unchanged. These results validate the optimality analysis and highlight the effectiveness of the proposed strategy on the inverter side.

Additionally, it should be noted that due to the inherent operational principle of the LCC-HVDC system, the voltage support performance decreases as the severity of the voltage sag increases. This is because the LCC-HVDC system provides reactive power support primarily by reducing the reactive power consumption of the converter, allowing the reactive power supplied by RPCs to exceed the consumption of the converter. However, for commonly used mechanically switched RPCs, since $Q_{cr} = B_c U_{pr}^2$, the reactive power supplied decreases as the voltage drops. Nevertheless, compared with conventional VDCOL strategy, the proposed strategy

consistently provides superior voltage support.

B. Case 2: Voltage Swell Caused by Reactive Power Surplus

For a sending-end system with multiple export HVDC links, the blocking of one link can lead to an increase in AC voltage on the rectifier side of the other links. This effect can be emulated by inserting a capacitor [22]. In this case, a reactive power surplus is simulated by connecting a $10 \mu\text{F}$ (373.93 Mvar) capacitor to the sending-end AC bus at $t=5.0$ s for a duration of 0.5 s. The corresponding simulation results are presented in Fig. 11(b).

During the fault, the VDCOL strategy, CLRPC strategy, and NRS fail to provide voltage support, resulting in the voltage U_{pr} of 1.130 p.u. during the steady-state fault. In contrast, the proposed strategy suppresses U_{pr} to 1.013 p.u., by increasing I_{dc} to the upper limit of 1.2 p.u.. While exhibiting a decline, U_{pr} remains above the lower limit of 0.9 p.u..

The transient stage during the first 100 ms exhibits drastic changes. A sudden rise in U_{pr} causes CFs in all strategies, superimposing “first decrease and then increase” TVDs on the overvoltage. With the VDCOL strategy, the peak overvoltage reaches 1.338 p.u. with two subsequent CFs being observed. The CLRPC strategy and NRS reduce this peak value but trigger one subsequent CF. The proposed strategy reduces the overvoltage to 1.221 p.u. and avoids subsequent CFs.

C. Case 3: CF-induced TVD

CFs induced by receiving-end AC faults are simulated, and the results are depicted in Fig. 11(c). When the VDCOL strategy is applied, U_{pr} initially drops before rising to 1.162 p.u., and during the second CF, it further increases to 1.169 p.u.. The CLRPC strategy and NRS, designed to improve the performance of LCC-HVDC systems under CFs, suppress subsequent CFs and stabilize U_{pr} at 1.025 p.u. and 0.985 p.u., respectively. The proposed strategy achieves the best performance, maintaining U_{pr} at 1.005 p.u., while ensuring that no overvoltage occurs at the receiving end.

D. Impact of Communication Delays

The proposed strategy relies solely on local measurements, making it independent of communication systems. However, in practice, LCC-HVDC systems share a reference current between converter stations, introducing communication delays. In this study, the reference current is derived from the rectifier control with the proposed strategy, with delays modeled as tens of milliseconds, which are typical for dedicated fiber-optic channels.

As shown in Fig. 12, communication delays postpone the effectiveness of the proposed strategy, slightly affecting the timing of its voltage support response. This results in a marginal reduction in the minimum voltage (0.01 p.u.). However, the delay does not impact voltage support during the steady-state fault. The most prominent consequence of the delay is the potential for overvoltage. This occurs because, after the rectifier-side voltage has been supported to 1.0 p.u., the inverter side continues executing the reference DC current set for the prior low-voltage stage. This mechanism is similar to the overvoltage caused by control delays of RESs discussed in [28].

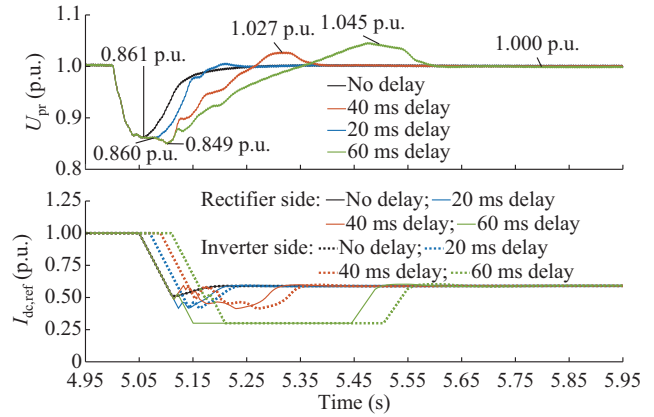


Fig. 12. Simulation results with different communication delays under 0.8 H sending-end short-circuit faults (fault durations are extended to 1 s).

Nonetheless, this effect is only observed in mild grid faults and for signal delays exceeding 20 ms. Even with delays of up to 60 ms, the overvoltage remains below 1.05 p.u., which is considered acceptable.

E. Robustness Against Equivalent Parameter Estimation Errors

Robustness to equivalent parameter estimation errors is crucial in practical applications. Under severe TVDs, where I_{dc} reaches its limits, parameter errors have a negligible impact on the voltage support performance. However, for mild TVDs, as shown in Fig. 13, parameter accuracy directly influences the computed reference DC current $I_{dc,ref}$.

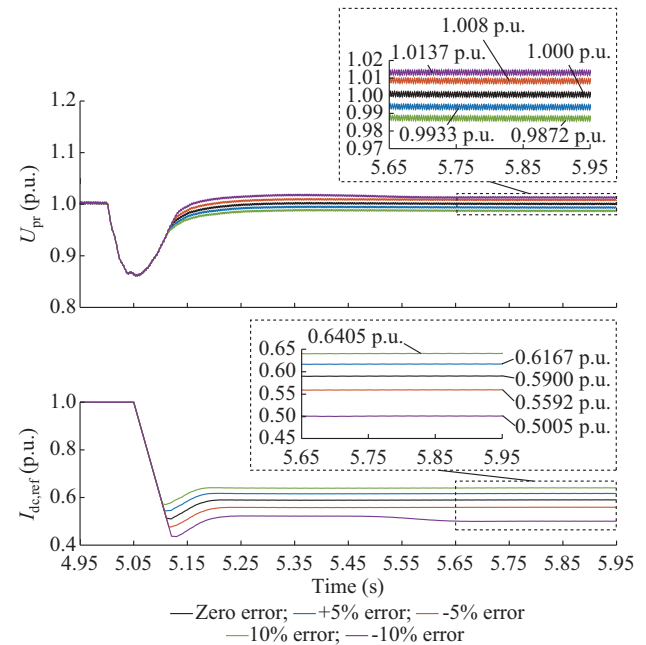


Fig. 13. Simulation results with different TEP estimation errors under 0.8 H sending-end short circuit faults (fault durations are extended to 1 s).

A positive (or negative) error in estimated parameters increases (or decreases) the $I_{dc,ref}$, leading to lower (or higher) U_{pr} . For a parameter estimation error of +10% or -10%, the corresponding deviation in U_{pr} is -1.28% or 1.37%, respectively. Given that existing TEP estimation methods ensure er-

rors remain below $\pm 10\%$, the proposed strategy demonstrates strong robustness against parameter uncertainties.

VI. CONCLUSION

This paper demonstrates that LCC-HVDC systems connected to strong receiving-end grids have significant potential to provide DVS to weak sending-end systems under TVD. An optimization model is developed to maximize the DVS capability, unlocking such potential. However, due to inherent challenges in modeling, solving, and implementation, directly achieving the optimal solution from the original model is nontrivial.

To overcome these challenges, optimality analysis is conducted using intuitive geometric illustrations, and a practical two-stage optimal DVS control strategy is proposed to iteratively approach the optimal solution under various conditions. The proposed strategy focuses on determining a suitable reference DC current, achieving optimal performance under mild TVDs and sub-optimality under severe TVDs. Security constraints are handled through coordinated local controls of the rectifier and inverter.

Dynamic simulations validate the effectiveness and superiority of the proposed strategy in enhancing system performance and highlight its robustness against communication delays and equivalent parameter estimation errors. The proposed strategy offers a promising solution to enhance voltage stability under TVDs and release the restricted transmission capacity of LCC-HVDC systems.

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