Fault Isolation and Arc Suppression for Single-line-to-ground Faults in Transformer-less SOP-based Flexible Interconnected Distribution Networks

Ruidong Xu, Zhongxue Chang, Guobing Song, Ke Jia, and Jiayi Yang

Abstract—**The transformer-less configuration is regarded as a preferred solution for soft-open-point (SOP)-based flexible interconnected distribution networks (FIDNs). This study proposes a reliable and cost-effective method for handling single-line-to-ground (SLG) faults in transformer-less SOP-based FIDNs. Firstly, the zero-sequence fault equivalent circuit of FIDNs is established, and the fault propagation characteristics between the grids interconnected by the SOP are analyzed. Secondly, a zero-sequence current isolation strategy based on proportional-resonant control is proposed to prevent fault propagation toward the healthy-side grid. An active injection-based grounding parameter identification (GPI) approach is then proposed, enabling accurate calculation of the compensation current for arc suppression. Finally, the selection of injected signal parameters is discussed, and the complete timing flow of the SLG fault handling method is presented. A 10 kV SOP-based FIDN model configured with a transformer-less topology is developed in PSCAD/EMTDC. The performance of the SLG fault handling method is verified under transition resistances ranging from 10 Ω to 10 kΩ. The results reveal that the average relative error in GPI is less than 4%. Furthermore, the compensated currents of faulty branch remain below 10 A across various fault conditions.**

Index Terms—**Distribution network, soft open point (SOP), single-line-to-ground (SLG) fault, fault isolation, zero-sequence current, grounding parameter identification, arc suppression.**

I. Introduction

THE growing demand for electricity, increasing integration of a high proportion of distributed generations into power grids, and variability of power flow have posed unprecedented challenges to traditional medium-voltage distribution networks [1], [2]. Soft-open-point (SOP)-based flexible interconnection technology is emerging as a promising solution to address these challenges, offering precise power control ability, fault ride-through capability, multi-port interfacing, and other advanced features [3]-[5]. Both theoretical research and engineering practice have demonstrated that flexible interconnected distribution networks (FIDNs) utilizing hybrid modular multilevel converters (MMCs) with a transformer-less configuration provide significant advantages in terms of control performance, construction cost, and space requirements [6], [7]. The FIDN mentioned in this study adopts such a configuration.

Single-line-to-ground (SLG) faults account for approximately 60% to 80% of all the faults in distribution networks [8], making them the most common type of faults. In FIDNs with a transformer-less topology, SLG faults can propagate through the SOP from one grid section to the other, thereby affecting a wider area. Furthermore, transient faults constitute around 50% to 90% of all SLG faults [9], [10] and can often be self-clearing through effective arc suppression strategies. Therefore, it is a critical technical requirement to develop an SLG fault handling method for transformer-less SOP-based FIDNs. This method must ensure both the fault isolation and arc suppression to eliminate transient faults.

In research related to fault isolation under SLG faults, [7] proposed a proportional-integral (PI) based zero-sequence controller to isolate low-frequency (below 1 Hz) zero-sequence currents caused by asymmetry in equipment parameters. However, the effectiveness of this zero-sequence controller significantly declines when isolating power-frequency zero-sequence currents induced by SLG faults. The dynamic behavior of the transformer-less MMC-based high-voltage direct current (MMC-HVDC) system under SLG faults was analyzed in [11], but the propagation characteristics of the zero-sequence current between the grid and MMC were not thoroughly explored. A negative- and zero-sequence current isolation strategy for SOPs was presented in [12], which was designed to isolate unbalanced currents under the normal operating conditions. However, this strategy did not account for the fault ride-through capability during faults, and the system dynamic equations were not derived. Other zero-sequence current isolation strategies were proposed for transformer-less MMC-HVDC systems in [13] and for three-phase voltage source converters (VSCs) in [14]. However, similar to the previous ones, these strategies focused on the

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faulty-side converter for fault isolation rather than utilized the healthy-side converter to isolate the fault. Consequently, under these strategies, the faulty-side converter lacks sufficient control margin to further suppress the fault arc.

Regarding the arc suppression, the conventional strategy typically involves configuring a Peterson coil. However, in FIDNs where operating modes and topologies change over time, it is challenging to select appropriate parameters for the Peterson coil. This often leads to overcompensation and ineffective arc suppression. Current arc suppression strategies can mainly be categorized into voltage-based and current-based ones.

The voltage-based arc suppression strategies extinguish arcs by controlling the faulty-phase voltage to zero. A novel approach proposed in [15] employed a single-phase inverter connected to the grid neutral point to control its voltage, thereby indirectly reducing the faulty-phase voltage and extinguishing the arc. A hybrid arc suppression device (ASD) was proposed in [16] and [17] to reduce the performance requirements of power electronic devices. This device combined a large-capacity ferromagnetic element with a low-capacity power electronic component in a parallel configuration. In [18], an ASD based on back-stepping control and second-order generalized integrator phase-locked loop (BSC-SOGI-PLL) was proposed, which used the neutral voltage of the bus and the faulty-phase voltage to adaptively set the compensation current reference for the ASD. A flexible ASD utilizing a three-phase cascaded H-bridge (CHB) was proposed in [19], which achieved arc suppression by controlling its neutral voltage to match the voltage of faulty branch. However, the voltage-based arc suppression strategies face challenges because of line impedance and load currents, which complicate the suppression of low-resistance (LR) SLG faults, particularly those occurring at the end of feeder. To address this issue, a residual voltage compensation loop was proposed in [20] to counteract the voltage drop across the faulty-phase line impedance.

By contrast, the current-based arc suppression strategies extinguish arcs by injecting inductive compensation current into the neutral point. The performance of these strategies is unaffected by factors such as load current and fault location. However, the reference value of the injected compensation current depends on the accurate grounding parameter identification (GPI) of the grid. A flexible ASD was proposed, which could be installed at the neutral point of transformer [21] or along the line [22], where arc suppression was achieved by injecting compensation current. However, determining the reference value of compensation current required real-time injection of a small current under normal operating conditions, which could interfere with the normal functioning of distribution network. A GPI method proposed in [23] estimated grounding parameters using two injection steps over a duration of up to 4 s. Fluctuations in the injection equipment and measurement errors during this period might lead to errors in parameter identification. Reference [24] proposed a novel topology consisting of three CHBs connected between any two phases of the system and between their shared neutral point and ground. The reference values for the three CHBs were calculated utilizing a double-loop passivity-based controller, enabling effective suppression of both high-resistance (HR) and LR SLG faults.

The implementation of ASD-based arc suppression strategies necessitates the integration of additional flexible grounding devices into the distribution network. These devices often have complex structural designs and entail considerable financial costs. Reference [25] recognized the potential of employing an SOP with a transformer-less topology to handle SLG faults. A cascaded model predictive control strategy for three-phase four-wire converters was proposed to limit and suppress SLG faults. However, this strategy relies on the use of a fourth-line bridge arm, which complicates its implementation in 10 kV medium-voltage distribution networks, where double closed-loop control strategies and three-phase three-wire systems are more commonly employed at this voltage level.

The main contributions of this study are summarized as follows.

1) The propagation characteristics of SLG faults in FIDNs are analyzed. Unlike the conclusions presented in [7] and [11], a unified zero-sequence equivalent circuit that incorporates both the DC-side and AC-side grids under an SLG fault is constructed. This circuit provides a comprehensive basis for analyzing SLG fault characteristics across various configurations.

2) A fault isolation strategy is established based on the dynamic equations derived from the zero-sequence equivalent circuit. This strategy ensures that SLG faults cannot propagate from the faulty side of SOP to the healthy side in transformer-less FIDNs.

3) An SOP-based arc suppression strategy is proposed. In contrast to the flexible grounding approaches, the proposed arc suppression strategy only requires adding capacitors to the DC bus of SOP, thereby eliminating the need for supplementary ASDs. Compared with the conventional voltage-based arc suppression strategies, the proposed arc suppression strategy demonstrates its superior performance in suppressing arcs from LR faults occurring at the terminals of feeders.

II. Basic Configuration and SLG Fault Characteristics of SOP-based FIDNs

A. Topology and Zero-sequence Equivalent Circuit of SOP

A schematic diagram of FIDN with an SLG fault and the topology of an SOP are shown in Fig. 1, where u_k is the voltage of phase k (k=a, b, c) on the AC grid; u_{vk} is the voltage of phase k on the AC valve side; i_k is the current of phase k on the AC valve side; u_{pk} and u_{nk} are the submodule (SM) voltages of the upper- and lower-arm bridges for phase k, respectively; i_{pk} and i_{nk} are the currents of the upper- and lower-arm bridges for phase k, respectively; u_p and u_n are the DC pole-to-ground voltages of the positive and negative poles, respectively; i_{dc} is the DC bus current; R_{ac} and L_{ac} are the equivalent resistance and inductance on the AC side, respectively; R_s and L_s are the equivalent resistance and inductance of arm bridges, respectively; and C_s is the additional

DC capacitance used for arc suppression. In a hybrid MMC, each bridge arm is composed of full-bridge submodules (FBSMs) and half-bridge submodules (HBSMs).

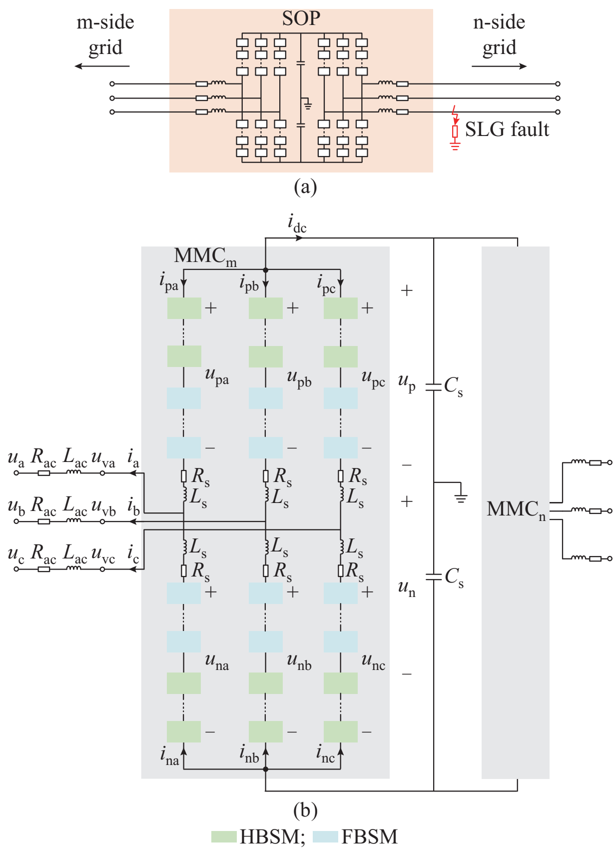

Fig. 1. Schematic diagram of FIND with an SLG fault and topology of SOP. (a) Schematic diagram of FIND with an SLG fault. (b) Topology of SOP.

As shown in Fig. 1(b), the SOP consists of two or more MMCs (e.g., MMC_m and MMC_n) that are connected in a back-to-back configuration on the DC bus. Each MMC can be independently started, blocked, and controlled. These MMCs are equipped with control segments for positive- and negative-sequence separation, including direct control of current, negative-sequence suppression, circulating current suppression control, and phase-locked loop (PLL) function. In terms of outer loop control, the objectives may include AC active power, AC reactive power, or DC bus voltage. Under normal operating conditions, only one MMC employs the U_{dc}-Q control strategy, while the others adopt the P-Q control strategy.

It is noteworthy that, due to the high quality of waveforms output from MMCs, DC capacitors are typically not required on the DC bus in traditional SOP configurations. However, in this study, additional DC bus capacitors are introduced to provide a grounding path under SLG faults. The maximum current flowing through these capacitors is the compensation current. Consequently, their rated capacity is minimal and does not lead to a significant increase in construction costs.

The Kirchhoff's voltage law (KVL) equations for the upper- and lower-arm bridges of phase k are expressed as:

$$u_k+R_{ac}i_k+L_{ac}\frac{\mathrm{d}i_k}{\mathrm{d}t}+R_s i_{pk}+L_s\frac{\mathrm{d}i_{pk}}{\mathrm{d}t}+u_{pk}-u_p=0 \tag{1}$$

$$u_k+R_{ac}i_k+L_{ac}\frac{\mathrm{d}i_k}{\mathrm{d}t}+R_s i_{nk}+L_s\frac{\mathrm{d}i_{nk}}{\mathrm{d}t}-u_{nk}+u_n=0 \tag{2}$$

Adding (1) and (2) and then dividing the result by 2, we can obtain:

$$u_k+R_{eq}i_k+L_{eq}\frac{\mathrm{d}i_k}{\mathrm{d}t}-e_k-u_{com}=0 \tag{3}$$

where R_{eq} and L_{eq} are the equivalent resistance and inductance of the AC side, respectively; e_k is the differential-mode value of the SM capacitor voltages on the upper- and lower-arm bridges of phase k; and u_{com} is the DC-side common-mode voltage. These variables are defined as:

$$R_{eq}=R_{ac}+\frac{R_s}{2} \tag{4}$$

$$L_{eq}=L_{ac}+\frac{L_s}{2} \tag{5}$$

$$e_k=-\frac{u_{pk}-u_{nk}}{2} \tag{6}$$

$$u_{com}=\frac{u_p-u_n}{2} \tag{7}$$

Under the steady-state conditions, (3) can be rewritten as:

$$\dot{U}_k+(R_{eq}+\mathrm{j}\omega L_{eq})\dot{I}_k-\dot{E}_k-\dot{U}_{com}=0 \tag{8}$$

where ω is the angular frequency; and $\dot{U}_k$, $\dot{I}_k$, $\dot{E}_k$, and $\dot{U}_{com}$ are the phase quantities of u_k, i_k, e_k, and u_{com} at the corresponding frequency, respectively.

Applying the symmetrical component transformation to the three-phase system in (8), the zero-sequence component can be obtained as:

$$\dot{U}_0+(R_{eq}+\mathrm{j}\omega L_{eq})\dot{I}_0-\dot{E}_0-\dot{U}_{com}=0 \tag{9}$$

where $\dot{U}_0$ and $\dot{I}_0$ are the zero-sequence voltage and current on the AC grid, respectively; and $\dot{E}_0$ is the zero-sequence differential-mode value of the SM capacitor voltages.

According to (9), the zero-sequence equivalent circuit of SOP is derived and shown in Fig. 2, where the parameters on m-side and n-side of SOP are denoted by subscripts m and n, respectively.

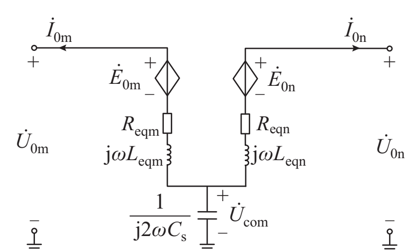

Fig. 2. Zero-sequence equivalent circuit of SOP.

B. Propagation of SLG Faults in SOP-based FIDNs

Taking a phase-a-to-ground (ATG) fault occurring on the n-side grid as an example, the boundary conditions for the faulty branch can be expressed as:

$$\dot{U}_{f0}=\dot{U}_{f(0)}-(Z_{\Sigma1}+Z_{\Sigma2}+3R_f)\dot{I}_{f0} \tag{10}$$

where $\dot{U}_{f(0)}$ is the pre-fault voltage of faulty branch; $\dot{U}_{f0}$ and $\dot{I}_{f0}$ are the zero-sequence voltage and current of faulty branch, respectively; $Z_{\Sigma1}$ and $Z_{\Sigma2}$ are the positive- and negative-sequence equivalent impedances of grid as viewed from the faulty branch, respectively; and R_f is the fault transient resistance.

The zero-sequence fault equivalent circuit of SOP-based FIDNs is shown in Fig. 3, where C_{0m} and C_{0n} are the total grounding capacitances of m-side (healthy-side) and n-side (faulty-side) grids, respectively; L_{gm} and L_{gn} are the inductances of the Peterson coils on m-side and n-side grids, respectively, when the Peterson coil grounding mode is adopted; and R_Σ and L_Σ are the equivalent resistance and inductance of faulty branch, respectively, which are defined as (11).

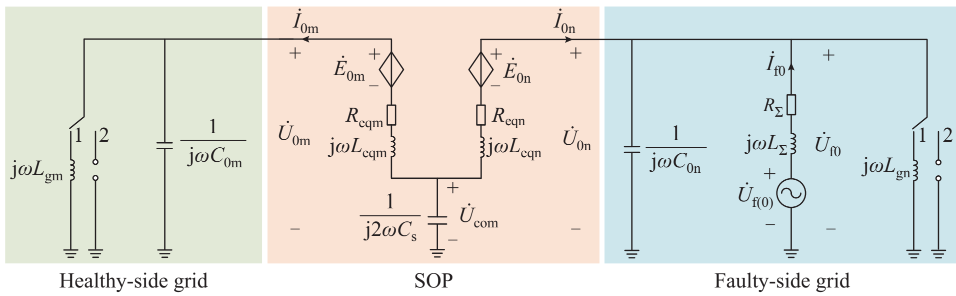

Fig. 3. Zero-sequence fault equivalent circuit of SOP-based FIDNs.

$$\begin{cases} R_\Sigma = 3R_f + R_{\Sigma1} + R_{\Sigma2} \\ L_\Sigma = L_{\Sigma1} + L_{\Sigma2} \end{cases} \tag{11}$$

where the subscripts 1 and 2 represent the positive- and negative-sequence components, respectively

As shown in Fig. 3, if the SOP does not activate its zero-sequence control strategy, the voltages $\dot{E}_{0m}$ and $\dot{E}_{0n}$ can be considered negligible (i.e., approximately zero). Under these conditions, the zero-sequence fault current flows from the faulty branch into the faulty-side grid, and then propagates through the SOP into the DC bus capacitors and the healthy-side grid.

C. SLG Fault Handling Method

To minimize the impact of SLG faults on FIDNs and suppress the fault arc as quickly as possible, an SOP-based SLG fault handling method is proposed, as illustrated in Fig. 4.

According to Fig. 4(a), when an SLG fault occurs, the power-frequency fault current flows from the faulty branch into the grounding capacitance and toward the SOP. At power frequency, a zero-sequence current isolation strategy is applied on the SOP to isolate the fault propagation, effectively preventing the fault current from reaching the SOP and the healthy-side grid.

In Fig. 4(b), during the isolation of the power-frequency fault current, an active injection control strategy is employed on the faulty-side MMC (i.e., $\dot{E}_{0n}$). The SOP injects zero-sequence currents at non-power frequencies into the faulty-side grid, allowing for GPI.

Once the grounding parameters have been identified, as shown in Fig. 4(c), the required inductive compensation current is calculated. The active injection control strategy on the faulty-side MMC is then replaced by an arc suppression strategy, which injects an appropriate compensation current into the faulty branch to nullify the fault current $\dot{I}_{f0}$ and suppress the arc.

Throughout the fault duration, the zero-sequence current isolation strategy also remains active on the healthy-side MMC, ensuring that the fault current does not propagate to the healthy-side grid.

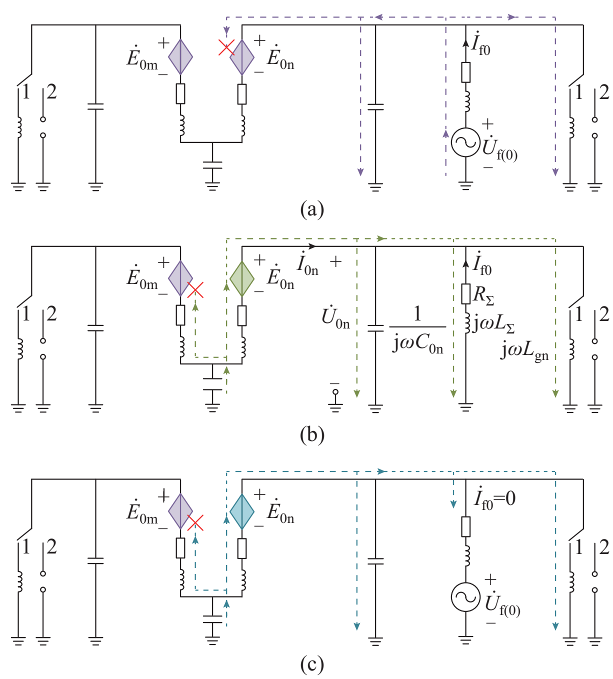

Fig. 4. SOP-based SLG fault handling method. (a) Zero-sequence current isolation at power frequency. (b) GPI at non-power frequencies. (c) Arc suppression at power frequency.

III. Fault Isolation and Arc Suppression Strategies

A. Fault Isolation Strategy

Equation (9) can be rewritten in the s-domain as (12). At the power frequency, the zero-sequence current $i_0(s)$ is determined by the differential-mode voltage $e_0(s)$ of SMs, along with zero-sequence voltage $u_0(s)$ and common-mode voltage $u_{com}(s)$.

$$(R_{\text{eq}}+sL_{\text{eq}})i_0(s)=e_0(s)-u_0(s)+u_{\text{com}}(s) \tag{12}$$

To control the zero-sequence current, it is proposed to utilize a feedback loop based on proportional-resonant (PR) control. Furthermore, the incorporation of feedforward loops for $u_0(s)$ and $u_{\text{com}}(s)$ can significantly enhance the response speed of the controllers. The control variable $e_0^*(s)$ is calculated as:

$$e_0^*(s)=(i_0^*(s)-i_0(s))\left(K_{\text{P}}+\frac{2K_{\text{R}}\omega_{\text{c}}s}{s^2+2\omega_{\text{c}}s+\omega_0^2}\right)+K_{\text{f}}(u_0(s)-u_{\text{com}}(s)) \tag{13}$$

where $i_0^*(s)$ is the reference value of zero-sequence current; K_{P} is the proportional coefficient; K_{R} is the resonant coefficient; ω_0 is the resonant frequency; ω_{c} is the resonant bandwidth; and K_{f} is the feedforward coefficient with values ranging from 0 to 1.

Actually, the PR-based feedback loop is inherently capable of controlling zero-sequence currents without steady-state error, while the feedforward loops for $u_0(s)$ and $u_{\text{com}}(s)$ are primarily intended to enhance the response speed of controllers. However, in practical systems, the grid-side zero-sequence voltage and the DC-side common-mode voltage may contain a small proportion of harmonics. If the feedforward coefficient K_{f} is set too high, these harmonics may be continuously amplified by the feedforward loop, causing positive feedback and ultimately leading to system instability [26], [27]. Consequently, in engineering applications, the feedforward coefficient K_{f} is typically set to a value less than 1. In this study, a conservative value of 0.6 is selected to achieve a balance between the response speed and stability of controllers.

From (13), setting $i_0^*(s)=0$ can isolate the propagation of SLG fault between different terminals of SOP.

B. Arc Suppression Strategy

As shown in (13), the arc suppression is achievable provided that $i_0^*(s)$ is set to an appropriate value. Based on Fig. 3, the current of faulty branch in the s-domain is given by:

$$i_{\text{f0}}(s)=\left(\frac{1}{sL_{\text{gn}}}-sC_{0\text{n}}\right)u_{0\text{n}}(s)-i_{0\text{n}}(s) \tag{14}$$

where $u_{0\text{n}}(s)$ and $i_{0\text{n}}(s)$ are the zero-sequence voltage and current on n-side grid, respectively.

To suppress the current of faulty branch to zero, the SOP needs to inject the following zero-sequence current:

$$i_{0\text{n}}(s)=\left(\frac{1}{sL_{\text{gn}}}-sC_{0\text{n}}\right)u_{0\text{n}}(s) \tag{15}$$

To prevent series resonance caused by the injection of the critical compensation current, the reference value of injected current is adjusted as:

$$i_0^*(s)=\left[\frac{1}{sL_{\text{gn}}}-(1+k_{\text{ov}})sC_{0\text{n}}\right]u_{0\text{n}}(s) \tag{16}$$

where k_{ov} is the overcompensation degree, which is set to be 5%.

C. Active Injection-based GPI Approach

As shown in (16), the effective arc suppression necessitates the precise identification of zero-sequence grounding parameters $C_{0\text{n}}$ and L_{gn} (if the Peterson coil grounding mode is used) on the faulty-side grid. Figure 4(a) illustrates that the identification of these grounding parameters at the power frequency is challenging due to the influence of faulty branch. To address this challenge, an active injection control strategy is proposed to mitigate the impact of the faulty branch on GPI.

As shown in Fig. 4(b), the injected signals are non-power-frequency signals, allowing the faulty-side grid to be treated as a signal-source system, which is excited solely by $\dot{E}_{0\text{n}}$ at the injected frequency. The KVL equation for the faulty-side grid is expressed as:

$$\dot{U}_{0\text{n}}=-(R_\Sigma+\text{j}\omega L_\Sigma)\dot{I}_{\text{f0}} \tag{17}$$

$$\dot{I}_{\text{f0}}=-\dot{I}_{0\text{n}}+\dot{U}_{0\text{n}}\left(\text{j}\omega C_{0\text{n}}+\frac{1}{\text{j}\omega L_{\text{gn}}}\right) \tag{18}$$

Substituting (18) into (17), we can obtain (19) for solving grounding parameters:

$$(R_\Sigma+\text{j}\omega L_\Sigma)\left[\left(\text{j}\omega C_{0\text{n}}+\frac{1}{\text{j}\omega L_{\text{g}}}\right)\dot{U}_{0\text{n}}-\dot{I}_{0\text{n}}\right]+\dot{U}_{0\text{n}}=0 \tag{19}$$

The solution steps for (19) are as follows.

In the first step, a single zero-sequence signal with a frequency above the power frequency is injected. The initial iterative value for the grounding capacitance can be obtained as:

$$C_{0\text{n}}^{(0)}=\left|\frac{\dot{I}_{0\text{n}}(\omega_1)}{\omega_1\dot{U}_{0\text{n}}(\omega_1)}\right| \tag{20}$$

where ω_1 is the angular frequency of injected signal in the first step.

In the second step, (19) can be split into two parts (real and imaginary parts). These split equations have four unknowns: R_Σ, L_Σ, $C_{0\text{n}}$, and L_{gn}. Therefore, in this step, dual non-power-frequency signals are injected to establish two complex equations.

The grounding parameters are solved using iterative algorithm. The initial iterative values of R_Σ, L_Σ, and L_{gn} are set to be 0, while that of $C_{0\text{n}}$ is set to be $C_{0\text{n}}^{(0)}$. This initial setting of the grounding capacitance ensures that the iterative process quickly converges to the actual value. Furthermore, if the faulty-side grid operates in the ungrounded mode, the calculated grounding impedance is likely to be substantial. In this case, the neutral point of the system is regarded as an open circuit, which does not affect the calculation of the grounding capacitance.

Figure 5 displays a complete block diagram of the SOP, incorporating the zero-sequence current isolation strategy and active injection control strategy, where U_{inj}^* is the reference amplitude of the injected signal; f_1, f_2, and f_3 are the three frequencies of injected signals; e_{a}^*, e_{b}^*, and e_{c}^* are the three-phase reference values of arm bridge voltages; e_d^* and e_q^* are the reference values of arm bridge voltages in the $dq0$ coordinate system; the subscripts + and – represent the positive and negative sequences, respectively.

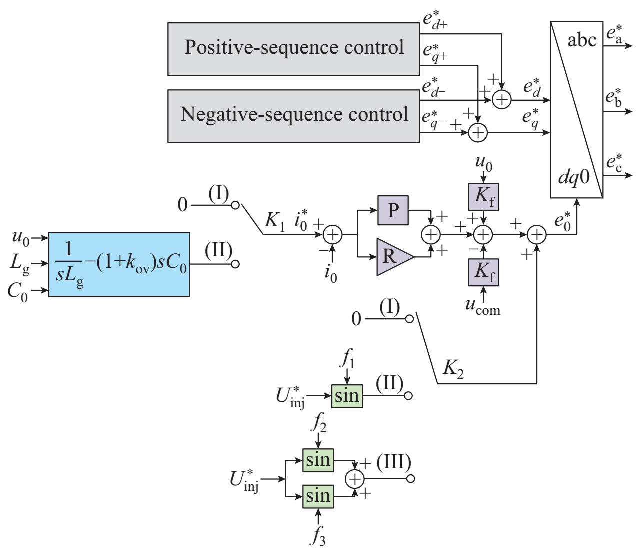

Fig. 5. Complete block diagram of SOP.

The functions of the control loops shown in Fig. 5 are listed in Table I.

TABLE I
FUNCTIONS OF CONTROL LOOPS

Mode	Control loop	Function
1	K_1=(I), K_2=(I)	Zero-sequence current isolation
2	K_1=(I), K_2=(II)	Single high-frequency signal injection
3	K_1=(I), K_2=(III)	Dual-frequency signal injection
4	K_1=(II), K_2=(I)	Power-frequency compensation current injection

IV. Discussion of Relevant Issues

A. Parameters of Injected Signals

For the active injection control strategy, the setting requirements for the frequency, amplitude, and injection duration of the injected signals are listed in Table II.

TABLE II
SETTING REQUIREMENTS FOR PARAMETERS OF INJECTED SIGNALS

Parameter	Setting requirement
Frequency	① Applicable frequency bands of simplified line model ② Constraints of SOP control capability ③ Impacts on grid
Amplitude	① Accuracy of measurement equipment ② Impacts on grid
Injection duration	Solution requirements of algorithm

The frequencies set for the injected signals are determined based on the frequency bands available for the simplified line model. The GPI is based on modeling the distribution feeder as a lumped zero-sequence capacitive reactance model. As the frequency increases, the error between this lumped parameter model and distributed parameter model gradually increases [28]. The ratio of the impedance amplitude of the lumped parameter model to that of the distributed parameter model is constrained to be less than twofold, and the error of their phase angles is kept below 90°. Based on the model parameters used in this paper, for a 20 km line, the applicable frequency range is 0-576 Hz for cable lines and 0-2117 Hz for overhead lines. Next, the frequency of injected signals should be limited to less than 10% of the SOP control frequency (500 Hz), ensuring that it can be accurately modulated by the SOP [27], [29]. Furthermore, the inter-harmonics frequency should be chosen as the injected signal frequency to minimize the impact of injected signals on the protection and control of the grid. Lastly, the frequency f_1 should be maximized within the permissible range to minimize the influence of the faulty branch and the inductance of Peterson coil on the calculation of the initial value. The frequencies f_2 and f_3 should be set near the power frequency to reduce errors caused by the frequency-dependent characteristics of system parameters. Therefore, the frequencies of injected signals are set as: $f_1 = 325$ Hz, $f_2 = 25$ Hz, and $f_3 = 75$ Hz.

The amplitudes set for the injected signals are determined based on the precision of measurement equipment and the potential impacts on the grid. The potential transformers commonly used in 10 kV distribution networks are WB1, and the standards require that the transformation ratio error at frequencies within 1 kHz does not exceed ±5% of their actual voltage [30]. Consequently, the amplitude of injected signals is set to be 10% of the rated voltage to ensure an adequate margin.

The total injection duration is set to be 300 ms. This involves injecting the signal at frequency f_1 for 100 ms, followed by the injection of signals at frequencies f_2 and f_3 for 200 ms. The data window length for phase extraction is set to be 40 ms, ensuring that 325 Hz, 25 Hz, and 75 Hz signals are orthogonal within the data window (i.e., the data window is the least common multiple of the periods of all signals). The GPI process is performed in the final 50 ms of the injection duration to ensure that the injection enters a steady state.

B. Starting Criterion

The starting criterion is set as:

$$\begin{cases} \left| \dot{U}_0 \right| \geq 10\% U_\mathrm{n} \\ \left| \dot{U}_1 \right| \geq 90\% U_\mathrm{n} \end{cases} \tag{21}$$

where $\dot{U}_1$ is the positive-sequence voltage; and U_n is the rated voltage of AC side. These values are extracted from the data measured over four power-frequency cycles.

The starting criterion requires the persistence of the condition for four power-frequency cycles. This is done to ensure that it remains unaffected by transient factors such as lightning strikes and load switching. Additionally, the positive-sequence voltage limitation can effectively prevent mis-activation caused by inter-phase short-circuit faults and inter-phase grounded short-circuit faults.

C. Implementation of SLG Fault Handling Method

A flow chart of the SLG fault handling method is shown in Fig. 6, where Δt_{I} is the stage of normal operation; Δt_{II} is the stage of active injection to identify the grounding parameters; and Δt_{III} is the stage of current compensation to suppress the fault arc.

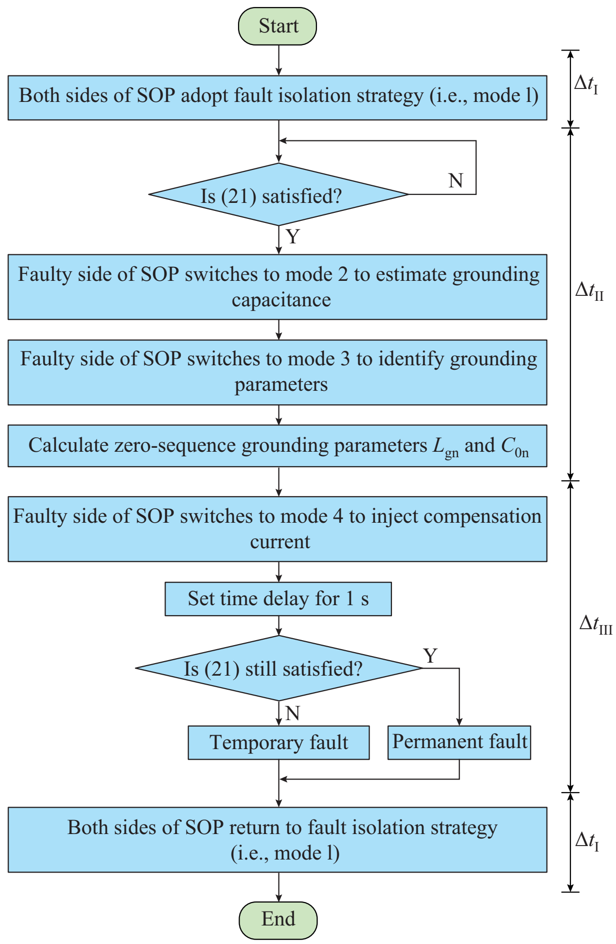

Fig. 6. Flow chart of SLG fault handling method.

V. Simulation Verification

A. Simulation Model and Parameters

A simulation model of an SOP-based FIDN shown in Fig. 7 has been developed in PSCAD/EMTDC to test the feasibility of the SLG fault handling method. In Fig. 7, S_{m} and S_{n} are the high-voltage networks connected to the distribution networks on the m-side and n-side of SOP, respectively; l_{m1}-l_{m3} and l_{n1}-l_{n3} are the cables; l_{m4}, l_{n4}, and l_{n5} are the overhead distribution lines; P_{m2}-P_{m4} and P_{n2}-l_{n5} are the loads; and K_{m} and K_{n} are the measurement points at the m-side and n-side of SOP, respectively. The main parameters of the simulation model are listed in Table III.

As shown in Fig. 7, two 10 kV distribution networks are flexibly interconnected via an SOP with a transformer-less configuration. The connection cables l_{m1} and l_{n1} distribute 5 MW of power from the m-side grid to n-side grid under the control of SOP. To highlight the general applicability of the SLG fault handling method and emphasize the effectiveness of its arc suppression strategy, the n-side grid is configured in the ungrounded mode.

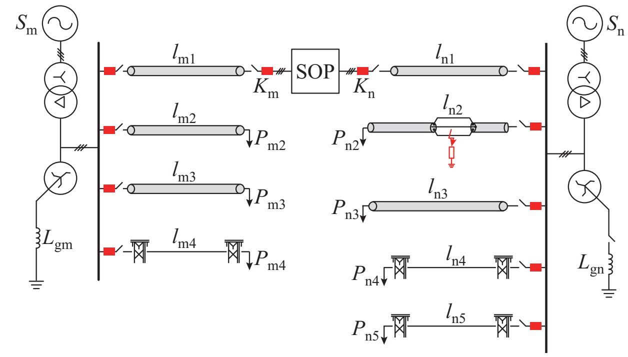

Fig. 7. Simulation model of SOP-based FIDN.

TABLE III
Main Parameters of Simulation Model

Parameter	Value
Solution time step	5 μs
AC grid rated voltage	10 kV
DC bus rated voltage	±10 kV
Distribution transformer capacity	15 MVA
Transformer leakage reactance	0.1 p.u.
Number of SMs on bridge arm	40
Capacitance of SM	3000 μF
Inductance of bridge arm	31.8 mH
DC bus capacitance	2000 μF
Length and load of l_{m1}	10 km, (5+j0)MVA
Length and load of l_{m2}	10 km, (3+j0.05)MVA
Length and load of l_{m3}	5 km, (3+j0.05)MVA
Length and load of l_{m4}	10 km, (3+j0.05)MVA
Length and load of l_{n1}	15 km, (−5+j0)MVA
Length and load of l_{n2}	15 km, (3+j0.05)MVA
Length and load of l_{n3}	15 km, (1.5+j0.05)MVA
Length and load of l_{n4}	10 km, (1.5+j0.05)MVA
Length and load of l_{n5}	10 km, (3+j0.05)MVA
Length and load of l_{n6}	5 km, (3+j0.05)MVA

B. Verification of SLG Fault Handling Method

Taking an ATG fault occurring on l_{n2} as an example, the simulation results at different locations are shown in Figs. 8-10.

As shown in Fig. 8(a) and (c), after the fault occurs, the faulty-phase voltage decreases, while the healthy-phase voltages increase, and the zero-sequence current is consistently maintained at a low level due to the zero-sequence current isolation strategy. As shown in Fig. 8(b) and (d), during the initial 100 ms after the fault occurs, a zero-sequence high-frequency signal of 325 Hz is injected. During the next 200 ms, the zero-sequence dual-frequency signals of 25 Hz and 75 Hz are injected. After 300 ms of the fault occurrence, the power-frequency compensation current is injected into the grid to extinguish the fault arc.

As shown in Fig. 9(a) and (b), immediately after the fault, the root mean square (RMS) value of the faulty-phase current of the faulty branch is 94.2 A. When the current compensation control strategy is implemented, the faulty-phase current of faulty branch is suppressed to 6.4 A, which is below the fault current threshold (10 A) for the Peterson coil grounding mode [31]. The faulty-phase voltage of faulty branch also decreases to zero. As shown in Fig. 9(c), the GPI is completed during the final 50 ms of active injection stage. The actual value of the grounding capacitance for the n-side grid is found to be 19.29 μF, and the calculated value is stable and accurate.

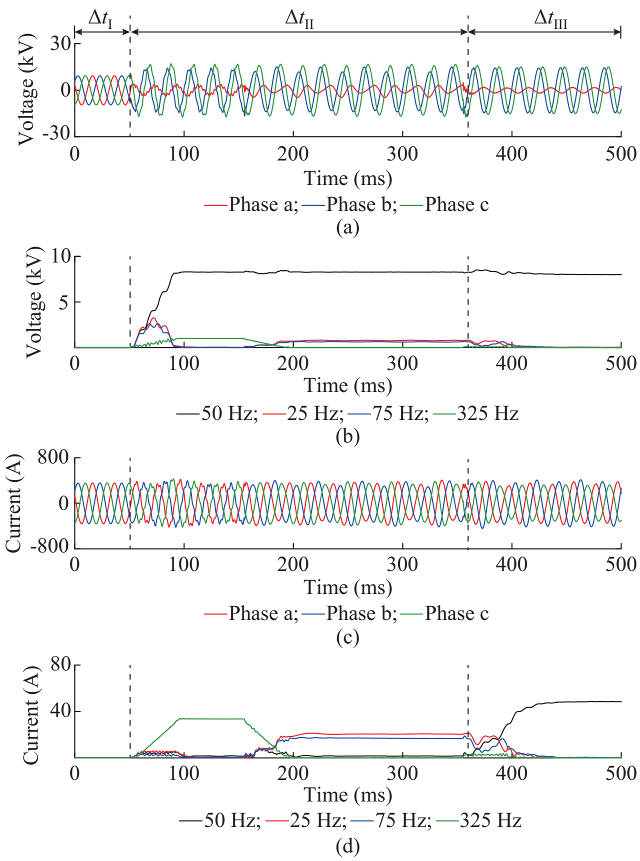

Fig. 8. Simulation results at K_n when an ATG fault occurs on l_{n2}. (a) Three-phase voltages. (b) Zero-sequence voltage amplitudes at different frequencies. (c) Three-phase currents. (d) Zero-sequence current amplitudes at different frequencies.

As shown in Fig. 10, the zero-sequence current isolation strategy limits the fault propagation to the healthy-side grid. After the completion of active injection and arc suppression, the voltage and current of the healthy-side AC bus of the SOP remain balanced in all three phases, with both frequency and amplitude staying constant.

C. GPI Performance Verification in Different Fault Cases

The test cases include faults occurring at the head, middle, and end of l_{n1}, and the load terminal on l_{n2}. The GPI performance is verified with the transition resistance ranging from 10 Ω to 10 kΩ. In each fault case, the grounding capacitance is calculated every 1 ms over a 50 ms interval. The distribution of the min-max, average, and middle 60% (i.e., 20%-80%) of the relative errors |*err*| for grounding capacitance in different fault cases is shown in Fig. 11.

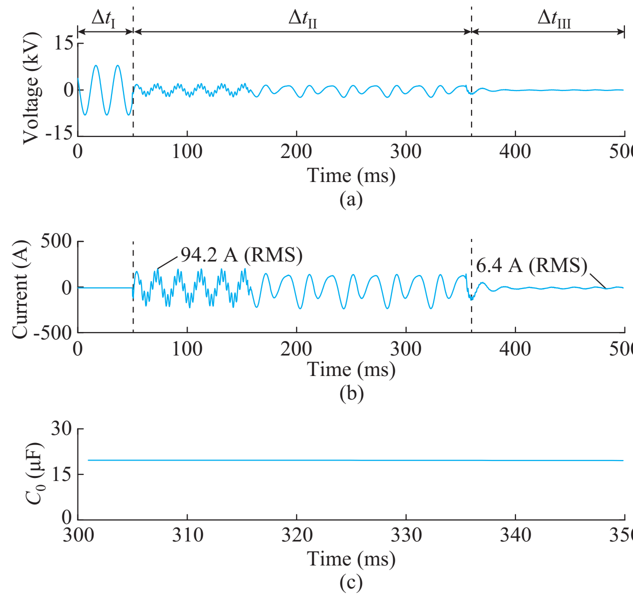

Fig. 9. Simulation results at faulty branch when an ATG fault occurs on l_{n2}. (a) Faulty-phase voltage of faulty branch. (b) Faulty-phase current of faulty branch. (c) Grounding capacitance.

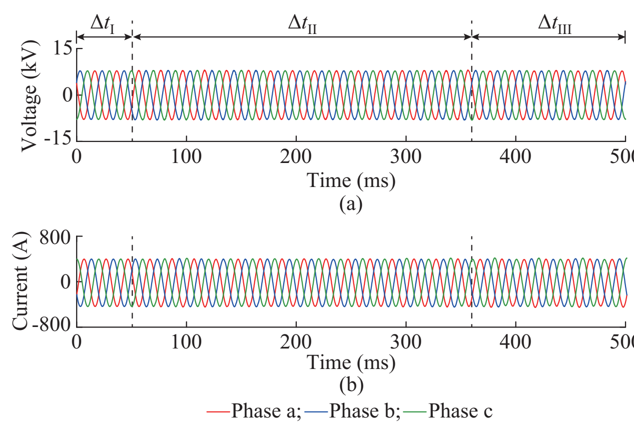

Fig. 10. Simulation results at K_m when an ATG fault occurs on l_{n2}. (a) Three-phase voltages. (b) Three-phase currents.

As shown in Fig. 11, the results exhibit some variability due to factors such as phasor extraction and calculation errors. For all the simulation results, the maximum relative error does not exceed 5%. Besides, averaging the calculation results can further reduce the impact of random errors, thereby limiting the error to within 4%. Therefore, it is capable of accurately identifying the grounding parameters after a fault.

D. Performance Verification of Arc Suppression in Different Fault Cases

In different fault cases, the RMS value for current of faulty branch I_{fa}, both before and after the arc suppression, is shown in Fig. 12.

As shown in Fig. 12, with various transition resistances, the compensated current of faulty branch remains below the arc extinguishing current. This result is consistent across different fault cases.

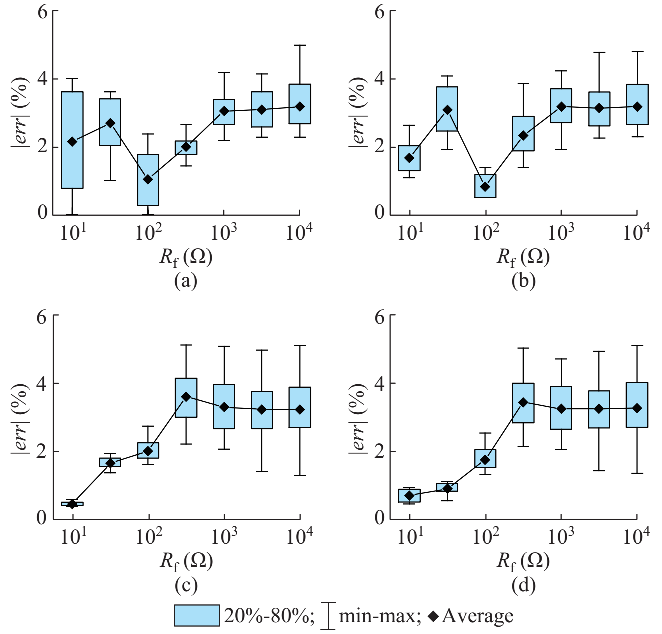

Fig. 11. Relative error of grounding capacitance in different fault cases. (a) Fault occurs at head of l_{n1}. (b) Fault occurs at middle of l_{n1}. (c) Fault occurs at end of l_{n1}. (d) Fault occurs at load terminal of l_{n2}.

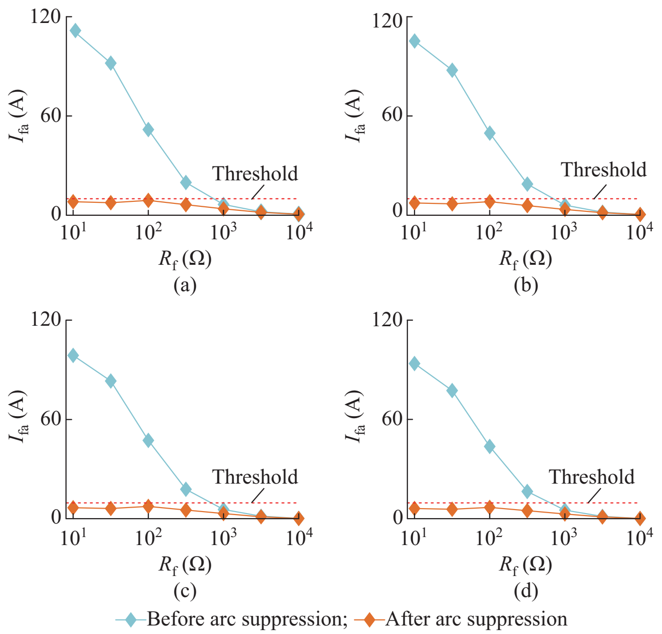

Fig. 12. RMS value for current of faulty branch before and after arc suppression in different fault cases. (a) Fault occurs at head of l_{n1}. (b) Fault occurs at middle of l_{n1}. (c) Fault occurs at end of l_{n1}. (d) Fault occurs at load terminal of l_{n2}.

E. Comparison with Traditional Voltage-based Arc Suppression Strategy

Taking an ATG fault occurring at the end of l_{n1} as an example, the proposed arc suppression strategy is compared with traditional voltage-based arc suppression strategy (i. e., directly controlling the faulty-phase voltage of SOP to zero). The simulation results are shown in Fig. 13.

As shown in Fig. 13(a) and (b), the proposed arc suppression strategy successfully achieves a substantially lower residual faulty-phase voltage and current of faulty branch when compared with the voltage-based arc suppression strategy. As shown in Fig. 13(c), the residual faulty-phase current obtained with the proposed arc suppression strategy is 6.4 A, which is sufficient to extinguish the fault arc. By contrast, the voltage-based arc suppression strategy yields a residual faulty-phase current of 62.7 A, which is insufficient for arc suppression.

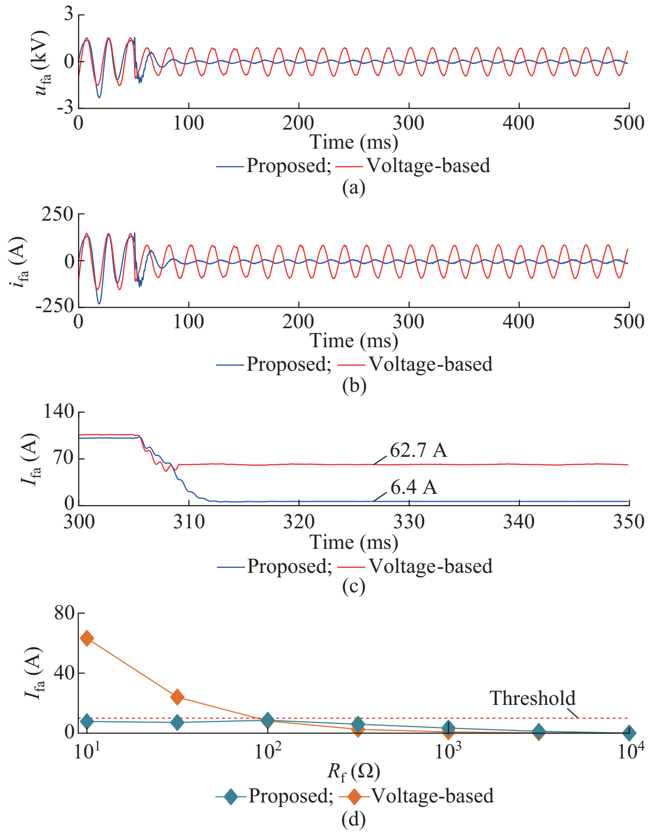

Fig. 13. Simulation results of two arc suppression strategies. (a) Faulty-phase voltage of faulty branch. (b) Faulty-phase current of faulty branch. (c) Faulty-phase current amplitude of faulty branch. (d) Average current after arc suppression with different transition resistances.

As shown in Fig. 13(d), with different transition resistances, the proposed arc suppression strategy limits the current of faulty branch below the threshold for arc suppression. On the other hand, the voltage-based arc suppression strategy exhibits inadequate performance in handling LR faults at the end of feeder.

F. Comparison with ASDs Based on Different Control

In this subsection, the feasibility of the proposed arc suppression strategy is further verified. Table IV summarizes the performance of different arc suppression strategies.

It can be seen in Table IV that the ASDs based on voltage control are simple to implement as they do not require the GPI. With magnetically controlled reactor (MCR), these strategies can effectively reduce the capacity of ASDs [16], [17]. However, the main drawback of these strategies is their limited performance in dealing with LR faults, which may even lead to an increase in the grounding current.

TABLE IV
COMPARISON OF DIFFERENT ARC SUPPRESSION STRATEGIES

Strategy	Transition resistance	Robustness to grid topology	Requirement of GPI	Interference with normal operation	Additional devices
ASDs based on voltage control [15]-[19]	HR	Arbitrary (*)	No (*)	No (*)	Yes
ASDs based on current control [21], [22]	LR and HR (*)	Arbitrary (*)	Yes	Yes	Yes
ASDs based on integrated control [20]	LR and HR (*)	Arbitrary (*)	Yes	Yes	Yes
SOP-based [25]	LR and HR (*)	Unique	Yes	No (*)	No (*)
Proposed arc suppression	LR and HR (*)	Arbitrary (*)	Yes	No (*)	No (*)

Note: "*" means better performance in a specific aspect.

The ASDs based on current control are effective in handling both HR and LR faults. However, these strategies rely on injecting signals before the fault occurs to identify the grounding parameters, which can interfere with the normal operation of distribution network.

The integration of residual voltage compensation control into the ASDs based on voltage control improves arc suppression for LR faults. This strategy, known as integrated control, enhances performance but increases reliance on GPI.

In transformer-less SOP-based FIDNs, the SOP itself can control the voltage and current at neutral point through additional control strategies, eliminating the necessity for ASDs. Although this strategy has been documented in [25], it typically requires a three-phase four-wire topology, which is rarely used in medium-voltage distribution networks. Consequently, its application in three-phase three-wire grids presents challenges.

The proposed arc suppression strategy based on current control injects non-power-frequency signals after a fault occurs to achieve GPI, avoiding any interference with the normal operation of distribution network. This approach has demonstrated excellent robustness to transition resistance and does not impose any special requirements on grid topologies.

VI. CONCLUSION

In this study, a novel SLG fault handling method for transformer-less SOP-based FIDNs is proposed. This method leverages an active injection-based GPI approach to efficiently suppress fault arcs, specifically targeting LR SLG faults. The key advantages of the SLG fault handling method are summarized as follows.

Firstly, the proposed arc suppression strategy does not require many additional injection devices and only necessitates minor modifications to the SOP, making it more cost-effective than the traditional flexible arc suppression strategies. Secondly, the active injection-based GPI approach demonstrates high accuracy across numerous fault cases. The signal injection and parameter identification are immediately activated after the fault occurrence. Unlike approaches that identify parameters during normal operation, the active injection-based GPI approach is unaffected by grid topology changes and does not disrupt power quality during normal operation. Thirdly, compared with the traditional voltage-based arc suppression strategies, the proposed arc suppression strategy is more effective in suppressing LR SLG faults, particularly those occurring at the end of feeders.

However, the primary limitation of the SLG fault handling method is its relatively complex control strategy, which is specifically tailored to SOP-based FIDNs or distribution networks equipped with VSCs. As such, it is not applicable to traditional distribution networks that lack power electronic devices.

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