Detailed Equivalent Modeling and Simulation of Modular Multilevel Converters with Partially-integrated Battery Energy Storage

Ramin Parvari, Shaahin Filizadeh, and Ioni Fernando

***Abstract*—This paper develops a detailed equivalent model for modular multilevel converters with partially-integrated battery energy storage. The proposed model gains computational efficiency in two ways. Firstly, it markedly reduces the large number of nodes in the conventional switching model of the converter, thereby shrinking the size of its admittance matrix. Secondly, it avoids computationally expensive re-triangularization of the admittance matrix during the normal operation of the converter and restricts it only to the rare occasions of converter blocking. Mathematical derivation of the model is carried out using differential equations of the converter. The computational efficiency and accuracy of the proposed model are confirmed by comparison of the results from its implementation in the PSCAD/EMTDC simulator against conventional detailed switching models and measurements from a single-phase scaled-down laboratory setup. This paper also shows a case study wherein a converter with partially-integrated batteries is included in the CIGRE B4-5 benchmark system.**

***Index Terms*—Battery energy storage system, equivalent model, electromagnetic transient simulation, modular multilevel converter.**

I. Introduction

ESCALATING deployment of renewable energy resources has made modern power grids more vulnerable to disturbances than those predominantly using synchronous machine-based generation [1]. The inherent variations and unpredictability of renewable resources pose challenges to the reliability of grids, voltage and frequency stability, and power quality [2], [3]. To address these issues, energy storage systems can be employed to mitigate the variations in availability, and improve power quality by providing ancillary services to the grid. Among various energy storage technologies, battery energy storage systems (BESSs) have sparked considerable attention due to their fast response, high-power capability, long cycle lifetime, and low self-discharge rate [4]-[8].

Typically, a two- or three-level voltage source converter (VSC) followed by a DC-DC converter is used to interface the BESS with the AC grid. The DC-DC converter steps up the battery voltage to that of a common DC collector bus; the VSC then converts the DC bus voltage to the voltage required by the AC grid. This type of integration is extensively examined in [9], [10]. Nevertheless, two- or three-level VSCs fall short compared with the family of modular multilevel converters (MMCs), as MMCs offer critical benefits such as modularity, scalability, low harmonics, and reduced switching losses [11], [12], thanks to their usage of building blocks known as sub-modules (SMs).

The concept of integration of BESSs into MMCs was first introduced in [13] wherein all SMs are equipped with BESSs via a bi-directional DC-DC converter. Concentrating on the potential of MMCs with full battery integration, [14] explores the converter by deriving an expression for circulating current to address reactive power compensation and rectify asymmetries in the AC grid voltage. In [15], control algorithms are devised to balance the state of charge of the batteries in MMCs with partially-integrated BESSs (MMC-BESSs), with corresponding limits on gains set. MMCs with full integration of BESSs, however, might be neither necessary nor cost-effective in high-voltage DC (HVDC) applications where a considerable number of SMs are present while only a small fraction of the capacity of the converter is required for ancillary services that require energy storage. Hence, MMC-BESSs emerge in which only a subset of SMs in each arm are supplemented with batteries. For example, [16] presents a converter in which the installed energy storage is 10% of the total rated power of the converter. MMC-BESSs combine the benefits of properly-sized energy storage with the quality and controllability of an MMC for high-power applications.

Computer simulation of MMCs, in general, and MMC-BESSs, in particular, is a challenging task using electromagnetic transient (EMT) simulators if models are constructed with topological connections of individual power electronic switches and passive elements. This is known as a detailed switching model (DSM). In EMT simulations, the electrical

Manuscript received: December 14, 2023; revised: April 30, 2024; accepted: June 26, 2024. Date of CrossCheck: June 26, 2024. Date of online publication: October 22, 2024.

This work was supported in part by the Natural Sciences and Engineering Research Council (NSERC) of Canada, MITACS Accelerate, Manitoba Hydro, and by the University of Manitoba.

R. Parvari and S. Filizadeh (corresponding author) are with the University of Manitoba, Winnipeg, MB R3T 5V6, Canada (e-mail: parvarir@myumanitoba.ca; shaahin.filizadeh@umanitoba.ca).

I. Fernando is with the Grid Infrastructure Planning Department of Manitoba Hydro, Winnipeg R3C 0G8, Canada (e-mail: itfernando@hydro.mb.ca).

DOI: 10.35833/MPCE.2023.000986

circuit is initially transformed into a companion network consisting of conductances and current sources, and subsequently solved to determine node voltages at each time step [17]. Simulating power electronic converters necessitates re-inversion of the admittance matrix at every switching event. Consequently, employing the DSM method results in large admittance matrices for MMC-type converters, which must be modified and inverted whenever the state of even a single switch changes. As a result, simulating MMCs with DSM presents significant and prohibitive challenges in reducing computation time [18]. The admittance matrix of a network with MMC-BESS is even larger and must be modified and inverted very frequently, as the associated DC-DC converters are operated with high frequency [19]. Thus, DSMs are typically employed for MMCs with a small number of SMs [20].

To overcome this major disadvantage, detailed equivalent models (DEMs) have been introduced, which offer dramatic computational efficiency while retaining the same level of accuracy as DSMs. This is commonly achieved by replacing each arm of the MMC with a Thevenin or Norton equivalent circuit, which reduces hundreds of nodes to two or three. In [18], a method is introduced that relies on partitioning the admittance matrix of the system and deriving an efficient time-varying Thevenin equivalent circuit for the stack of SMs in conventional MMCs. Similar approach is taken in [21] while enhancing accuracy of the model during DC faults. For MMCs with full integration of BESSs, the stack of SMs is lumped to a Thevenin equivalent circuit with a time-varying resistor [19], [22]. A computationally efficient equivalent model of current source MMC is derived in [23], where each arm of the converter is aggregated to a Norton equivalent circuit with two nodes by eliminating internal intermediate nodes.

It must be noted that even with a DEM the network admittance matrix (albeit a much smaller one than that of a DSM) must still be re-factorized at every switching instant because the Thevenin (or Norton) equivalent resistor of the arm circuit varies with time depending on the switching signal of each SM [24]. Therefore, it is evident that avenues for improvement of the computational efficiency of DEMs exist.

This paper develops a novel DEM for MMC-BESSs. An equivalent voltage source is developed that, combined with one insulated gate bipolar transistor (IGBT) and two diodes, represents the MMC's arm stack in normal and blocked operation modes. The value of the voltage source is obtained through differential equations with the voltages of SM capacitors and currents of inductors of DC-DC converters as the state variables. The role of the included IGBT is to switch between normal and blocked modes of the converter. Two diodes serve as an equivalent half-bridge diode rectifier during blocking with no impact during normal operation. In the derivation of the proposed DEM, both the Euler and trapezoidal integration methods are used to achieve a constant admittance matrix for the converter to circumvent frequent re-factorization during normal operation, thus achieving significant computational efficiency improvement. Matrix re-inversions in the proposed DEM are only limited to rare events when the converter is blocked, e.g., in a DC fault.

The proposed model is well-suited for system-level analyses, particularly when examining the behavior of MMC-BESS within interconnected systems. State variables such as capacitor voltages and inductor currents are accessible in full detail and can be leveraged for control purposes. Additionally, the developed EMT model can aid in designing and sizing individual components for specific applications. However, this model does not account for switching power losses, as detailed physical characteristics of power electronic switches are not considered, thus excluding conduction and switching losses from the analysis.

The paper proceeds with continuous-time modeling of the stack of SMs in Section II, and model discretization in Section III. Section IV describes the DC-DC converter control. A simulation case study of the converter is presented in Section V. Computational efficiency of the proposed model is studied in Section VI. The accuracy of the proposed model is verified against experimental results in Section VII, followed by the conclusion in Section VIII.

II. Continuous-time Modeling of Stack of SMs

Figure 1(a) shows a three-phase MMC-BESS with the stack of SMs and arm inductors in the upper and lower arms. The stack of SMs consists of two SM types: those with a battery and a DC-DC converter (BESS-SMs) and those with conventional SMs (CONV-SMs), as shown in Fig. 1(b) and (c), respectively. The aim of the proposed model is to represent the stack of SMs with a computationally efficient model; once obtained, each arm stack is then connected to the arm inductors and the rest of the system using conventional EMT models.

The total number of SMs in each arm is N, out of which there are M BESS-SMs. In both SM types, the main switch cell is a half-bridge (HB) arrangement consisting of two switches denoted as T_1 and T_2 in Fig. 1(b) and (c). The on-state resistance of these switches is denoted as R_{on}. Each SM has a capacitor with a capacitance of C_{sm} and leakage resistance of R_{Csm} that retains an instantaneous voltage v_{Csm}. The current of the CONV-SM capacitor has only one component, i.e., i_{Carm} (coming from the right side), while the BESS-SM capacitor current is composed of two components, i.e., i_{Carm} and i_{Cbat} (coming from the left side). Current i_{Carm} is in fact the arm current i_{arm} switched by the main switch cell, and i_{Cbat} is the current provided by BESS. Each arm consists of an arm inductor with the inductance of L_{arm}. The voltage produced by each SM is denoted as v_{sm}. Note that all variables such as v_{Csm} and i_{arm} may be expressed as functions of time using the notation (t) after the variable to represent their instantaneous values at time t throughout the paper.

To increase the battery voltage v_b to the level required for the SM capacitor, a boost converter is used. The converter must facilitate bidirectional energy transactions between the battery and the terminal power system. For this purpose, a bidirectional boost converter is considered. The boost converter is composed of a SM inductor L_{sm} with series resistance of R_L that carries the current i_L and a switch cell containing IGBTs Q_1 and Q_2 with respective anti-parallel diodes.

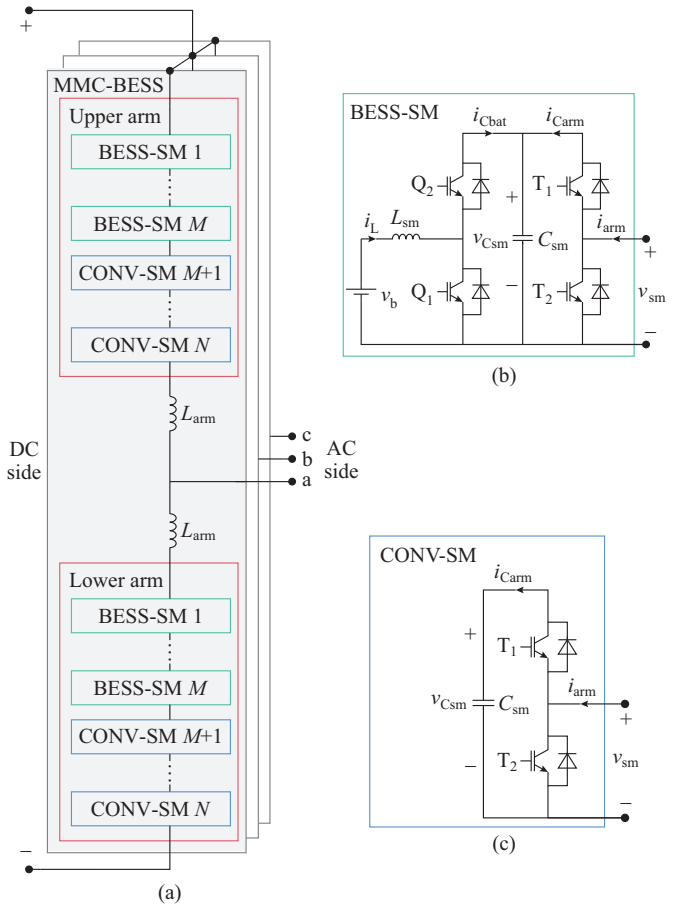

Fig. 1. Circuit topology of MMC BESS. (a) Three-phase MMC-BESSs. (b) BESS-SM. (c) CONV-SM.

A. Modeling for Normal Operation

In this subsection, the arm stack is modeled in the normal mode for which the main SM switch cells are operated according to modulation waveforms and switching strategy of choice. A circuit analysis approach is adopted to derive the equivalent circuit of the arm stack. For this purpose, the switch cells, i.e., the main SM switch cell or the boost converter's switch cell in the DC-DC boost converter, are modeled using a combination of dependent voltage and current sources, and then they are replaced with their equivalents.

1) Main SM Switch Cell

The main SM switch cell is shown in Fig. 2(a), wherein switches T_1 and T_2 are operated in a complementary manner. If the switching function $s(t)$ of the main switch cell is defined as (1), the SM voltage v_{sm} and the current i_{Carm} can be written as (2).

$$s(t)=\begin{cases}1 & T_1\text{: on, } T_2\text{: off}\\ 0 & T_1\text{: off, } T_2\text{: on}\end{cases} \tag{1}$$

$$\begin{cases}v_{sm}(t)=R_{on}i_{arm}(t)+s(t)v_{Csm}(t)\\ i_{Carm}(t)=s(t)i_{arm}(t)\end{cases} \tag{2}$$

R_{on} is considered to be the same for IGBTs and anti-parallel diodes, as is commonly done in EMT-type models. Equation (2) offers a dependent-source representation of the cell, as indicated in Fig. 2(b).

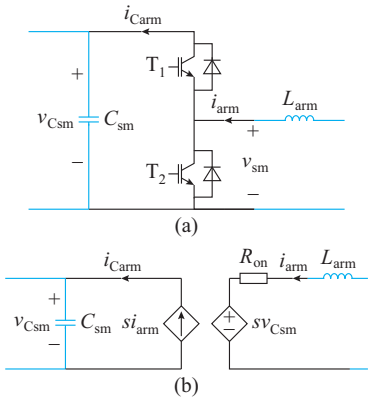

Fig. 2. Main SM switch cell. (a) Main SM switch cell. (b) Model of main SM switch cell with dependent sources.

2) Switch Cell in DC-DC Boost Converter

The switch cell in the DC-DC boost converter is shown in Fig. 3(a). With a switching function $q(t)$ for Q_1 and Q_2 defined as (3), the voltage and current relationships at the ports of the switch cell can be written as (4).

$$q(t)=\begin{cases}1 & Q_1\text{: on, } Q_2\text{: off}\\ 0 & Q_1\text{: off, } Q_2\text{: on}\end{cases} \tag{3}$$

$$\begin{cases}v_{Q1}(t)=R'_{on}i_L(t)+\big(1-q(t)\big)v_{Csm}(t)\\ i_{Cbat}(t)=\big(1-q(t)\big)i_L(t)\end{cases} \tag{4}$$

where R'_{on} is the on-state resistance of a DC-DC boost converter switch; and v_{Q1} is the voltage across switch Q_1. This leads to the representation of the switch cell with dependent sources, as shown in Fig. 3(b).

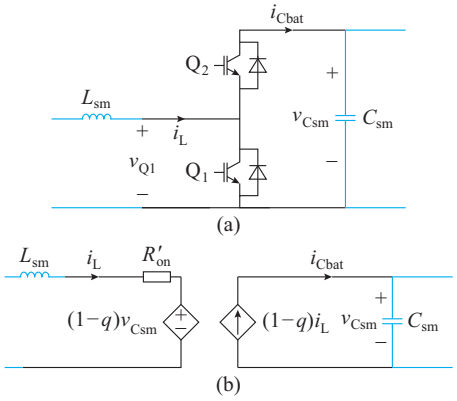

Fig. 3. Switch cell in DC-DC boost converter. (a) DC-DC boost converter switch cell. (b) Model of DC-DC boost converter switch cell with dependent sources.

By replacing the two switch cells with their dependent-source equivalent models, a BESS-SM and a CONV-SM can be represented as shown in Fig. 4(a) and (b), respectively.

To obtain a computationally-efficient admittance matrix-based EMT simulation model, the equivalent circuits of SMs in Fig. 4 are further reduced to only one voltage source in series with a resistor by replacing other circuit elements using algebraic and differential equations that govern those elements. These equations are interfaced with the nodal-analysis solution of the network.

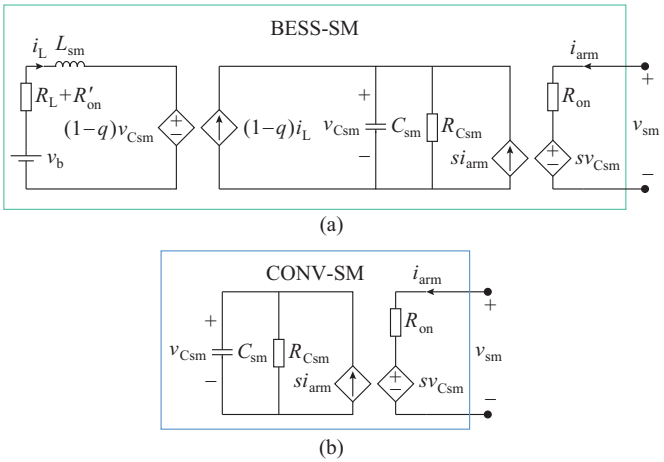

Fig. 4. Normal mode model of SM with dependent sources. (a) BESS-SM. (b) CONV-SM.

Figure 5 depicts the equivalent model that shows two SM types, each involving only three nodes (two terminal nodes and one internal node between the dependent voltage source and the equivalent resistance).

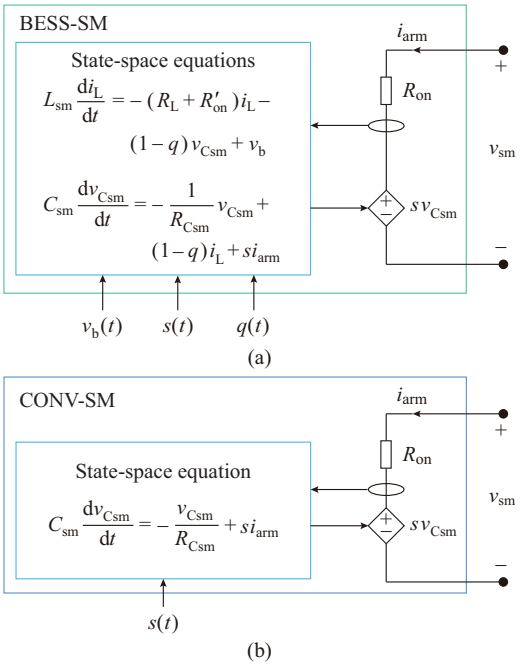

Fig. 5. Normal mode model of SM represented by differential equations. (a) BESS-SM. (b) CONV-SM.

By connecting SM models together, the equivalent arm model of a MMC-BESS is achieved, as illustrated in Fig. 6, in which v_{stack} is the total voltage produced by stack of SMs. This model is valid only for the normal operation mode in which the main switches in each SM, i.e., T_1 and T_2, are switched in a complementary manner. Note that vector algebra is used in the derivation of arm model in Fig. 6. It must be noted that two types of vector multiplication are used in this model. The first one is the dot product (denoted by "·"), which returns a scalar value equal to the sum of the products of the corresponding entries of two vectors. The second one is a product without dot notation that gives a vector whose elements are achieved by multiplication of the corresponding entries of two (or more) vectors. The definitions of the vectors in Fig. 6 are expressed in (5)-(10), where $\mathbf{1}$ is the ones vector, $\boldsymbol{s}(t)$ is the SM switching vector, $\boldsymbol{q}(t)$ is the DC-DC switching vector, $\boldsymbol{v}_{Csm}(t)$ is the vector of SM capacitor voltages, $\boldsymbol{i}_L(t)$ is the vector of DC-DC inductor currents, and $\boldsymbol{v}_b(t)$ is the vector of battery voltages. In these equations, numbered subscripts denote the variable in the respective SMs, either CONV-SMs or BESS-SMs.

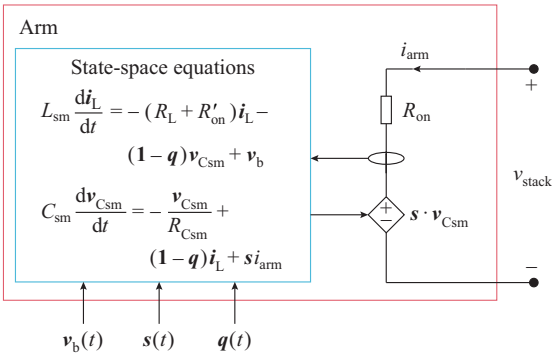

Fig. 6. Model of MMC-BESS arm during normal operation with differential equations.

$$\mathbf{1}=\left[\underbrace{1,1,\ldots,1}_{N}\right]^{\mathrm{T}} \tag{5}$$

$$\boldsymbol{s}(t)=\left[\underbrace{s_1(t),s_2(t),\ldots,s_N(t)}_{N}\right]^{\mathrm{T}} \tag{6}$$

$$\boldsymbol{q}(t)=\left[\underbrace{q_1(t),q_2(t),\ldots,q_M(t)}_{M},\underbrace{1,1,\ldots,1}_{N-M}\right]^{\mathrm{T}} \tag{7}$$

$$\boldsymbol{v}_{Csm}(t)=\left[\underbrace{v_{Csm1}(t),v_{Csm2}(t),\ldots,v_{CsmN}(t)}_{N}\right]^{\mathrm{T}} \tag{8}$$

$$\boldsymbol{i}_L(t)=\left[\underbrace{i_{L1}(t),i_{L2}(t),\ldots,i_{LM}(t)}_{M},\underbrace{0,0,\ldots,0}_{N-M}\right]^{\mathrm{T}} \tag{9}$$

$$\boldsymbol{v}_b(t)=\left[\underbrace{v_{b1}(t),v_{b2}(t),\ldots,v_{bM}(t)}_{M},\underbrace{0,0,\ldots,0}_{N-M}\right]^{\mathrm{T}} \tag{10}$$

B. Modeling for Blocked Mode

When the converter is blocked, e.g., during a DC fault, all IGBTs are turned off and only the freewheeling diodes conduct the current. By adopting a similar circuit-based approach, the blocked-mode models of the BESS-SM and CONV-SM are obtained, as shown in Fig. 7(a) and (b), respectively. It is worth noting that these circuits resemble those in Fig. 4 except that si_{arm} is replaced with i_{Carm}.

The same procedure is followed to transform the derived circuits to differential equations, as shown in Fig. 8.

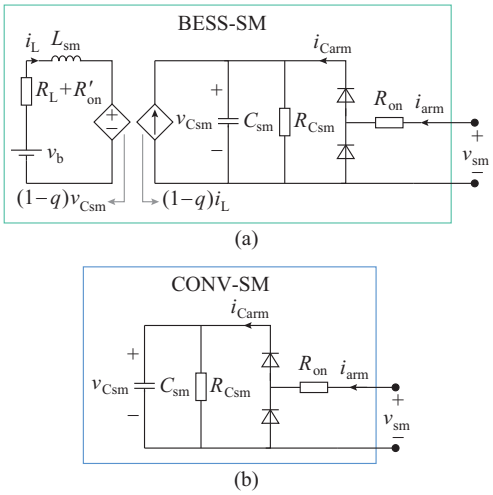

Fig. 7. Blocked mode model of SM with dependent sources. (a) BESS-SM. (b) CONV-SM.

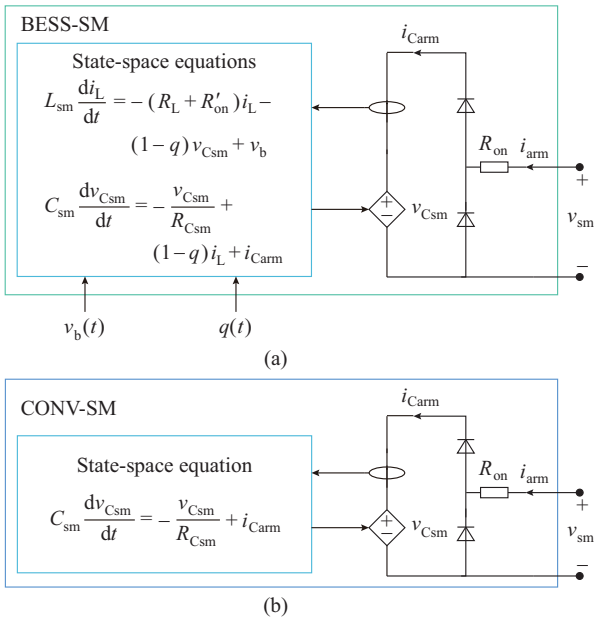

Fig. 8. Blocked mode model of SM represented by differential equations. (a) BESS-SM. (b) CONV-SM.

In the blocked mode, each SM is a half-wave diode rectifier and hence series connected SMs may be considered as one equivalent half-wave rectifier. The model of the arm stack circuit is readily realized by series connection of all SMs and using vector notation, as indicated in Fig. 9.

C. Generalized Arm Stack Model

The equivalent circuits of the converter arm of an MMC-BESS for normal and blocked modes of operation can be amalgamated into a single circuit by adding an extra controlled switch with an on-state resistance of R_{on} and two diodes. This is illustrated in Fig. 10, where the controlled switch is turned on/off using the blocking signal. As long as the arm operates in normal mode, the switch is turned on and, along with the anti-parallel diode, it inserts the equivalent voltage source into the path of the current.

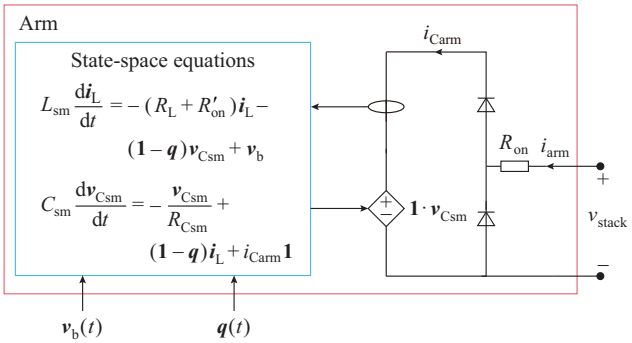

Fig. 9. Blocked mode model of arm represented by differential equations.

In the blocked mode of operation, the controlled switch is turned off and the circuit becomes a HB diode rectifier. The operation modes are determined according to the blocking signal defined as follows.

$$\begin{cases} b(t)=\begin{cases}0 & \text{normal mode}\\ 1 & \text{blocked mode}\end{cases} \\ \bar{b}(t)=1-b(t)\end{cases} \tag{11}$$

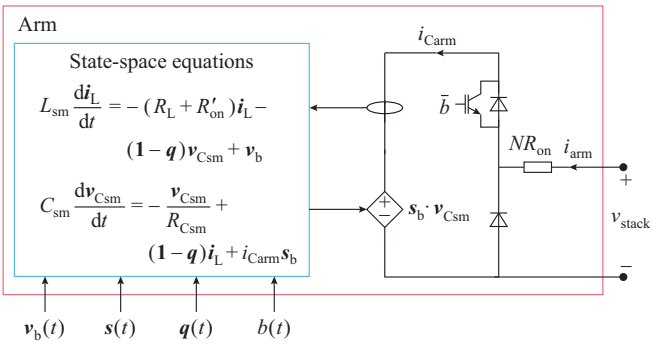

Fig. 10. Generalized model of arm stack.

Some parameters and variables of the circuit in Fig. 10 must be modified through a selector function whose purpose is to switch between the normal and blocked modes. This is done via the following vector function with the same length as the ones introduced in (5)-(10).

$$\boldsymbol{s}_b(t)=\bar{b}(t)\boldsymbol{s}(t)+b(t)\mathbf{1} \tag{12}$$

III. Model Discretization

In this section, the governing equations of the arm stack derived in Section II are discretized for the purpose of time-domain simulation with a fixed time step. Depending on the integration method used in the discretization process, there will be different EMT models for the arm of the converter with varying accuracy and numerical stability properties. The trapezoidal rule of integration is widely used in EMT modeling applications. In the context of an MMC with patially-integrated BESS, however, using the trapezoidal rule yields a time-varying Thevenin resistor in the discretized model of the dependent voltage source in Fig. 10. This is due to the fact that the value of the dependent voltage source is related to its current at the present time step, i.e., $i_{Carm}(t)$. The value of the Thevenin resistance, on the other

hand, varies with the switching functions $\boldsymbol{s}(t)$, which, in turn, necessitates re-triangularization of the admittance matrix every time a switching event occurs. Utilizing the trapezoidal integration method during the discretization process, the equivalent Thevenin resistance of the arm in normal mode, as expressed in the following equation, comprises the on-state resistance of all switches, along with the summation of companion resistances associated inserted capacitors.

$$R_{\text{th}} = NR_{\text{on}} + \left(\frac{\Delta t}{2C_{\text{sm}}} \,/\!/\, R_{\text{Csm}} \right) \times \mathbf{1} \cdot \boldsymbol{s}(t) \tag{13}$$

where Δt denotes the integration time step. In order to overcome this major computational drawback, the terms with $i_{\text{Carm}}(t)$ are discretized with Euler's method of integration, which expresses the integral as a function of the integrand at the previous time step, i. e., $i_{\text{Carm}}(t-\Delta t)$. Note that other terms such as $\boldsymbol{i}_{\text{L}}(t)$ and $\boldsymbol{v}_{\text{b}}(t)$, which do not contribute to creation of the time-varying Thevenin resistance, are discretized with the trapezoidal integration method. The resulting discrete-time model for the arm of the converter is shown in Fig. 11, in which the intermediate variables g_{L}, r_{C}, k_{L}, k_{C}, ***det***, ***A***, ***B***, ***C***, ***D***, ***W***, ***X***, ***Y***, and ***Z*** are explicitly summarized in following equations.

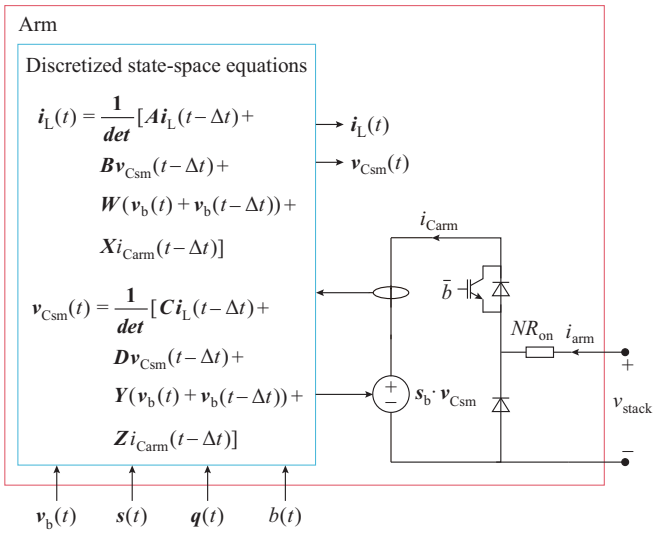

Fig. 11. Discretized model of converter arm using trapezoidal and Euler's integration methods.

$$g_{\text{L}} = \frac{\Delta t}{2L_{\text{sm}}} \tag{14}$$

$$r_{\text{C}} = \frac{\Delta t}{2C_{\text{sm}}} \tag{15}$$

$$k_{\text{L}} = g_{\text{L}}\left(R_{\text{L}} + R'_{\text{on}}\right) \tag{16}$$

$$k_{\text{C}} = \frac{r_{\text{C}}}{R_{\text{Csm}}} \tag{17}$$

$$\boldsymbol{det} = \left(1+k_{\text{L}}\right)\left(1+k_{\text{C}}\right)\mathbf{1} + g_{\text{L}} r_{\text{C}}\left(\mathbf{1} - \boldsymbol{q}(t)\right) \tag{18}$$

$$\boldsymbol{A} = \left(1-k_{\text{L}}\right)\left(1+k_{\text{C}}\right)\mathbf{1} - g_{\text{L}} r_{\text{C}}\left(\mathbf{1} - \boldsymbol{q}(t)\right)\left(\mathbf{1} - \boldsymbol{q}(t-\Delta t)\right) \tag{19}$$

$$\boldsymbol{B} = \left(1+k_{\text{L}}\right)\left(1+k_{\text{C}}\right)\mathbf{1} + g_{\text{L}} r_{\text{C}}\left(\mathbf{1} - \boldsymbol{q}(t)\right) \tag{20}$$

$$\boldsymbol{C} = r_{\text{C}}\left(\left(1+k_{\text{L}}\right)\left(\mathbf{1} - \boldsymbol{q}(t-\Delta t)\right) + \left(1-k_{\text{L}}\right)\left(\mathbf{1} - \boldsymbol{q}(t)\right)\right) \tag{21}$$

$$\boldsymbol{D} = \left(1+k_{\text{L}}\right)\left(1-k_{\text{C}}\right)\mathbf{1} - g_{\text{L}} r_{\text{C}}\left(\mathbf{1} - \boldsymbol{q}(t)\right)\left(\mathbf{1} - \boldsymbol{q}(t-\Delta t)\right) \tag{22}$$

$$\boldsymbol{W} = g_{\text{L}}\left(1+k_{\text{C}}\right)\mathbf{1} \tag{23}$$

$$\boldsymbol{X} = -2g_{\text{L}} r_{\text{C}}\left(\mathbf{1} - \boldsymbol{q}(t)\right)\boldsymbol{s}_{\text{b}}(t-\Delta t) \tag{24}$$

$$\boldsymbol{Y} = \left(1+k_{\text{L}}\right)\left(1+k_{\text{C}}\right)\mathbf{1} + g_{\text{L}} r_{\text{C}}\left(\mathbf{1} - \boldsymbol{q}(t)\right) \tag{25}$$

$$\boldsymbol{Z} = g_{\text{L}} r_{\text{C}}\left(\mathbf{1} - \boldsymbol{q}(t)\right) \tag{26}$$

Note that except for the dot notation for dot products, all other mathematical operations such as addition, multiplication, and division are performed element-wise on arrays. Evidently, there is no term including $i_{\text{Carm}}(t)$ in the expansion of the product $\boldsymbol{s}_{\text{b}}(t) \cdot \boldsymbol{v}_{\text{Csm}}(t)$ that could have otherwise been manifested as an external Thevenin resistor.

It is also worth mentioning that the value of the voltage source in Fig. 11 is known at the present time and can be found from the previous values of the states. Hence, the symbol of an independent voltage source is used in the figure.

Note that in addition to terminal voltage and current of stack of SMs, all other state variables such as SM capacitor voltages and BESS inductor currents are fully accessible during simulation.

The accuracy of the model utilizing the mixed integration method remains unaffected for simulation of MMCs, as demonstrated in [24], despite theoretical superiority of the trapezoidal method over Euler's method.

IV. DC-DC Converter Control

DC-DC converters are usually used to obtain a stabilized output voltage from a given input DC voltage. The regulated DC output voltage is achieved by modulating the widths of the pulses by which the switches turn on and off. This method is called pulse width modulation (PWM) wherein the duty cycle, as a controlling signal, is compared with a high-frequency saw-tooth carrier to generate the gate pulses. In a well-controlled converter, the output voltage is regulated regardless of the loading and variations in the input voltage. However, in the proposed topology, the output voltage of the DC-DC converter, i.e., the voltage of the SM capacitor, shall remain within a limited range for proper operation of the MMC. If the total DC voltage across the HVDC link is V_{dc}, the average voltage of each capacitor will be around V_{dc}/N regardless of the presence of BESS in some sub-modules. On the other hand, the input port of each DC-DC converter is connected to a battery, which is a voltage source in essence. Therefore, in the DC-DC converter under examination, both the input and output ports of each converter function as DC voltage sources. This implies that the duty cycle must remain constant if the converter is considered ideal. Even when considering non-idealities such as the series resistance of the inductor and the on-state resistance of the switches, the range within which the duty cycle can vary is small, thus preventing any substantial control via duty cycle adjustments. In such circumstances, current-control techniques can be employed to regulate the DC-DC converter. In

this scenario, the inductor current serves as an independent variable, enabling the regulation of the power transfer to or from each battery.

The method used in this paper is the peak current mode (PCM) control [25] wherein the peak of the inductor current, which is the same as the peak of the switch current, is bounded. The circuit diagram of PCM control method of DC-DC converter is illustrated in Fig. 12. In this circuit, the rising edge of the clock pulse with the switching period of T_s sets the SR-latch and turns on Q_1. Consequently, the inductor current starts to rise until it reaches the given peak value i_{ctrl} when the comparator resets the SR-latch; this turns on Q_2 and causes the inductor current to fall until the next rising edge of the clock pulse is issued which starts the next period of switching. It is worth mentioning that a hysteresis-type current controller may also be used to regulate the inductor current that yields similar effects on the overall system performance provided that the inductor current ripple component is neglected. However, the switching frequency is not constant as in PCM control and may vary depending on the state of batteries and the converter.

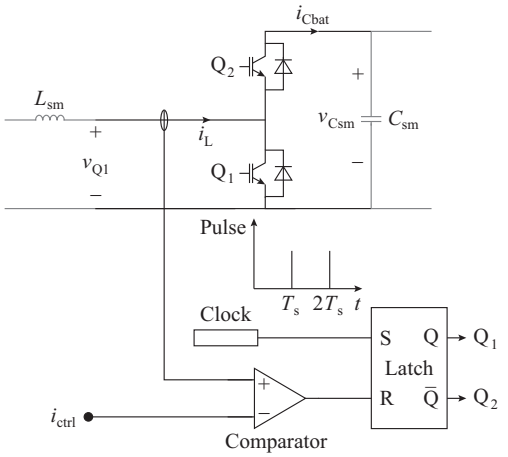

Fig. 12. Circuit diagram of PCM control of DC-DC converter.

V. Simulation Case Study

In this section, the proposed model DEM is used in EMT simulation of a large HVDC system to demonstrate the functionalities of the MMC-BESS. The case study focuses mainly on the converter-level responses and waveforms, and ancillary services such as inertial support are not demonstrated. The CIGRE B4-57 MMC-HVDC grid [26], [27] with four MMC stations B2, B3, E1, and F1, as shown in Fig. 13, is considered. Each station includes an MMC (comprising HB SMs) with a rated AC voltage of 220 kV connected to an external AC system via a transformer with the respective turns ratio. All the converters share a common DC voltage rated at 400 kV through HVDC transmission lines (TLs) and cables. Nearest level control (NLC) [28] is used to generate firing pulses for the IGBTs in all converter stations. Furthermore, circulating current suppression control (CCSC) [29] is added to the control circuit of each station for elimination of the second-order harmonics in arm current. Table I highlights specifications of the converters in each station.

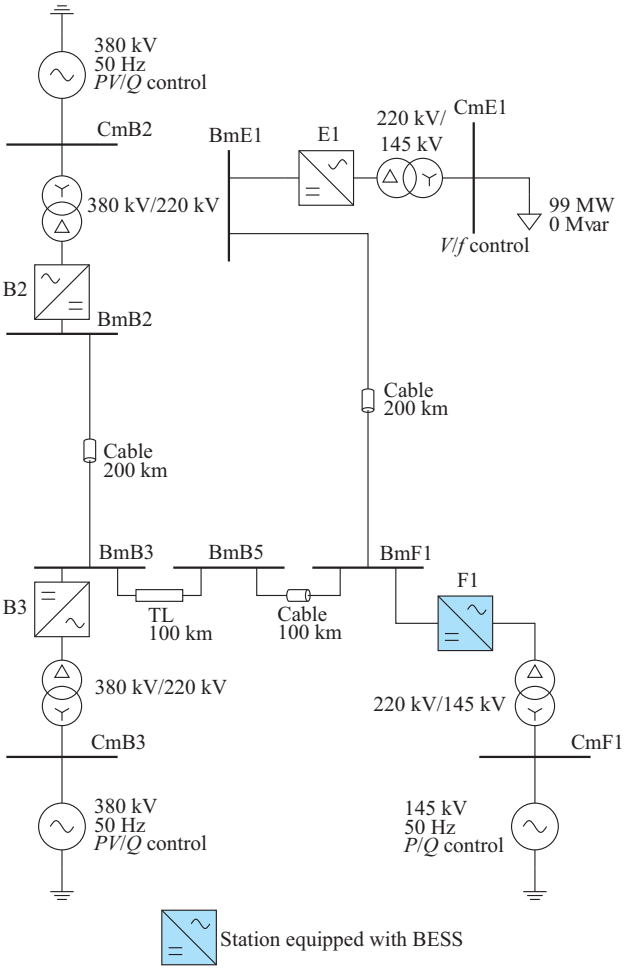

Fig. 13. CIGRE B4-57 MMC-HVDC grid with four MMC stations.

The *dq* reference frame theory [30] is employed as the main control scheme in each station, which is shown in Fig. 14. In Fig. 14, P represents the active power, Q represents the reactive power, and V_{dc} represents the DC voltage. The quantities V_{abc} and i_{abc} correspond to the three-phase voltages and currents, respectively, while θ is the phase angle measured by the phase-locked loop (PLL). Additionally, $V_{ac\text{-}rms}$ denotes the root mean square (RMS) voltage on the AC side, and i_d, i_q, v_d, and v_q are the direct and quadrature components of the three-phase currents and voltages, respectively. All variables with a superscript * indicate their corresponding reference values. However, generation of the reference *dq* currents and/or voltages varies from station to station. At bus CmE1, the voltage magnitude and frequency are regulated since it operates in the islanded mode with a fixed load on its AC side. The bus CmF1 is a *P*/*Q*-controlled bus whose reference *dq* currents are produced by outer loops regulating the active and reactive power with respective reference values. Both buses CmB2 and CmB3 are *PV*/*Q*-controlled with the same strategy used in the bus CmF1 except that the reference active power is augmented by the DC voltage deviation from its rated value multiplied by a droop coefficient so that the DC voltage drops as DC power delivered towards the DC hub is increased.

TABLE I
SPECIFICATIONS OF CONVERTERS

Converter	Rated power (MW)	BESS included	Number of CONV-SMs	Number of BESS-SMs	SM capacitance (mF)	Capacitor leakage resistance (MΩ)	Switch on resistance (mΩ)	Arm inductance (mH)	Transformer voltage ratio (kV/kV)	Transformer leakage reactance (p.u.)	Transformer copper loss (p.u.)
B2	800	No	200	0	10.0	10	1	29	380/220	0.18	0.006
B3	1200	No	200	0	15.0	10	1	19	380/220	0.18	0.006
E1	200	No	200	0	2.5	10	1	116	145/220	0.18	0.006
F1	800	Yes	200	100	10.0	10	1	29	145/220	0.18	0.006

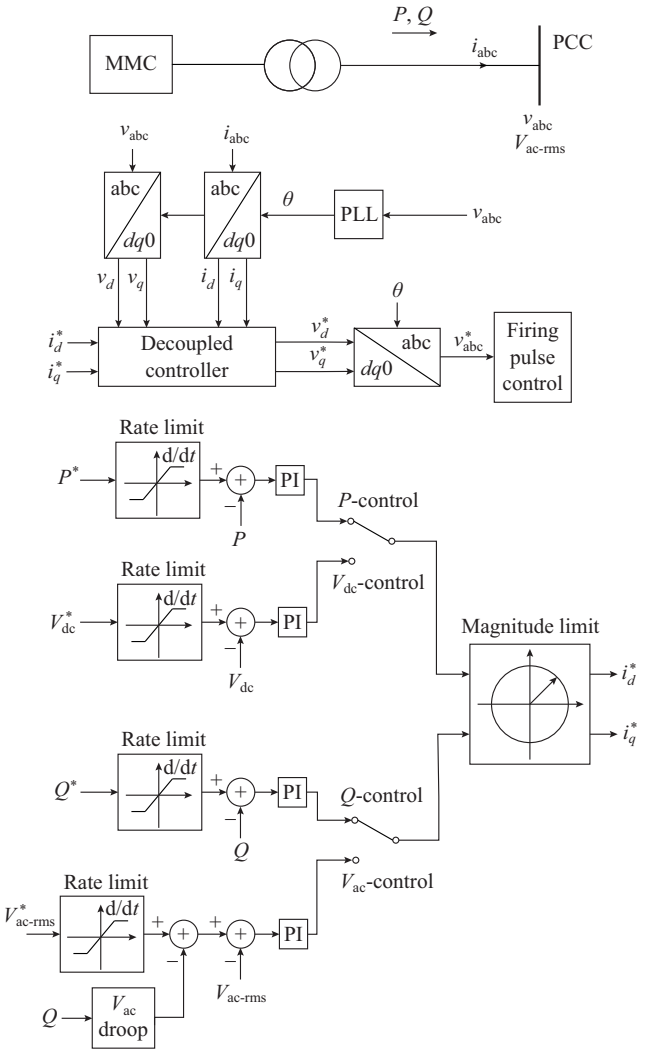

Fig. 14. Control block diagram of MMC.

The control of BESS is largely independent from the control modes of the MMC due to two main reasons. Firstly, the DC voltage regulation is managed by the MMC, which incorporates sorting and balancing algorithms. BESS does not engage in this control mode as it does not attempt to regulate sub-module voltage via feedback control loops. Secondly, reactive power and/or AC voltage are regulated either by modulation index or the imaginary component of the current in the decoupled *dq* reference frame, with BESS integration exerting minimal influence on this control mode. Active power is the sole variable modulated by the injection or absorption of battery power. The adjustment of battery power commands (or battery current) is then dictated by the chosen control function, which may originate from frequency control or inertial support mechanisms.

The converter F1 is equipped with BESS. It consists of 200 HB SMs, half of which are upgraded to include batteries and DC-DC converters. For simplicity, the battery is modeled with a DC voltage behind an internal resistor with values of 1.2 kV and 1.0 mΩ, respectively. DC-DC converters are operated under the PCM control wherein the peak current is determined based on the power command, to be either injected or absorbed, and battery's specifications. Note that the peak current is approximately the same as the battery's average current thanks to the relatively high-inductance reactor of the DC-DC converter. The DC-DC converter's inductor is 0.1 H with series resistance of 1.0 mΩ, which is switched with the frequency of 2 kHz. All simulations are executed with the time step of 10 μs.

A. Injection and Absorption of Power by Batteries

Initially, the converter F1 delivers 500 MW to the DC side without drawing active power from the batteries. Once steady state is achieved, a demand for 72 MW of power from the batteries is initiated at $t=2$ s, while maintaining the power command of the AC system at bus CmF1 at 500 MW, along with other AC buses. Subsequently, at $t=3$ s, the batteries are instructed to charge with the same power. Figures 15, 16, and 17 depict the DC voltage, power at the DC terminals of the four converter stations, and the total battery power at the converter F1, respectively. Despite operating in both charging and discharging modes, the DC voltage at each bus remains within a range of 0.025 p.u.. However, the DC power varies based on the bus type and control mode of each station. While the DC power aligns with the power command from the batteries at the bus BmF1, the power at the bus BmE1 remains constant due to its fixed AC-side load. Consequently, the surplus power from the batteries, either +72 MW starting at $t=2$ s or −72 MW starting at $t=3$ s, is distributed among stations CmB2 and CmB3 according to their respective power/voltage droop characteristics.

B. Arm-level Waveforms

Figure 18 shows the arm currents and the average SM capacitor voltages in the top and bottom arms of the MMC-BESS. These waveforms are taken while the batteries are charged with the peak current order of 100. Note that the differential current, which is the same as AC terminal current, exhibits sinusoidal behavior.

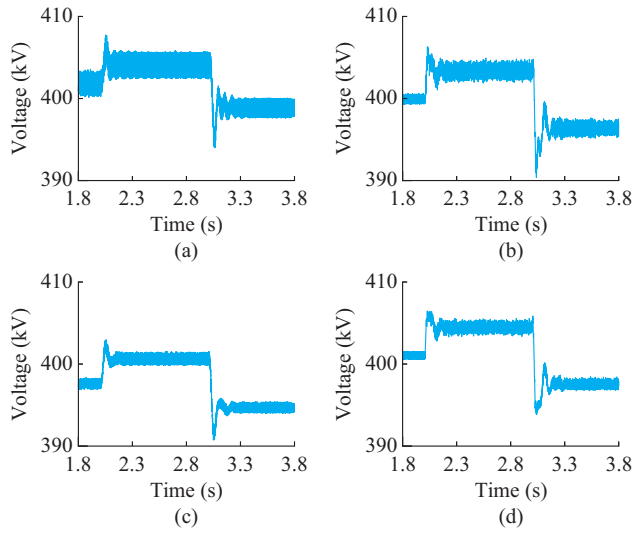

Fig. 15. DC voltage at DC terminals of converter stations. (a) BmB2. (b) BmE1. (c) BmB3. (d) BmF1.

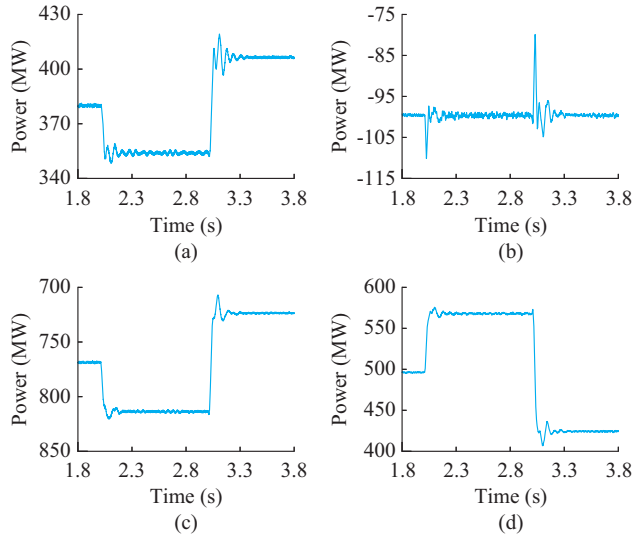

Fig. 16. Power at DC terminals of converter stations. (a) BmB2. (b) BmE1. (c) BmB3. (d) BmF1.

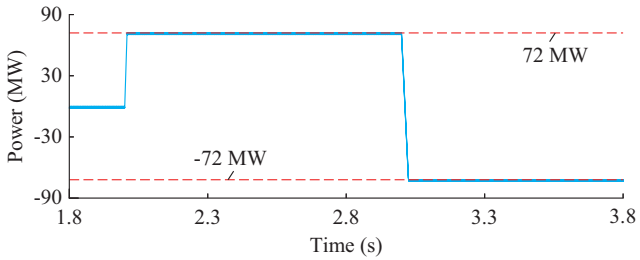

Fig. 17. Total battery power.

Conversely, the circulating current is constant. Thus, the arm currents are nearly completely sinusoidal with a DC offset because of the operation of the circulating current suppression controller.

It is also noted that the average voltages across capacitors of CONV-SMs and BESS-SMs are slightly different due to the inherent topological asymmetry.

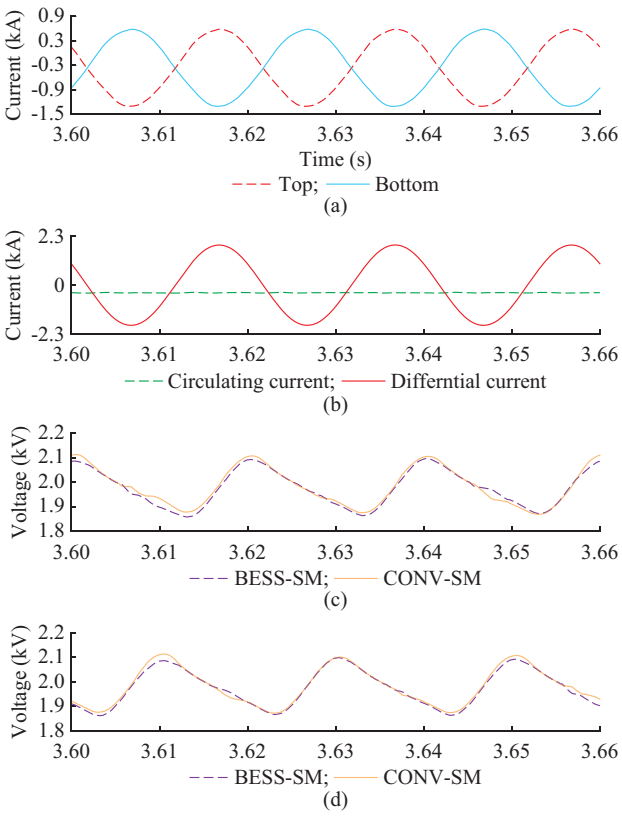

Fig. 18. Arm currents, circulating and differential currents, and average voltages across CONV-SMs and BESS-SMs. (a) Arm currents. (b) Circulating and differential currents. (c) Average of voltages across CONV-SM capacitors. (d) Average of voltages across BESS-integrated SM capacitors.

C. Response of Battery Currents

The steady-state current waveforms of sample batteries from the top and bottom arms are depicted along with the commanded peak current in Fig. 19. As shown in Fig. 19, the battery current (which is the same as the inductor current of DC-DC converter) rises up at the beginning of a switching period until it reaches the commanded peak current (100 A in this case). Reaching the peak value, the inductor current starts to fall until the next switching period starts. It is evident that the average inductor current (99 A in this case) is close to the peak current and the difference is often neglected.

The transient responses of the battery (inductor) currents to a step change in the commanded peak current from 100 A to −100 A are shown in Fig. 20 for two representative batteries. They both quickly settle into the requested steady state, with a settling time that is influenced by the inductance of DC-DC converter.

D. Pole-to-pole (PTP) DC Fault

At $t=2$ s, a PTP DC fault is applied at the bus BmF1. The fault is detected when the magnitude of DC current exceeds 6 kA, and a blocking signal is issued after 30 μs. Subsequently, after 2 cycles (40 ms), the AC-side breakers open. This blocking and tripping scheme is implemented for all stations. Figure 21 illustrates the DC current of each converter. It is important to note that the measured current direction is toward the DC hub.

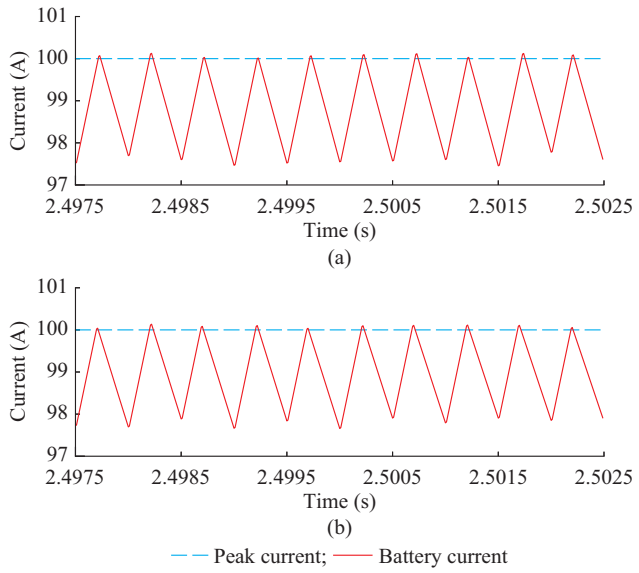

Fig. 19. Steady-state current waveforms of batteries. (a) Top arms. (b) Bottom arms.

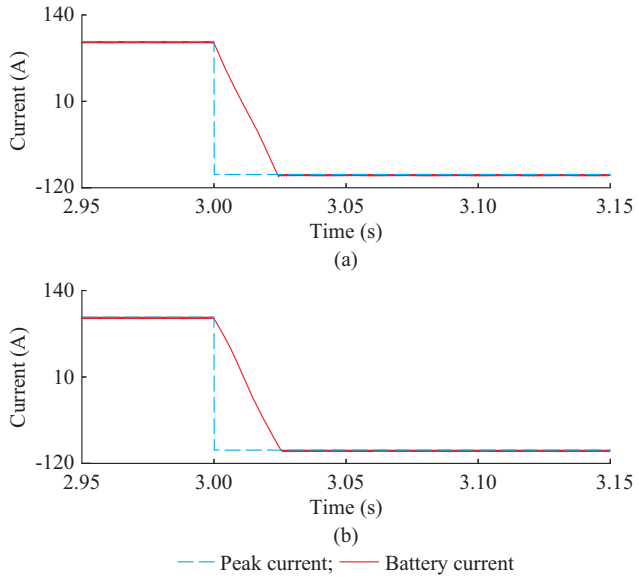

Fig. 20. Transient responses of battery currents to a step change in commanded peak current. (a) Sample battery current from the top arm. (b) Sample battery current from the bottom arm.

It is evident that the current increases immediately after the fault occurrence. Subsequently, all converters are blocked, while the AC breakers have not yet disconnected the stations from their AC sides. Consequently, the AC sides contribute to the DC fault current, as depicted in Fig 22. However, it is worth mentioning that the AC side of converter CmE1 does not contribute to the fault current since it operates in islanded mode, with a passive load on its AC side.

VI. Computational Efficiency of Proposed Model

This section studies computational efficiency of the proposed model. The performance of the proposed model is compared against that of DSM wherein the MMC-BESS is built with individual switching elements, i.e., IGBTs, diodes, and passive elements.

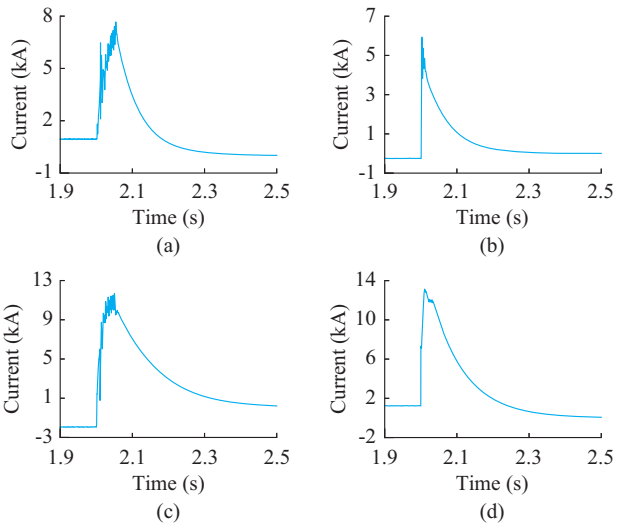

Fig. 21. DC currents under PTP DC fault at bus BmF1. (a) BmB2. (b) BmE1. (c) BmB3. (d) BmF1.

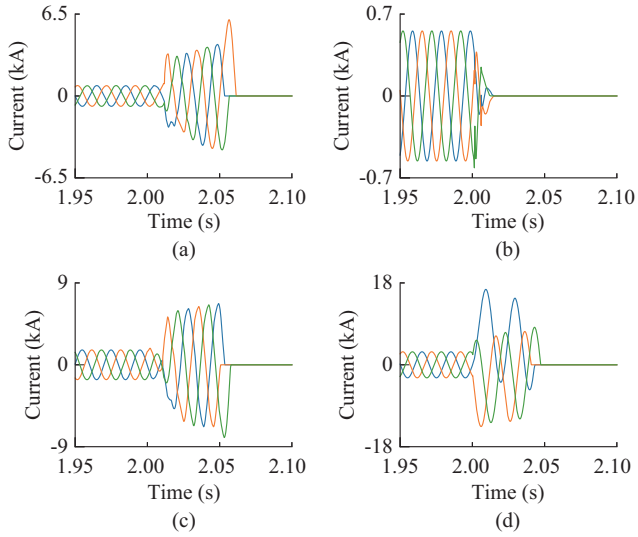

Fig. 22. AC currents under PTP DC fault at bus BmF1. (a) BmB2. (b) BmE1. (c) BmB3. (d) BmF1.

A three-phase MMC with fully-integrated BESS supplying a three-phase RL load is considered, as shown in Fig. 23. The simulation is carried out by changing the number of SMs in each run. Note that the peak current is set to be zero and the SM capacitance is updated so that the equivalent arm capacitance $C_{\text{arm}} = C_{\text{sm}}/N$ remains constant at 600 μF. The battery voltage is also modified for each case so that the ratio of the battery voltage to that of the SM capacitor is kept constant at 0.6. The inductance and switching frequency of the DC-DC converter are set to be 9 mH and 1 kHz, respectively. Each case is simulated for 1 s with the time step of 50 μs in the PSCAD/EMTDC simulator on a computer with Intel Core i7-12700 2.10 GHz CPU and 32 GB installed RAM. To remove the impact of plotting on the CPU run time, all graphs are removed after having validated the accuracy of waveforms. Figure 24 shows the CPU run time versus the number of SMs for the DSM and the proposed DEM. It is evident that the run time grows exceedingly large

with the number of SMs for DSMs while it stays essentially constant for the proposed model. Practical MMC-BESS circuits will have considerably larger SM counts, so that the computational efficiency of the proposed model is anticipated to be orders of magnitude compared with this illustrative example, which is better than a DSM for practical MMC-BESSs.

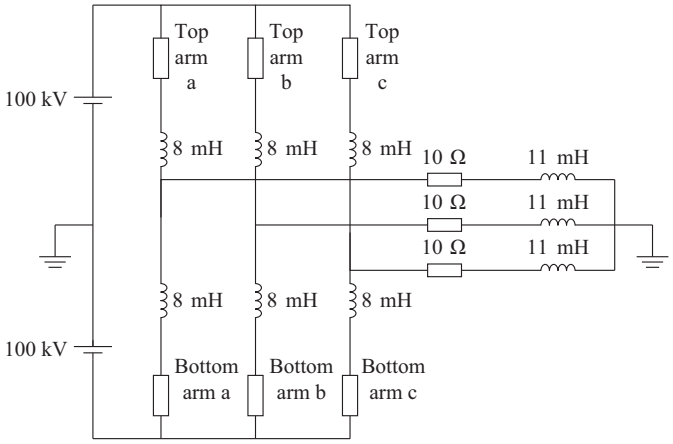

Fig. 23. Case study for computational efficiency.

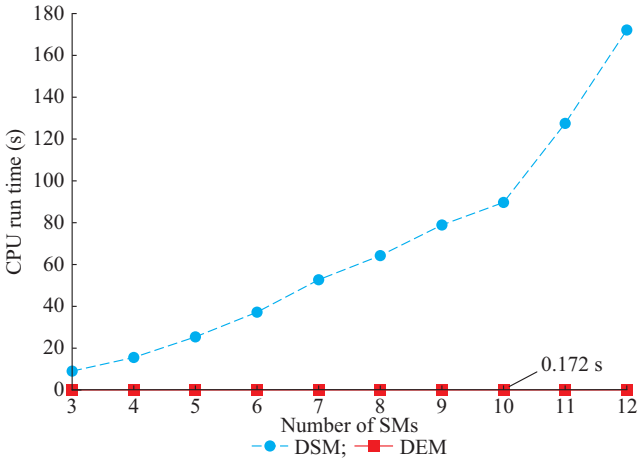

Fig. 24. CPU run time versus number of SMs.

VII. Experimental Validation

Presently there is no commercially available DEM for the MMC-BESS that could be used for accuracy cross-validation. Thus, this section validates the accuracy of the proposed model by comparing its results against those obtained from a down-scaled single-phase prototype of an MMC-BESS. Figure 25 depicts the schematic diagram of the developed test-bed shown in Fig. 26. In Fig. 25, R_{load} and L_{load} are the load resistance and inductance, respectively. Table II shows the specifications and parameters of the experimental setup.

The NLC method for pulse generation is used for firing the switches in each arm. For sorting and balancing of capacitor voltages as well as measurement and monitoring, waveforms including arm currents, SM capacitor voltages, battery voltages, and battery currents are measured and interfaced with the signal measurement unit through analog-to-digital conversion.

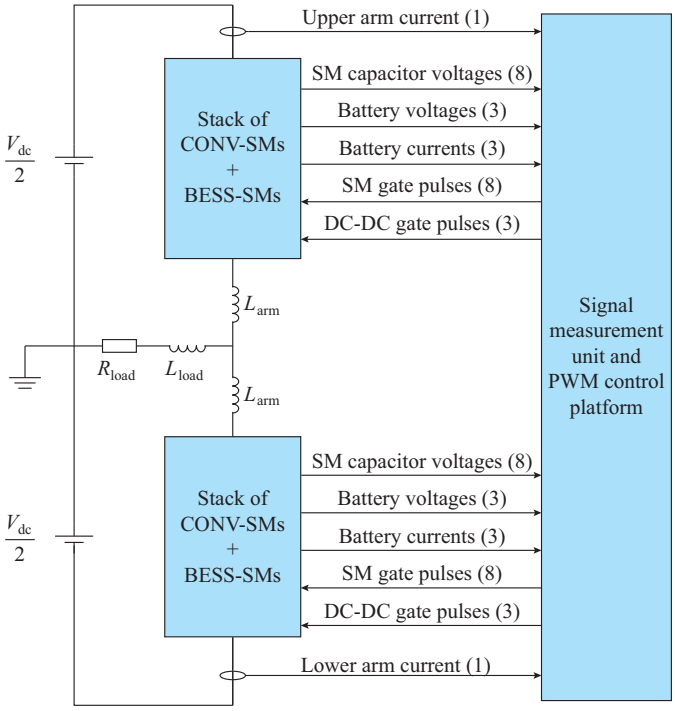

Fig. 25. Schematic diagram of experimental setup.

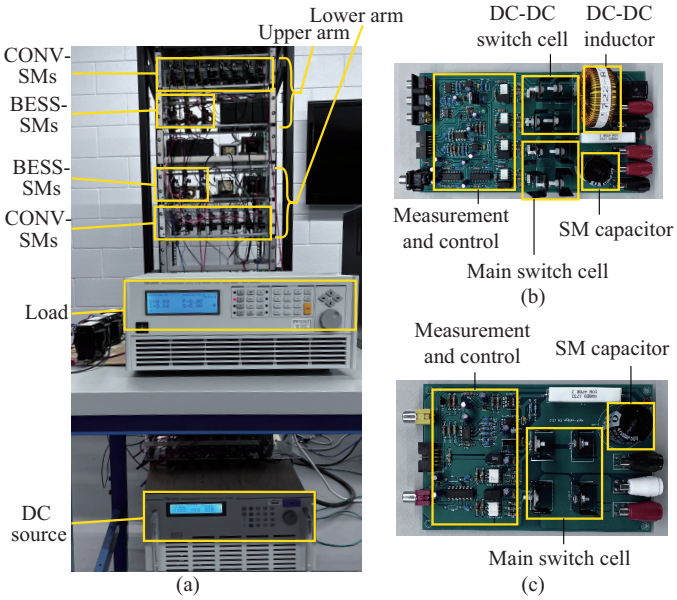

Fig. 26. Experimental testbed. (a) Experimental setup. (b) BESS-SM. (c) CONV-SM.

The gate pulses for all switches are then generated and sent back to the MMC-BESS hardware via PWM generation platform. A 1 kHz anti-aliasing filter is used for each low-frequency analog signal in order to eliminate the noises associated with analog-to-digital conversion.

A model of the experimental setup is built in the PSCAD/EMTDC simulator using the proposed model. The simulation time step is set to be 10 μs. Figures 27 and 28 compare low-frequency steady-state waveforms from the experimental setup against those produced by the proposed model for two battery current commands $I_{ctrl} = 1$ A (discharging) and $I_{ctrl} = -0.8$ A (charging), respectively.

TABLE II
PARAMETERS OF EXPERIMENTAL SETUP

Parameter	Value
Total number of SMs per arm	8
Number of BESS-SMs per arm	3
DC link voltage (V)	200
SM capacitance (μF)	4700
Modulation index	0.95
AC voltage frequency (Hz)	60
DC-DC converter switching frequency (kHz)	10
Arm inductance (mH)	8
DC-DC converter inductance (μH)	900
Load inductance (mH)	10
Load resistance (Ω)	10.24
Battery nominal voltage (V)	12
Battery capacity (Ah)	7

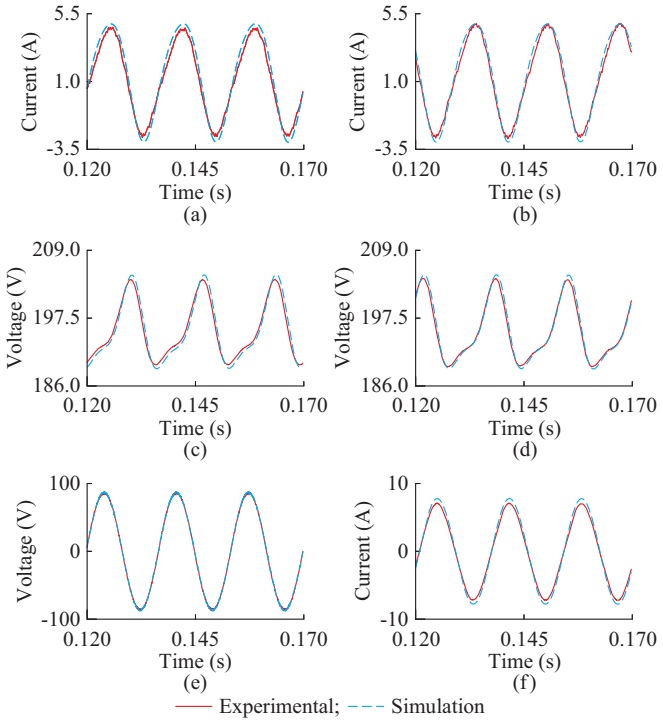

Fig. 27. Low-frequency steady-state waveforms with $I_{ctrl}=1$ A (discharging). (a) Top arm current. (b) Bottom arm current. (c) Sum of top capacitor voltages. (d) Sum of bottom capacitor voltages. (e) Terminal voltage. (f) Load current.

The comparison clearly shows that both simulation and experimental waveforms follow each other closely. Note that RMS errors calculated for voltage and current waveforms of Figs. 27 and 28 are less than 0.5% and 10%, respectively. The higher error in current measurement stems from two reasons. Firstly, it is impractical to precisely adjust the power supply for the hall effect sensor to obtain an exact value. Secondly, the arm and load inductors are not accurately measured and modeled. These components exhibit nonlinearity, and their inductance varies with current. However, in the simulation, they are treated as fixed linear inductors.

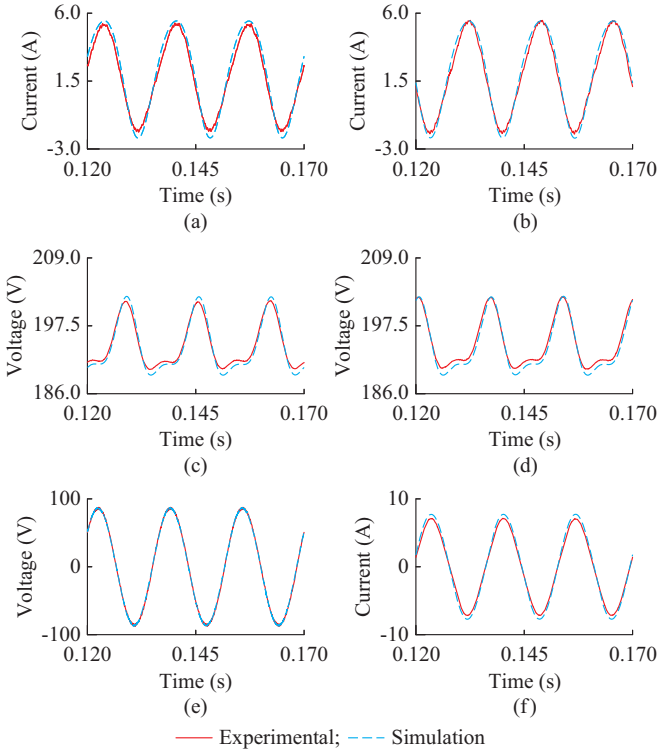

Fig. 28. Low-frequency steady-state waveforms with $I_{ctrl}=-0.8$ A (charging). (a) Top arm current. (b) Bottom arm current. (c) Sum of top capacitor voltages. (d) Sum of bottom capacitor voltages. (e) Terminal voltage. (f) Load current.

The transient responses of the DC current to step changes in the reference peak current are also shown in Fig. 29. In this experiment, the DC current is achieved by passing the circulating current into a first-order filter with a time constant of 0.1 s to eliminate the second- and higher-order harmonics. As shown in Fig. 29, the DC current decreases when the reference peak current of the battery (or inductor) is increased and vice versa. Furthermore, the results of simulations and experiments show excellent conformity.

VIII. CONCLUSION

A novel detailed equivalent model was introduced for EMT simulation of MMCs with partially-integrated BESS. The proposed model offers significant reductions in computational load by diminishing the number of nodes that are interconnected to other nodes in the structure of the MMC. Except when blocking is invoked, the proposed model eliminates time-varying electrical conductances, thereby avoiding re-factorization of the admittance matrix; this further helps its computational efficiency. State variables such as SM capacitor voltages and DC-DC inductor currents are also computed and are accessible for control purposes such as NLC modulation and battery current control. To study the performance of the MMC-BESS, the PCM control strategy is introduced by which the battery current, and hence its power is controlled with a simple circuitry. Different operation modes such as charging, discharging, and idle modes can be prompted by adjusting the peak current to a positive value, negative value, and zero, respectively.

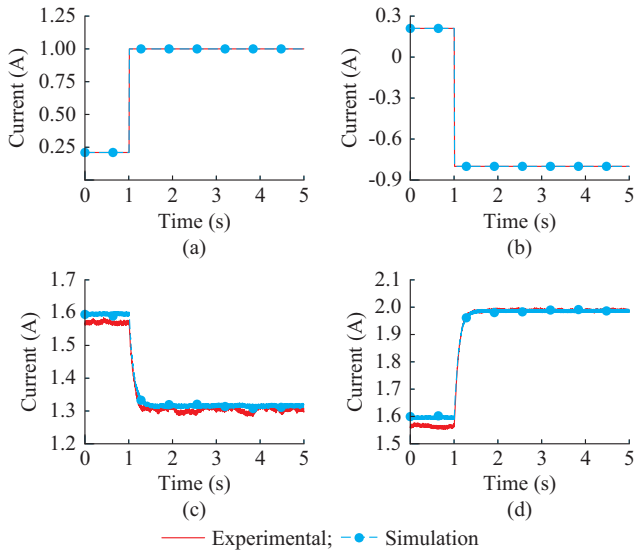

Fig. 29. Responses of DC current to step changes in reference peak current. (a) Positive peak current step change. (b) Negative peak current step change. (c) DC current response to positive step change. (d) DC current response to negative step change.

Moreover, PCM adds a protection layer to limit the current of the battery and DC-DC converter switches. The computational advantage of the proposed model is demonstrated against a conventional DSM, and it is observed that orders of magnitude improvement in computational efficiency are achieved. The accuracy of the proposed model is validated using experimental results from a single-phase down-scaled version of the MMC-BESS.

REFERENCES

[1] J. Rocabert, R. Capó-Misut, R. S. Muñoz-Aguilar *et al*., "Control of energy storage system integrating electrochemical batteries and supercapacitors for grid-connected applications," *IEEE Transactions on Industry Applications*, vol. 55, no. 2, pp. 1853-1862, Mar. 2019.

[2] H. Bevrani, A. Ghosh, and G. Ledwich, "Renewable energy sources and frequency regulation: survey and new perspectives," *IET Renewable Power Generation*, vol. 4, no. 5, pp. 438-457, Aug. 2010.

[3] I. Serban and C. Marinescu, "Control strategy of three-phase battery energy storage systems for frequency support in microgrids and with uninterrupted supply of local loads," *IEEE Transactions on Power Electronics*, vol. 29, no. 9, pp. 5010-5020, Sept. 2014.

[4] S. M. Lukic, J. Cao, R. C. Bansal *et al*., "Energy storage systems for automotive applications," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 6, pp. 2258-2267, Jun. 2008.

[5] B. Dunn, H. Kamath, and J. M. Tarascon, "Electrical energy storage for the grid: a battery of choices," *Science*, vol. 334, no. 6058, pp. 928-935, Nov. 2011.

[6] M. Świerczyński, D. I. Stroe, A. I. Stan *et al*., "Selection and performance-degradation modeling of $LiMO_2/Li_4Ti_5O_{12}$ and $LiFePO_4$/C battery cells as suitable energy storage systems for grid integration with wind power plants: an example for the primary frequency regulation service," *IEEE Transactions on Sustainable Energy*, vol. 5, no. 1, pp. 90-101, Jan. 2014.

[7] D. I. Stroe, V. Knap, M. Swierczynski *et al*., "Operation of a grid-connected lithium-ion battery energy storage system for primary frequency regulation: a battery lifetime perspective," *IEEE Transactions on Industry Applications*, vol. 53, no. 1, pp. 430-438, Jan. 2017.

[8] J. Fang, H. Li, Y. Tang *et al*., "On the inertia of future more-electronics power systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 4, pp. 2130-2146, Dec. 2019.

[9] H. Bevrani, T. Kato, T. Ise *et al*., *Grid Connected Converters*, Amsterdam: Elsevier, 2022.

[10] F. Díaz-González, A. Sumper, and O. Gomis-Bellmunt, *Modeling, Control, and Simulation*. West Sussex: John Wiley & Sons, 2016, pp. 163-208.

[11] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Proceedings of 2003 IEEE Bologna PowerTech Conference*, Bologna, Italy, Jun. 2003, pp. 1-6.

[12] B. Gemmell, J. Dorn, D. Retzmann *et al*., "Prospects of multilevel VSC technologies for power transmission," in *Proceedings of 2008 IEEE PES Transmission and Distribution Conference and Exposition*, Chicago, USA, Apr. 2008, pp. 1-16.

[13] M. Schroeder and J. Jaeger, "The idea of a modular multilevel converter with integrated batteries," in *Proceedings of 2012 International Conference on Smart Grid Technology, Economics and Policies*, Nuremberg, Germany, Dec. 2012, pp. 1-6.

[14] A. Lachichi, "Modular multilevel converters with integrated batteries energy storage," in *Proceedings of 2014 International Conference on Renewable Energy Research and Application*, Milwaukee, USA, Oct. 2014, pp. 828-832.

[15] M. Vasiladiotis and A. Rufer, "Analysis and control of modular multilevel converters with integrated battery energy storage," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 163-175, Jan. 2015.

[16] P. D. Judge and T. C. Green, "Modular multilevel converter with partially rated integrated energy storage suitable for frequency support and ancillary service provision," *IEEE Transactions on Power Delivery*, vol. 34, no. 1, pp. 208-219, Feb. 2019.

[17] H. Dommel and B. P. Administration, *Electromagnetic Transients Program Reference Manual: (EMTP) Theory Book*. Bonneville: Bonneville Power Administration, 1986.

[18] U. N. Gnanarathna, A. M. Gole, and R. P. Jayasinghe, "Efficient modeling of modular multilevel HVDC converters (MMC) on electromagnetic transient simulation programs," *IEEE Transactions on Power Delivery*, vol. 26, no. 1, pp. 316-324, Jan. 2011.

[19] N. Herath, S. Filizadeh, and M. S. Toulabi, "Modeling of a modular multilevel converter with embedded energy storage for electromagnetic transient simulations," *IEEE Transactions on Energy Conversion*, vol. 34, no. 4, pp. 2096-2105, Dec. 2019.

[20] M. Saeedifard and R. Iravani, "Dynamic performance of a modular multilevel back-to-back HVDC system," *IEEE Transactions on Power Delivery*, vol. 25, no. 4, pp. 2903-2912, Oct. 2010.

[21] N. Ahmed, L. Ängquist, S. Mahmood *et al*., "Efficient modeling of an MMC-based multiterminal DC system employing hybrid HVDC breakers," *IEEE Transactions on Power Delivery*, vol. 30, no. 4, pp. 1792-1801, Aug. 2015.

[22] N. Herath and S. Filizadeh, "Improved average-value and detailed equivalent models for modular multilevel converters with embedded storage," *IEEE Transactions on Energy Conversion*, vol. 37, no. 3, pp. 1998-2008, Sept. 2022.

[23] M. M. Bhesaniya and A. Shukla, "Norton equivalent modeling of current source MMC and its use for dynamic studies of back-to-back converter system," *IEEE Transactions on Power Delivery*, vol. 32, no. 4, pp. 1935-1945, Aug. 2017.

[24] R. Parvari, S. Filizadeh, and D. Muthumuni, "An accelerated detailed equivalent model for modular multilevel converters," *Electric Power Systems Research*, vol. 223, pp. 109648-109655, Oct. 2023.

[25] R. W. Erickson and D. Maksimović, *Current-programmed Control, Fundamentals of Power Electronics*. Cham: Springer International Publishing, 2020, pp. 725-804.

[26] T. Vrana, S. Dennetiere, Y. Yang *et al*., "The CIGRÉ B4 DC grid test system," *CIGRE Electra*, vol. 270, pp. 10-19, Oct. 2013.

[27] Manitoba Hydro International. (2023, May). CIGRE B4-57 Working Group developed models. [Online]. Available: https://www.pscad.com/knowledge-base/article/57

[28] K. Sharifabadi, L. Harnefors, H. P. Nee *et al*., *Modulation and Submodule Energy Balancing*. West Sussex: Wiley-IEEE Press, 2016, pp. 232-271.

[29] B. Bahrani, S. Debnath, and M. Saeedifard, "Circulating current suppression of the modular multilevel converter in a double-frequency rotating reference frame," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 783-792, Jan. 2016.

[30] A. Yazdani and R. Iravani, *Space Phasors and Two-dimensional Frames*. Hoboken: Wiley-IEEE Press, 2010, pp. 69-114.

Ramin Parvari received the B.Sc. degree in electrical engineering from the University of Tabriz, Tabriz, Iran, in 2012, and the M.Sc. degree in electrical engineering from Sharif University of Technology, Tehran, Iran, in 2014. He is currently pursuing a Ph.D. degree in electrical engineering at the Uni-

versity of Manitoba, Winnipeg, Canada. His research interests include electromagnetic transient simulation, modeling and control of modular multilevel converters, and integration of grid-scale battery energy storage systems.

Shaahin Filizadeh received the B.Sc. and M.Sc. degrees in electrical engineering from Sharif University of Technology, Tehran, Iran, in 1996 and 1998, respectively, and the Ph.D. degree from the University of Manitoba, Winnipeg, Canada, in 2004. He is currently a Professor with the Department of Electrical and Computer Engineering, University of Manitoba. He is a Registered Professional Engineer in the Province of Manitoba. His research interests include electromagnetic transient simulation and power electronics.

Ioni Fernando is employed with Manitoba Hydro in the Grid Infrastructure Planning Department. She holds a B.Sc. (Eng.) degree with first class honors from the University of Moratuwa, Moratuwa, Sri Lanka and a Ph.D. degree from the University of Manitoba, Winnipeg, Canada. She is an Adjunct Professor in the Department of Electrical and Computer Engineering, University of Manitoba, Senior Member of IEEE and a Professional Engineer in the Province of Manitoba. Her research interests include HVDC system, power system stability, system protection, and electromagnetic transient simulation.