Maximum Loadability Evaluation Method for Multi-voltage-level DC Distribution Network with DC Electric Springs

Xiaolong Xu, Qianggang Wang, *Senior Member*, *IEEE*, Jianquan Liao, *Member*, *IEEE*, Yuan Chi, *Member*, *IEEE*, Tao Huang, *Senior Member*, *IEEE*, Niancheng Zhou, *Senior Member*, *IEEE*, Yiyao Zhou, and Xuefei Zhang

***Abstract*—The multi-voltage-level DC distribution network (MVL-DC-DN) is a promising network for efficiently integrating rapidly growing DC loads, and fast-growing load demand would bring a challenge to the MVL-DC-DN in terms of the maximum loadability. This paper considers the DC electric spring (DC-ES) as a novel candidate flexible resource for enhancing the maximum loadability of the MVL-DC-DN, and proposes an evaluation method for the maximum loadability. Firstly, with the consideration of device constraints, the impact that the DC-ES on the maximum loadability of the DC distribution network (DC-DN) is analyzed via a simplified equivalent circuit. Subsequently, the power flow (PF) model of an MVL-DC-DN with DC-ESs is established. Finally, a method based on continuation power flow (CPF) for evaluating the maximum loadability of an MVL-DC-DN with DC-ESs is proposed. During the evaluation, limitations of the DC-ES and the DC transformer (DCT) are considered. The consideration of the practical constraints avoids the overestimation of the maximum loadability. The case study verifies the effectiveness of the proposed method.**

***Index Terms*—DC electric spring, loadability, DC distribution network, continuation power flow (CPF).**

NOMENCLATURE

A. Symbols

S_{1es}-S_{4es}	Switches of DC electric spring (DC-ES)
S_{1D}-S_{8D}	Switches of dual active bridge (DAB)
S_{pass}	Bypass switch of DC-ES
S_1-S_3	Interconnection switches

B. Sets

E	Set of buses with a type of V
E'	Set of buses with a type of V_{es}
E''	Set of buses with a type of P
N	Set of all buses
S	Set of swing buses

C. Parameters

σ	Step size for continuation power flow (CPF)
C	Filter capacitor in DC-ES
C_{1D}, C_{2D}	Capacitors in DAB
E_{dc}	Electromotive force of energy storage device in DC-ES
f_s	Switching frequency of DAB
I_{lim}	Current limitation of DC transformer (DCT)
L	Filter inductance in DC-ES
L_D	Auxiliary inductance of DAB
n_h	Turn ratio of high-frequency AC transformer in DAB
n_c	Controlled turn ratio between primary and secondary sides of DCT
P_L^{ini}	Initial power sum of non-critical load (NL) and critical load (CL)
P_{NL}^{ini}	Initial power of NL
P_{CL}^{ini}	Initial power of CL
P_b	Baseline load power
P_{es}^{rate}	Rated power capability of DC-ES
R	Line resistance
T_s	Switching period of switches in DAB
V_{DC}	Output voltage of DC voltage source
V_{es}^{lim}	Output voltage limit of DC-ES
x	A constant value equaling to 1 or −1

Manuscript received: February 21, 2024; revised: June 15, 2024; accepted: August 22, 2024. Date of CrossCheck: August 22, 2024. Date of online publication: September 13, 2024.

This work was supported in part by the National Natural Science Foundation of China (No. 52077017).

X. Xu, Q. Wang (corresponding author), Y. Chi, N. Zhou, Y. Zhou, and X. Zhang are with the State Key Laboratory of Power Transmission Equipment Technology, Chongqing University, Chongqing, China (e-mail: xuxiaolong@cqu.edu.cn; qianggang1987@cqu.edu.cn; chiyuanee@cqu.edu.cn; cee_nczhou@cqu.edu.cn; yiyaozhou@cqu.edu.cn; zhangxuefei@cqu.edu.cn).

J. Liao is with the College of Electrical Engineering, Sichuan University, Chengdu, China (e-mail: jquanliao@scu.edu.cn).

T. Huang is with the Department of Energy, Politecnico di Torino, Torino, Italy (e-mail: tao.huang@polito.it).

DOI: 10.35833/MPCE.2024.000187

Y_{loss} Equivalent power loss admittance of DCT

D. Variables

α Proportion of increased NL power relative to total increased power, within 0-1

α_i α for bus i

λ Load parameter

$\lambda^{\max}$ Load parameter corresponds to the maximum load power a network can afford

λ^{p} Prediction value of λ

D Phase shift of DAB

f_i Mismatch power for bus i

i_{L} Filter inductance current

i_{LD} Current on auxiliary inductance of DAB

i, j Index numbers of buses

I_{DC} DC current on distribution line

n_1, n_2 Indexes of elements in vectors $\boldsymbol{V}_{\text{es}}^{\lim}$ and $\boldsymbol{\alpha}$

P_{L} Power sum of CL and NL

$P_{\text{L}}^{\max}$ The maximum load power a network can afford

P_{NL} Power of NL

P_{CL} Power of CL

$P_{\text{NL},i}$ Power of NL on bus i

$P_{\text{b},i}$ Baseline load power of bus i

$P_{\text{L},i}$ Load power of bus i

P_{es} Power of DC-ES

P_{tran} Power transferred by DAB

R_{sr} Resistance between sending and receiving buses

$R_{i-1,i}$ Branch resistance between bus $i-1$ and i

v_1, v_2 Voltages on primary and secondary sides of AC high-frequency transformer in DAB

V_{es} Voltage of DC-ES

$V_{\text{es},i}$ Voltage of DC-ES on bus i

$V_{\text{es},i}^{\lim}$ Voltage limitation of DC-ES on bus i

V_{target} Target voltage maintained by DC-ES

V_i Voltage of bus i

$V_{1\text{D}}$, $V_{2\text{D}}$ Voltages on primary and secondary sides of DAB

V_s, V_r Voltages of sending and receiving buses

Y_{ij} Element in the i^{th} row and j^{th} column of admittance matrix of a DC distribution network (DC-DN)

Y_{ij}^{mod} Element in the i^{th} row and j^{th} column of admittance matrix of a multi-voltage-level DC distribution network (MVL-DC-DN)

$Y_{ij}^{\text{I/O}}$ Element in the i^{th} row and j^{th} column of input/output matrix of DCT

E. Vectors and Matrices

$\boldsymbol{\alpha}$ Vector of proportion for increased NL power relative to total increased power

$\boldsymbol{\alpha}^{\text{diag}}$ Diagonal matrix with $\boldsymbol{\alpha}$ as diagonal elements

$\Delta\boldsymbol{C}$ Vector of correction amount

$\boldsymbol{e}_k$, $\boldsymbol{e}_s$, $\boldsymbol{e}_r$, $\boldsymbol{e}_m$ Row vectors whose elements equal to 0 except the k^{th}, s^{th}, r^{th}, or m^{th} elements equal to 1

$\boldsymbol{f}$ Mismatch vector of power for buses

$\boldsymbol{f}_\lambda$ Vector of partial derivative for $\boldsymbol{f}$ with respect to λ

$\boldsymbol{f}_{\lambda,\text{I}}$ Matrix of partial derivative for $\boldsymbol{f}$ with respect to λ in Stage I

$\boldsymbol{f}_{\lambda,\text{II}}$ Matrix of partial derivative for $\boldsymbol{f}$ with respect to λ in Stage II

$\boldsymbol{f}_{\lambda,\text{III}}$ Matrix of partial derivative for $\boldsymbol{f}$ with respect to λ in Stage III

$\boldsymbol{f}_V$ Matrix of partial derivative for $\boldsymbol{f}$ with respect to bus voltage

$\boldsymbol{f}_{V,\text{I}}$ Matrix of partial derivative for $\boldsymbol{f}$ with respect to voltage in Stage I

$\boldsymbol{f}_{V,\text{II}}$ Matrix of partial derivative for $\boldsymbol{f}$ with respect to voltage in Stage II

$\boldsymbol{f}_{V,\text{III}}$ Matrix of partial derivative for $\boldsymbol{f}$ with respect to voltage in Stage III

$\boldsymbol{J}_{\text{I}}$ Jacobian matrix in Stage I

$\boldsymbol{J}_{\text{II}}$ Jacobian matrix in Stage II

$\boldsymbol{J}_{\text{III}}$ Jacobian matrix in Stage III

$\boldsymbol{J}_{\text{CLV}}$ Jacobian matrix for current limitation violation

$\boldsymbol{P}_{\text{es}}^{\text{rate}}$ Vector of rated power capability for DC-ESs

$\boldsymbol{P}_{\text{L}}$ Vector of load power

$\boldsymbol{P}_{\text{NL}}$ Vector of NL power

$\boldsymbol{P}_{\text{b}}$ Vector of baseline load power

$\boldsymbol{V}_{\text{es}}^{\lim}$ Vector of DC-ES output voltage limit

$\boldsymbol{V}$ Vector of bus voltage

$\boldsymbol{V}_{\text{es}}$ Vector of DC-ES voltage

$\boldsymbol{V}^{\text{diag}}$ Diagonal matrix with $\boldsymbol{V}$ as diagonal elements

$\boldsymbol{V}_{\text{es}}^{\text{diag}}$ Diagonal matrix with $\boldsymbol{V}_{\text{es}}$ as diagonal elements

$\boldsymbol{V}^{\text{p}}$ Vector of predicted bus voltage

$\boldsymbol{Y}^{\text{I/O}}$ Input/output matrix of DCT

$\boldsymbol{Y}$ Admittance matrix of a DC-DN

$\boldsymbol{Y}^{\text{mod}}$ Admittance matrix of an MVL-DC-DN

$\boldsymbol{Y}_j^{\text{mod}}$ Vector formed by the i^{th}-row elements of $\boldsymbol{Y}^{\text{mod}}$

I. Introduction

In recent years, more and more DC loads are integrated into distribution networks (DNs) [1], [2]. Demand for various voltage levels has promoted the development of multi-voltage-level DC distribution networks (MVL-DC-DNs) [3], and the networks with different voltage levels are interconnected by DC transformers (DCTs). The MVL-DC-DN is also effective for integrating distributed generations (DGs). Nevertheless, DGs can have negative impacts on MVL-DC-DNs, such as deterioration of power quality [4], [5]. In addition, fast-growing DC loads also bring challenges to MVL-DC-DNs, in terms of the maximum loadability. The DC electric spring (DC-ES) [6] is a promising candidate resource to address these problems. Although scholars have conducted

comprehensive research focusing on applications of the DC-ES such as voltage regulation [7], DG consumption [8], and harmonic cancellation [9], the application of the DC-ES for enhancing the maximum loadability of MVL-DC-DNs is yet to be explored. The maximum loadability is a prevalent indicator of a network and a static voltage collapse occurs when the maximum loadability is exceeded [10].

The DC-ES is typically connected in series with a non-critical load (NL) [6] to form a smart load, and then connected in parallel with a critical load (CL) [6], [11], [12]. Consumed power of the smart load can be regulated by controlling output voltage of the DC-ES, thereby maintaining the voltage of the CL [13], [14]. Given the excellent performance in MVL-DC-DNs, DC-ESs are expected to be widely deployed in the future and play an important role. Consequently, with the ability to inject power [6], DC-ESs would be significant resources for enhancing the maximum loadability. On this basis, evaluating how much the maximum loadability can be enhanced by DC-ESs becomes a necessary research problem.

Common methods for evaluating the maximum loadability of a network are summarized in Table I. The evaluation methods can be categorized into the optimization-based method and bifurcation analysis method. The optimization-based method aims to determine the maximum load power that the network can support under various constraints, which are typically formulated and solved using methods such as second-order cone programming (SOCP) [15], semi-definite programming (SDP) [16], sequential convex programming (SCP) [17], and non-linearity programming (NLP) [18]. These methods usually perform a high efficiency in term of calculation. However, they do not develop a comprehensive model, failing to capture details in voltage stability [17]. These details may be helpful for future works during the evaluation process such as weak branch identification.

TABLE I
SUMMARY OF COMMON METHODS FOR EVALUATING MAXIMUM LOADABILITY

Method	Technique	Advantage	Disadvantage
Optimization-based method	SOCP, SDP	High flexibility in modeling operational constraints	Accuracy of optimal solution depends on accuracy of relaxation
	SCP	High accuray	Low computing efficiency
	NLP	No transformation is required on the model	Easy to fall into local optima
Bifurcation analysis method	DM	Light calculation burden	Cannot handle inequality constraints or identify type of bifurcation point
	CPF	High accuracy and details in voltage stability can be captured	Convergence highly depends on search step size and parameter selection

The bifurcation analysis method is another way to evaluate the maximum loadability [19], including the direct method (DM) [20] and the continuation power flow (CPF) method [21]. The DM aims to evaluate the maximum loadability via direct calculation of a saddle node bifurcation point (SNBP), but it cannot identify the limit induced bifurcation point (LIBP). The LIBP is usually caused by limitations of power sources (or devices working as power sources) and it can easily lead to a voltage collapse [22]. In MVL-DC-DNs, current limitations of DCTs for protection purpose are easily triggered and result in an LIBP under a heavy load condition. Consequently, the application of the DM is limited by this phenomenon.

As for the CPF method, it is a homotopy-idea-based method that tracks the entire solution manifolded through predictive-corrective iterations [21]. In [23], the CPF method is used to evaluate and compare the maximum loadability of the DC distribution network (DC-DN) and the MVL-DC-DN. The result indicates that the MVL-DC-DN outperforms the DC-DN in terms of the maximum loadability. Compared with optimization-based methods, the CPF method provides more accurate results because it retains the original constraints. Additionally, the CPF method develops a comprehensive model that reflects details in voltage stability and does not have the problem of local optima. In terms of bifurcation identification, it can effectively identify an LIBP by checking the limitations after a corrective iteration.

However, research on CPF methods regarding an MVL-DC-DN with DC-ESs has been rare. During the CPF, as the load power increases, the voltage limitations of DC-ESs will be triggered and the bus voltages cannot be maintained. At this moment, bus types are changed. Bus type conversion would extremely complicate the corrective iterations, and even lead to an incorrect evaluation. Moreover, the treatment of DCTs whose current limitations are triggered is also an issue that should be considered, as the expected external characteristics of them are also changed. To address the above-mentioned issues, this paper proposes an evaluation method based on CPF for the maximum loadability of an MVL-DC-DN with DC-ESs. The major contributions of this paper are summarized as follows.

1) An evaluation method based on CPF for the maximum loadability of an MVL-DC-DN with DC-ESs is proposed. The output voltage and power capability limitations of the DC-ES and the current limitations for the DCT are considered. The consideration of practical constraints effectively prevents the network from collapsing caused by overestimating the maximum loadability.

2) Type conversion logic of buses deployed with a DC-ES is analyzed. This logic is analyzed by watching how the limitations of the DC-ES are triggered as the load goes up. This logic helps the corrective iterations directly determine the conversion type for a bus with fewer judgment procedures.

3) As a novel resource, the DC-ES is adopted to enhance the maximum loadability of MVL-DC-DNs. Impacts of two elements (i.e., voltage limitation of DC-ES and power of NL connecting in series with DC-ES) on enhancing the maximum loadability are analyzed. This analysis can provide a reference for planning DC-ESs in MVL-DC-DNs.

The rest of this paper is organized as follows. In Section II, the impact of the DC-ES on the maximum loadability of DC-DN is analyzed. In Section III, power flow (PF) models of both the MVL-DC-DN and the MVL-DC-DN with DC-

ESs are established. In Section IV, the evaluation method for the maximum loadability of an MVL-DC-DN with DC-ESs is described. In Section V, the results of case study are shown and analyzed. Section VI concludes this paper with the final remarks.

II. Impact of DC-ES on Maximum Loadability of DC-DN

A simplified equivalent circuit of a DC-DN with a DC-ES is illustrated in Fig. 1. The DC-ES functions as a controllable voltage source to maintain the bus voltage. Note that all of the loads in this paper are modeled as pure constant power loads.

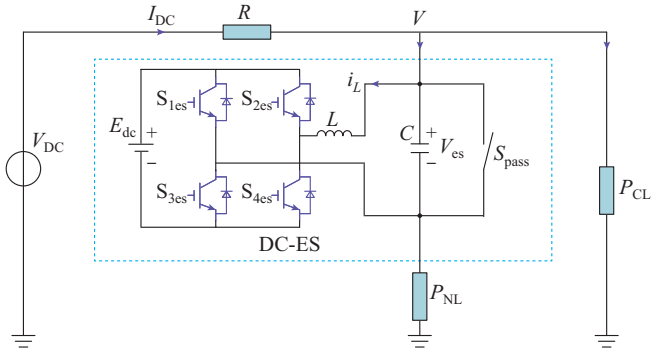


Fig. 1. Simplified equivalent circuit of DC-DN with DC-ES.

When the bus voltage V is maintained to be V_{target}, the load power of the simplified network is expressed as:

$$\begin{cases} P_L = \dfrac{V_{DC} - V_{target}}{R} V_{target} - P_{es} \\ P_{es} = \dfrac{P_{NL} V_{es}}{V_{target} - V_{es}} \end{cases} \tag{1}$$

Equation (1) indicates that an increase of the load power results in a bigger output voltage amplitude and output power of the DC-ES, thus maintaining the bus voltage.

A. Maximum Loadability Without Considering Rated Power Capability of DC-ES

Under a heavy load power, the output voltage of the DC-ES will reach its limit, and the bus voltage cannot be maintained anymore. The output power of the DC-ES is described as:

$$P_{es} = \frac{V_{es}^{lim}(\alpha\lambda P_b + P_{NL}^{ini})}{V - V_{es}^{lim}} \tag{2}$$

The partial derivatives of P_{es} with respect to V and λ are written as:

$$\begin{cases} \dfrac{\partial P_{es}}{\partial V} = -\dfrac{V_{es}^{lim}(\alpha\lambda P_b + P_{NL}^{ini})}{(V - V_{es}^{lim})^2} > 0 \\ \dfrac{\partial P_{es}}{\partial \lambda} = \dfrac{\alpha P_b V_{es}^{lim}}{V - V_{es}^{lim}} < 0 \end{cases} \tag{3}$$

Equation (3) indicates that the output power of the DC-ES increases with the load power even when the output voltage of the DC-ES is limited.

The maximum loadability of the simplified circuit can be expressed as:

$$\begin{cases} P_L^{ini} + \lambda^{max} P_b = \dfrac{V(V_{DC} - V)}{R} - \dfrac{V_{es}^{lim}(\alpha\lambda^{max} P_b + P_{NL}^{ini})}{V - V_{es}^{lim}} \\ P_L^{ini} = P_{NL}^{ini} + P_{CL}^{ini} \end{cases} \tag{4}$$

λ^{max} is expressed as (5) by rewritten (4).

$$\lambda^{max} = \frac{-V^3 + V^2(V_{es}^{lim} + V_{DC}) - V(V_{es}^{lim} V_{DC} + RP_L^{ini})}{P_b R(\alpha V_{es}^{lim} + V - V_{es}^{lim})} + \frac{RV_{es}^{lim}(P_L^{ini} - P_{NL}^{ini})}{P_b R(\alpha V_{es}^{lim} + V - V_{es}^{lim})} \tag{5}$$

The partial derivatives of λ^{max} with respect to V_{es}^{lim} and α are expressed as:

$$\frac{\partial \lambda^{max}}{\partial V_{es}^{lim}} = V \frac{\alpha\left[\dfrac{V(V - V_{DC})}{R} + P_L^{ini}\right] - P_{NL}^{ini}}{P_b[(\alpha - 1)V_{es}^{lim} + V]^2} \tag{6}$$

$$\frac{\partial \lambda^{max}}{\partial \alpha} = -V_{es}^{lim}\left[\frac{-V^3 + V^2(V_{es}^{lim} + V_{DC})}{P_b R(\alpha V_{es}^{lim} + V - V_{es}^{lim})^2} + \frac{-V(V_{es}^{lim} V_{DC} + RP_L^{ini}) + RV_{es}^{lim}(P_L^{ini} - P_{NL}^{ini})}{P_b R(\alpha V_{es}^{lim} + V - V_{es}^{lim})^2}\right] \tag{7}$$

$\left|V(V - V_{DC})/R\right| > P_L^{ini}$ is always satisfied before V_{es}^{lim} is reached. Thus, $\partial\lambda^{max}/\partial V_{es}^{lim}$ is negative. This means that the maximum loadability of the network can be further enhanced by the DC-ES with a bigger $\left|V_{es}^{lim}\right|$, and a bigger α leads to a similar result.

Furthermore, the second-order partial derivatives of λ^{max} with respect to V_{es}^{lim} and α are expressed as:

$$\frac{\partial^2 \lambda^{max}}{\partial (V_{es}^{lim})^2} = -2V(\alpha - 1)\frac{\alpha\left[\dfrac{V(V - V_{DC})}{R} + P_L^{ini}\right] - P_{NL}^{ini}}{P_b[(\alpha - 1)V_{es}^{lim} + V]^3} \tag{8}$$

$$\frac{\partial^2 \lambda^{max}}{\partial \alpha^2} = 2(V_{es}^{lim})^2\left[\frac{-V^3 + V^2(V_{es}^{lim} + V_{DC})}{P_b R(\alpha V_{es}^{lim} + V - V_{es}^{lim})^2} + \frac{-V(V_{es}^{lim} V_{DC} + RP_L^{ini}) + RV_{es}^{lim}(P_L^{ini} - P_{NL}^{ini})}{P_b R(\alpha V_{es}^{lim} + V - V_{es}^{lim})^2}\right] \tag{9}$$

It is evident that $\partial^2\lambda^{max}/\partial(V_{es}^{lim})^2$ is negative in the negative reference direction, and an increase in V_{es}^{lim} reduces the efficiency for enhancing the maximum loadability. Conversely, the opposite result can be expected for α.

B. Maximum Loadability Considering Rated Power Capability of DC-ES

According to (3), the output power of the DC-ES increases with the power of NLs even when the output voltage of the DC-ES is limited. Usually, to ensure the security of the DC-ES, a rated power capability is set to the DC-ES.

After the rated power of the DC-ES is reached, the DC-ES functions as a constant power source. The maximum loadability of the network is expressed as:

$$\lambda^{max} = \frac{V_s^2}{4RP_b} + \frac{P_{es}^{rate} - P_L^{ini}}{P_b} \tag{10}$$

The partial derivative of λ^{max} with respect to P_{es}^{rate} is ex-

pressed as:

$$\frac{\partial \lambda^{\max}}{P_{\text{es}}^{\text{rate}}} = \frac{1}{P_{\text{b}}} \tag{11}$$

Equations (10) and (11) demonstrate that a larger rated power capability of the DC-ES results in a greater enhanced maximum loadability.

C. Working Mode Conversion Logic of DC-ES

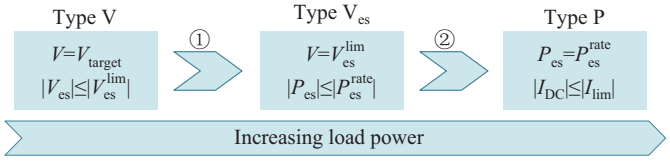
In a DC-DN, during the process of identifying the maximum loadability by constantly increasing the load power, the DC-ES can operate in various modes. Equation (1) demonstrates that, within a light-load range, the bus voltage can be maintained via adjusting the voltage of the DC-ES. While under an overload condition, although the output voltage of the DC-ES is limited, the output power of the DC-ES still increases with the load power. After the rated power capability of the DC-ES is reached, the DC-ES functions as a constant power source. The consumed power of the bus equals to the load power minus the rated power capability of the DC-ES. Therefore, in a DC-DN, the DC-ES could function sequentially as a controllable voltage source, a constant voltage source, and a constant power source, striving to provide the best power injection within its capacity.

According to the analyzed working mode of the DC-ES, three kinds of bus types are defined and listed as follows. And the bus type conversion logic for a bus connected to a DC-ES is illustrated in Fig. 2.

1) Type V: the bus voltage is maintained at a fixed value.

2) Type V_{es}: the voltage of the DC-ES is maintained at a fixed value.

3) Type P: the net load power of the bus is known.



① Voltage limitation violation; ② Power capability violation

Fig. 2. Bus type conversion logic for a bus connected to a DC-ES.

D. Maximum Loadability Considering Current Limitation of DCT

DCT is a power electronic device whose current limitation significantly affects the maximum loadability of an MVL-DC-DN. An insufficient current limitation would be easily exceeded under heavy load conditions. Assume there is a DCT between the power source and the load bus in Fig. 1. Equation (12) yields the maximum loadability of the circuit in Fig. 1 when the current limitation of the DCT is reached.

$$\begin{cases} \lambda^{\max} = -\dfrac{R^2 I_{\text{lim}}^3 + a_2 I_{\text{lim}}^2 + b_2 I_{\text{lim}} + c_2}{P_{\text{b}}[RI_{\text{lim}} + (1-\alpha)V_{\text{es}}^{\text{lim}} - V_{\text{s}}]} \\ a_2 = RV_{\text{es}}^{\text{lim}} - 2RV_{\text{s}} \\ b_2 = RP_{\text{L}}^{\text{ini}} - V_{\text{s}}V_{\text{es}}^{\text{lim}} + V_{\text{s}}^2 \\ c_2 = V_{\text{es}}^{\text{lim}} P_{\text{CL}}^{\text{ini}} - V_{\text{s}} P_{\text{L}}^{\text{ini}} \end{cases} \tag{12}$$

III. PF Models of MVL-DC-DN and MVL-DC-DN with DC-ESs

A. PF Model of DC-DN

The topology of a DC-DN is illustrated in Fig. 3, and the PF model of the DC-DN meets (13).

$$\boldsymbol{V}^{\text{diag}}\boldsymbol{Y}\boldsymbol{V} + \boldsymbol{P}_{\text{L}} = \boldsymbol{0} \tag{13}$$

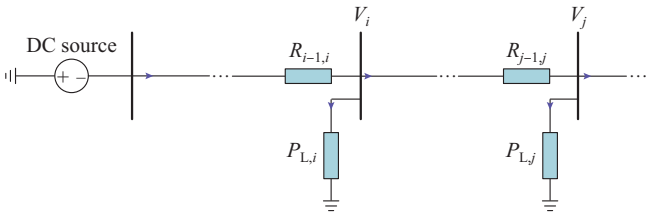


Fig. 3. Topology of a DC-DN.

B. PF Model of MVL-DC-DN

In an MVL-DC-DN, the DCT plays an essential role for power transmission between networks at different voltage levels. DCTs usually adopt the dual active bridge (DAB) topology with a single-phase shift modulation [24]. The topology of a DAB-based DCT is illustrated in Fig. 4. For the DAB-based DCT, the power transmission meets (14).

$$P_{\text{tran}} = \frac{n_{\text{h}} V_{1\text{D}} V_{2\text{D}}}{2 f_{\text{s}} L_{\text{D}}} D(1-D) \tag{14}$$

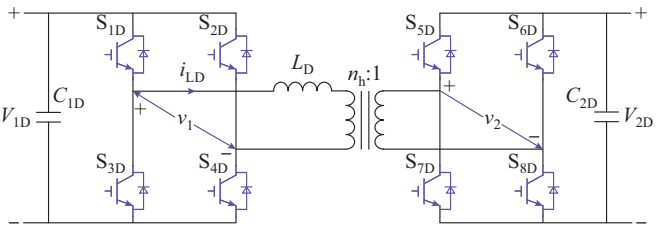


Fig. 4. Topology of a DAB-based DCT.

Comparing with the AC transformer (ACT), the DCT offers more flexible control strategies. For instance, control strategies aim to maintain a constant voltage ratio between the primary and secondary sides of the DCT, as well as a constant output power and a constant output voltage on the secondary side of the DCT [25]. Note that these aims are achieved on the premise that the current of the DCT is within its limitation.

The topology of an MVL-DC-DN is illustrated in Fig. 5.

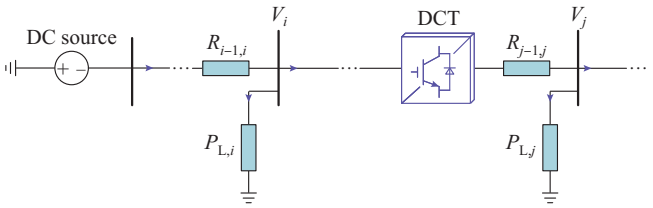


Fig. 5. Topology of an MVL-DC-DN.

In the MVL-DC-DN, the input/output (I/O) matrix of the

DCT is determined by its control strategy. And the PF model of the MVL-DC-DN can be obtained by substituting the I/O matrix into the model of a DC-DN. Assuming that a DCT is deployed between bus i and bus j, and the corresponding PF model is expressed as:

$$\begin{cases} \boldsymbol{V}^{\mathrm{diag}}\boldsymbol{Y}^{\mathrm{mod}}\boldsymbol{V}+\boldsymbol{P}_{\mathrm{L}}=\boldsymbol{0} \\ Y_{ij}^{\mathrm{mod}}=Y_{12}^{\mathrm{I/O}} \\ Y_{ji}^{\mathrm{mod}}=Y_{21}^{\mathrm{I/O}} \\ Y_{ii}^{\mathrm{mod}}=Y_{ii}+Y_{11}^{\mathrm{I/O}}+Y_{ij} \\ Y_{jj}^{\mathrm{mod}}=Y_{jj}+Y_{22}^{\mathrm{I/O}}+Y_{ji} \end{cases} \tag{15}$$

$\boldsymbol{Y}^{\mathrm{I/O}}$ is described in detail in [26]. Note that other elements of $\boldsymbol{Y}^{\mathrm{mod}}$ are equal to those in $\boldsymbol{Y}$.

C. PF Model of MVL-DC-DN with DC-ESs

The topology of an MVL-DC-DN with DC-ESs is illustrated in Fig. 6. Its PF model is expressed as:

$$\boldsymbol{V}^{\mathrm{diag}}\boldsymbol{Y}^{\mathrm{mod}}\boldsymbol{V}+\boldsymbol{P}_{\mathrm{L}}-(\boldsymbol{V}^{\mathrm{diag}}-\boldsymbol{V}_{\mathrm{es}}^{\mathrm{diag}})^{-1}(\boldsymbol{V}_{\mathrm{es}}^{\mathrm{diag}}\boldsymbol{P}_{\mathrm{NL}})=\boldsymbol{0} \tag{16}$$

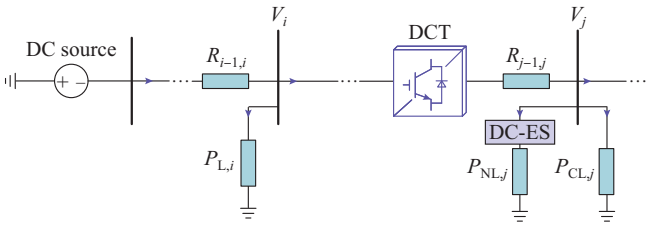


Fig. 6. Topology of an MVL-DC-DN with DC-ESs.

Note that $\boldsymbol{V}_{\mathrm{es}}$ has the same dimension as $\boldsymbol{V}$. If bus i is not deployed with a DC-ES, $V_{\mathrm{es},i}\equiv 0$.

IV. Evaluation Method for Maximum Loadability of MVL-DC-DN with DC-ESs

A. Framework of Proposed Method

The proposed method primarily includes the prediction step and the correction step, which are executed alternately. Limitations of DC-ESs and DCTs are handled in the correction step. After each correction step, the limitations are checked. If any limitation is violated, the corresponding variable is set to its limit. Then, the correction step is re-executed. Once the stopping criterion is satisfied, the evaluation is finished. The framework of the proposed method is illustrated in Fig. 7.

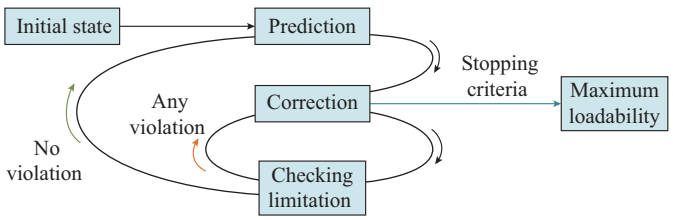


Fig. 7. Framework of proposed method.

B. Prediction Step

During the CPF, an approximate solution for the next PF calculation is obtained in the prediction step by taking a step forward in the direction tangent to the current PF result. The process of the prediction step is described as:

$$\begin{bmatrix} \boldsymbol{V}^{\mathrm{p}} \\ \lambda^{\mathrm{p}} \end{bmatrix}=\begin{bmatrix} \boldsymbol{V} \\ \lambda \end{bmatrix}+\sigma\begin{bmatrix} \Delta\boldsymbol{V} \\ \Delta\lambda \end{bmatrix} \tag{17}$$

$$\begin{bmatrix} \Delta\boldsymbol{V} \\ \Delta\lambda \end{bmatrix}=\begin{bmatrix} \boldsymbol{f}_V & \boldsymbol{f}_\lambda \\ \boldsymbol{e}_k & \end{bmatrix}^{-1}\begin{bmatrix} \boldsymbol{0} \\ x \end{bmatrix} \tag{18}$$

where x equals 1 if the k^{th} element of the vector $[\boldsymbol{V},\lambda]^{\mathrm{T}}$ is λ; otherwise, x equals -1. The proximate solution will be corrected in the correction step.

Note that the selection of the step size σ is essential for the convergence of the CPF. A large value of σ can accelerate the CPF, but increasing the risk of non-convergence near the maximum loadability point. In contrast, a small value of σ can effectively decrease the risk of non-convergence, but slows the process. To balance the convergence and the calculation speed, the value of σ in this paper is defined as follows. In the initial phase, when the bus voltages vary at a slower rate than the load power, a large value of σ is used to accelerate the process. Conversely, when the bus voltages vary at a faster rate than the load power, the value of σ is reduced by dividing a number greater than one, thus facilitating the convergence. The variation speed for both the bus voltages and the load power can be evaluated by conducting a tangent in the direction of increasing load power.

C. Correction Step

The entire evaluation process covers three stages. The definitions of the three stages are listed as follows. Switching conditions for the stages include two criteria: the output voltage and the output power limits of the DC-ES.

Stage I: neither the output voltage nor the output power of the DC-ES has reached the limits.

Stage II: the output voltage of the DC-ES has reached the limit, while the output power has not.

Stage III: both the output voltage and the output power of the DC-ES have reached the limits.

During the correction step, the Jacobian matrices for the three stages are different from each other, but related. After a correction step, if any DC-ES meets the switching conditions, the evaluation switches to the corresponding stage, and is corrected again. Correction steps for the three stages are described as follows.

1) Stage I

In this stage, voltages of the buses deployed with a DC-ES are kept at a fixed value, and the bus type is V. Mismatch vector of power for these buses is expressed as:

$$\begin{cases} \boldsymbol{f}(\boldsymbol{V},\boldsymbol{Y}^{\mathrm{mod}},\boldsymbol{P}_{\mathrm{L}},\boldsymbol{P}_{\mathrm{b}},\lambda)=\boldsymbol{V}^{\mathrm{diag}}\boldsymbol{Y}^{\mathrm{mod}}\boldsymbol{V}+\boldsymbol{P}_{\mathrm{L}}+\lambda\boldsymbol{P}_{\mathrm{b}}-\boldsymbol{A} \\ \boldsymbol{A}=(\boldsymbol{V}^{\mathrm{diag}}-\boldsymbol{V}_{\mathrm{es}}^{\mathrm{diag}})^{-1}[\boldsymbol{V}_{\mathrm{es}}^{\mathrm{diag}}(\lambda\boldsymbol{\alpha}^{\mathrm{diag}}\boldsymbol{P}_{\mathrm{b}}+\boldsymbol{P}_{\mathrm{NL}})] \\ \boldsymbol{V}^{\mathrm{diag}}=diag(\boldsymbol{V}) \\ \boldsymbol{\alpha}^{\mathrm{diag}}=diag(\boldsymbol{\alpha}) \end{cases} \tag{19}$$

where $\boldsymbol{\alpha}$ has a same dimension as $\boldsymbol{V}$. If bus i is not deployed with DC-ESs, $\alpha_i\equiv 0$.

The Jacobian matrix can be obtained according to (19),

which includes three blocks.

$$\boldsymbol{J}_{\mathrm{I}}=\begin{bmatrix}\boldsymbol{f}_{V,\mathrm{I}} & \boldsymbol{f}_{\lambda,\mathrm{I}}\\ \boldsymbol{e}_m & \end{bmatrix} \tag{20}$$

where the subscript m means that the m^{th} element among $[\boldsymbol{V}^{\mathrm{P}},\lambda^{\mathrm{P}}]^{\mathrm{T}}$ is selected as a continuation parameter, with the maximum absolute value among $[\Delta\boldsymbol{V},\Delta\lambda]^{\mathrm{T}}$. When a variable is selected as the continuation parameter, it always equals to its prediction value.

For the buses with type V, their voltages are maintained via adjusting voltages of DC-ESs. In the Jacobian matrix, the column elements, which correspond to the buses deployed with a DC-ES, equal to partial derivatives of the unbalanced power with respect to the voltage of the DC-ES. In this paper, a bus connected to a power source is considered as the swing bus. Row elements corresponding to the swing bus equal to 0, except the diagonal elements equal to 1. Besides, λ is also a variable during the CPF, and the partial derivative of the unbalanced power with respect to λ is included in the Jacobian matrix. Other elements of the Jacobian matrix are the same as elements in a Jacobian matrix of an MVL-DC-DN. Elements of the matrix $\boldsymbol{f}_{V,\mathrm{I}}$ and the vector $\boldsymbol{f}_{\lambda,\mathrm{I}}$ are expressed as:

$$f_{V,\mathrm{I},ij}=\begin{cases}0 & i\neq j,i\in S\|j\in E\\ -V_iB & i=j,j\in E\\ Y_{ij}^{\mathrm{mod}}V_i & i\neq j,i\in N-S,j\notin E\\ 1 & i=j,i\in S\\ Y_{ij}^{\mathrm{mod}}V_i+\boldsymbol{Y}_i^{\mathrm{mod}}\boldsymbol{V} & i=j,i\notin E\cup S,j\notin E\end{cases} \tag{21}$$

$$f_{\lambda,\mathrm{I},i}=P_{\mathrm{b},i}-\alpha_iV_{\mathrm{es},i}P_{\mathrm{b},i}/(V_i-V_{\mathrm{es},i}) \tag{22}$$

$$B=(P_{\mathrm{NL},i}+\lambda\alpha_iP_{\mathrm{b},i})/(V_i-V_{\mathrm{es},i})^2 \tag{23}$$

Corrections for the variables are expressed as:

$$\begin{cases}\Delta\boldsymbol{C}=-\boldsymbol{J}_{\mathrm{I}}^{-1}\begin{bmatrix}\boldsymbol{f} & 0\end{bmatrix}^{\mathrm{T}}\\ f_i=0 \quad i\in S\end{cases} \tag{24}$$

where the elements of $\Delta\boldsymbol{C}$ include both corrections of bus voltages and DC-ES voltages.

2) Stage II

In this stage, the output voltages of some DC-ESs are limited, and these DC-ESs function as constant voltage sources. Their bus types are converted from type V to type $\mathrm{V_{es}}$. The power equations of these buses are the same as (19), and the Jacobian matrix in the compact form is expressed as:

$$\boldsymbol{J}_{\mathrm{II}}=\begin{bmatrix}\boldsymbol{f}_{V,\mathrm{II}} & \boldsymbol{f}_{\lambda,\mathrm{II}}\\ \boldsymbol{e}_m & \end{bmatrix} \tag{25}$$

Since not all buses belonging to set E are converted to type $\mathrm{V_{es}}$ simultaneously, both the types V and $\mathrm{V_{es}}$ could exist in the network. Thus, the Jacobian matrix $\boldsymbol{J}_{\mathrm{II}}$ can be obtained by making some modifications to the Jacobian matrix $\boldsymbol{J}_{\mathrm{I}}$. Column elements corresponding to the buses with the type $\mathrm{V_{es}}$ equal to partial derivatives of the unbalanced power with respect to the bus voltages. Elements of the matrix $\boldsymbol{f}_{V,\mathrm{II}}$ and vector $\boldsymbol{f}_{\lambda,\mathrm{II}}$ are expressed as:

$$f_{V,\mathrm{II},ij}=\begin{cases}Y_{ij}^{\mathrm{mod}}V_i+\boldsymbol{Y}_i^{\mathrm{mod}}\boldsymbol{V}-V_{\mathrm{es},i}B & i=j,i\in E'\\ Y_{ij}^{\mathrm{mod}}V_i & i\neq j,i\in E'\\ f_{V,\mathrm{I},ij} & i\notin E'\end{cases} \tag{26}$$

$$f_{\lambda,\mathrm{II},ij}=P_{\mathrm{b},i}+\alpha_iV_{\mathrm{es},i}P_{\mathrm{b},i}/(V_i-V_{\mathrm{es},i}) \tag{27}$$

$$V_{\mathrm{es},i}=V_{\mathrm{es},i}^{\mathrm{lim}} \quad i\in E' \tag{28}$$

$\boldsymbol{V}_{\mathrm{es}}^{\mathrm{lim}}$ has the same dimension as $\boldsymbol{V}$. If bus i is not deployed with a DC-ES, the corresponding $V_{\mathrm{es},i}^{\mathrm{lim}}\equiv 0$. Corrections for the variables are expressed as:

$$\begin{cases}\Delta\boldsymbol{C}=-\boldsymbol{J}_{\mathrm{II}}^{-1}\begin{bmatrix}\boldsymbol{f} & 0\end{bmatrix}^{\mathrm{T}}\\ f_i=0 \quad i\in S\\ V_{\mathrm{es},i}=V_{\mathrm{es},i}^{\mathrm{lim}} \quad i\in E'\end{cases} \tag{29}$$

3) Stage III

In this stage, the output power of some DC-ESs is limited, and these DC-ESs function as constant power sources. Their bus types are converted from type $\mathrm{V_{es}}$ to type P. The power equations for these buses are expressed as:

$$f_i:(\boldsymbol{V}^{\mathrm{diag}}\boldsymbol{Y}^{\mathrm{mod}}\boldsymbol{V})_i+P_{\mathrm{L},i}+\lambda P_{\mathrm{b},i}+P_{\mathrm{es},i}^{\mathrm{rate}}=0 \quad i\in E'' \tag{30}$$

The Jacobian matrix in the compact form for this stage is expressed as:

$$\boldsymbol{J}_{\mathrm{III}}=\begin{bmatrix}\boldsymbol{f}_{V,\mathrm{III}} & \boldsymbol{f}_{\lambda,\mathrm{III}}\\ \boldsymbol{e}_m & \end{bmatrix} \tag{31}$$

Elements of the vectors $\boldsymbol{f}_{V,\mathrm{III}}$ and $\boldsymbol{f}_{\lambda,\mathrm{III}}$ are expressed as:

$$f_{V,\mathrm{III},ij}=\begin{cases}Y_{ij}^{\mathrm{mod}}V_i+\boldsymbol{Y}_i^{\mathrm{mod}}\boldsymbol{V} & i=j,i\in E''\\ Y_{ij}^{\mathrm{mod}}V_i & i\neq j,i\in E''\\ f_{V,\mathrm{II},ij} & i\notin E''\end{cases} \tag{32}$$

$$f_{\lambda,\mathrm{III},ij}=P_{\mathrm{b},i} \quad i\in E'' \tag{33}$$

Corrections for the variables are expressed as:

$$\begin{cases}\Delta\boldsymbol{C}=-\boldsymbol{J}_{\mathrm{III}}^{-1}\begin{bmatrix}\boldsymbol{f} & 0\end{bmatrix}^{\mathrm{T}}\\ f_i=0 \quad i\in S\\ V_{\mathrm{es},i}=V_{\mathrm{es},i}^{\mathrm{lim}} \quad i\in E'\end{cases} \tag{34}$$

D. Correction for Current Limitation Violation of DCT

After a correction, if a current limitation violation of the DCT occurs, the result should be corrected again. For example, in Stage III, a current limitation violation occurs on the second side of a DCT, then the Jacobian matrix $\boldsymbol{J}_{\mathrm{CLV}}$ is yielded as (30), with a minor modification to $\boldsymbol{J}_{\mathrm{III}}$.

$$\boldsymbol{J}_{\mathrm{CLV}}=\begin{bmatrix}\boldsymbol{f}_{V,\mathrm{III}} & \boldsymbol{f}_{\lambda,\mathrm{III}}\\ Y_{21}^{\mathrm{I/O}}\boldsymbol{e}_s-Y_{22}^{\mathrm{I/O}}\boldsymbol{e}_r & \end{bmatrix} \tag{35}$$

Corrections of the variables are expressed as:

$$\begin{cases}\Delta\boldsymbol{C}=-\boldsymbol{J}_{\mathrm{CLV}}^{-1}\begin{bmatrix}\boldsymbol{f} & 0\end{bmatrix}^{\mathrm{T}}\\ f_i=0 \quad i\in S\\ V_{\mathrm{es},i}=V_{\mathrm{es},i}^{\mathrm{lim}} \quad i\in E'\\ f_{n+1}=V_s/R_{sr}-V_r/R_{sr}-I_{\mathrm{lim}}\end{cases} \tag{36}$$

After that, the current on the second side of the DCT should be kept. And PF model should be corrected according to (14) instead of I/O relationship in (15). The correction

in detail is described based on Fig. 8. Here, a virtual bus with a voltage of V_m is introduced to help form PF model of the DCT.

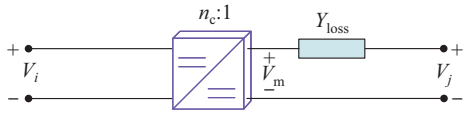


Fig. 8. Equivalent model of DCT.

The PF model of the DCT at this time meets (37).

$$\begin{cases} \dfrac{n_h V_i V_m D(1-D)}{2f_s L_D} + V_i(V_i - V_{i-1})Y_{i-1,i} = 0 \\ (V_m - V_j)V_m Y_{loss} - \dfrac{n_h V_i V_m D(1-D)}{2f_s L_D} = 0 \\ (V_m - V_j)V_j Y_{loss} + (V_j - V_{j+1})Y_{loss} = 0 \\ (V_m - V_j)Y_{loss} - I_{lim} = 0 \end{cases} \tag{37}$$

In (37), four independent equations are established exactly corresponding to four variables, which are voltages on the primary and second sides of the DCT V_i and V_j, virtual bus voltage V_m, and phase shift D. This satisfies the necessary condition under which the PF model of a network is solvable. And the Jacobian matrix should also be reconfigured according to (37).

E. Convergence of Proposed Method

To enhance the convergence performance of the proposed method, three aspects should be focused on under the premise of a solvable PF model.

1) The proposed method is a CPF-based method, which alternately carries the prediction steps and the correction steps upon an initial operation point. It is essentially crucial to find a proper initial iterative point for the convergence of the entire CPF process [27]. A proper initial iterative point can be found according to Lipschitz condition and an inequality condition (Theorem 1 in [27]), and the proof is presented in [28]. Moreover, [29] gives a concise and less conservative convergence condition (Theorem 1), which could provide an easier way to set the initial value to guarantee the convergence.

2) Proper selection of the continuation parameter helps improve the convergence over the whole evaluation process. Near the maximum loadability point, selecting λ as a parameter easily makes power equations unsolvable, leading to non-convergence of the corrective iteration. This is because the predicted load parameter λ^{pre} at this position easily exceeds the critical point. Selecting the bus voltage as a parameter could effectively avoid this issue, since its predicted value at this position and its value at the maximum loadability point are within the same range (initial voltage of 0). Usually, the variable with the largest absolute value among the predictions is selected as the continuation parameter, making the selection adaptive.

3) A proper step size of σ in the prediction step is benefit for improving the convergence. As this topic was previously discussed in Section IV-B, it will not be elaborated upon here.

F. Solution Procedure

Figure 9 illustrates the comprehensive procedure for evaluating the maximum loadability of an MVL-DC-DN with DC-ESs. As mentioned in Section II-A, the output power of a DC-ES increases with the load power even when its voltage is limited. Therefore, during the limitation checking process, the power capability limitation of a DC-ES is checked first. If the power capability limitation of a DC-ES is violated, its voltage violation will not be considered. When $\Delta\lambda^p < 0$ is satisfied, the evaluation is finished.

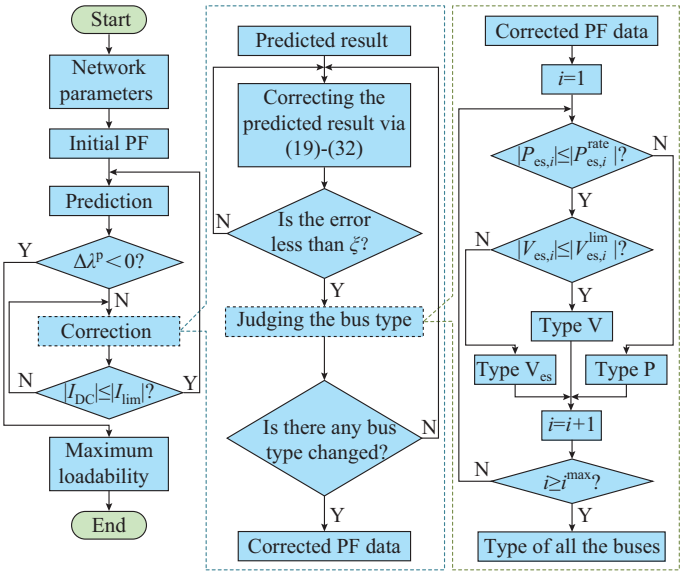


Fig. 9. Comprehensive procedure for evaluating maximum loadability of an MVL-DC-DN with DC-ESs.

V. Case Study

The performance of the proposed method is demonstrated in this section. Simulations are conducted in MATLAB 2018b on a 64-bit computer with a 3.00 GHz CPU and 16 GB RAM. A modified Pacific Gas and Electric Company (PG&E) 69-bus network is adopted as the test network, whose topology is shown in Fig. 10.

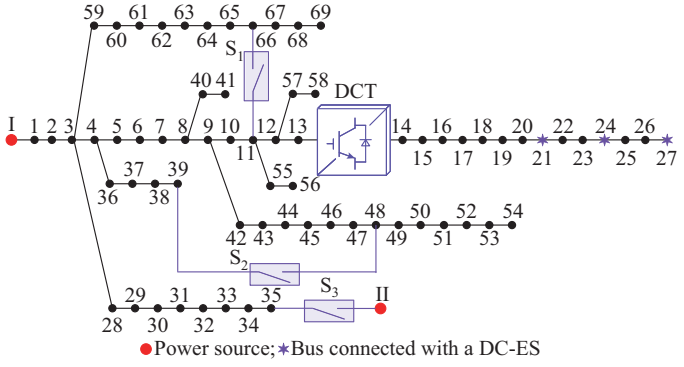


Fig. 10. Topology of modified PG&E 69-bus network.

Note that in the following study, the current limitation of the DCT is assumed to be large enough unless specifically stated. And the interconnection switches S_1, S_2, and S_3 are off by default. In the MVL-DC-DN, the reactance and reac-

tive power are both ignored [30], [31]. The turn ratio of the DCT is controlled to be constant. The baseline load power vector $\boldsymbol{P}_{\mathrm{b}}$ consists of the original load power for each bus. All parameters of the MVL-DC-DN are listed in Table II.

TABLE II
PARAMETERS OF MVL-DC-DN

Parameter	Value
Controlled turn ratio of DCT (p.u.)	0.9
Switching frequency of DCT (Hz)	1000
Auxiliary inductance (mH)	0.1
Winding turn ratio of DCT	2
Rated voltage on transformer sides (kV)	12.66/6.33
Voltage base on transformer sides (kV)	12.66/6.33
Power base (MVA)	10

A. Maximum Loadability Comparison Between MVL-DC-DN and MVL-DC-DN with DC-ESs

With the parameters of DC-ESs listed in Table III, the voltage curves of the MVL-DC-DN with and without DC-ESs are illustrated, where λ corresponding to the bifurcation point of the voltage curve represents the maximum loadability of the networks. A larger λ means a greater maximum loadability. It can be observed from Fig. 11 that the maximum loadability of the MVL-DC-DN with DC-ESs is nearly 0.2 greater than that of the one without DC-ESs. Obviously, the DC-ESs have enhanced the maximum loadability of the MVL-DC-DN.

TABLE III
PARAMETERS OF DC-ESS

Parameter	Value
DC-ES location	Buses 21, 24, and 27
$V_{\mathrm{es},i}^{\mathrm{lim}}$ (p.u.)	–0.5, –0.5, –0.5
$P_{\mathrm{es},i}^{\mathrm{rate}}$ (p.u.)	–0.009, –0.008, –0.007

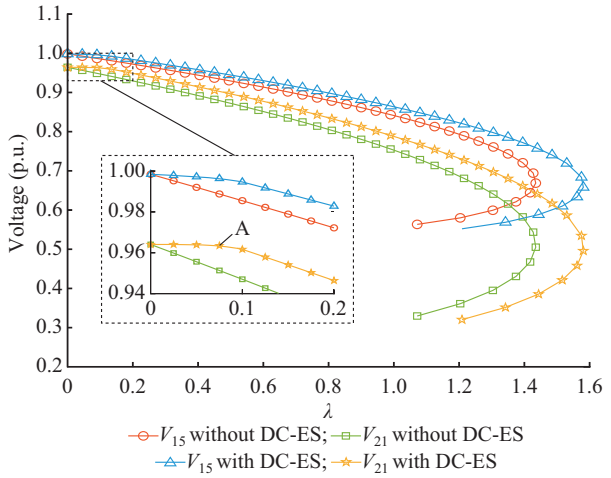


Fig. 11. Voltage curves of MVL-DC-DN with and without DC-ESs.

The three stages distinguished in Section IV-C are shown in the Fig. 11 and Fig. 12.

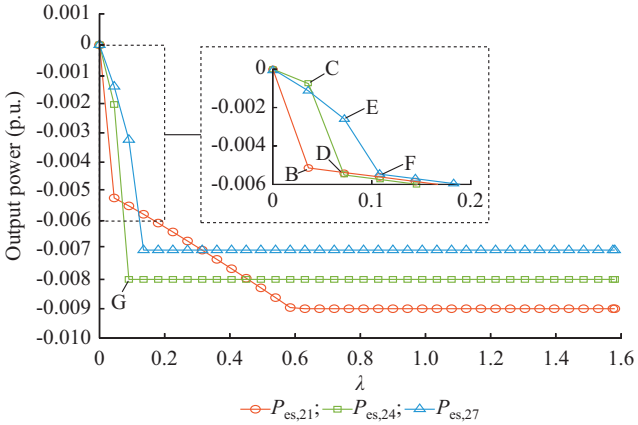


Fig. 12. Output power curves of MVL-DC-DN with DC-ESs.

Stage I: in Fig. 11, before point A, the voltage of Bus 21 can be regulated to the target value by the DC-ES, and the bus type is V. In Fig. 12, point B corresponds to point A. Before point B, DC-ESs connected to Bus 24 and Bus 27 do not reach their output voltage limits. However, the power curve of Bus 24 experiences a turning point at point C. The reason is that, after point B, the DC-ES on Bus 21 is unable to sustain the bus voltage. Consequently, a considerable amount of additional power is needed to be injected by the DC-ES on Bus 24 in order to maintain the bus voltage. It is evident that the slope of the curve increases after point C.

Stage II: after point B, the DC-ES on Bus 21 reaches its output voltage limit but still holds the power injection. During this process, the DC-ES on Bus 24 passes through point D. At point D, the output voltage of the DC-ES is limited, which results in point E. The DC-ES on Bus 27 reaches its output voltage limit at point F.

Stage III: after point G, the DC-ES on Bus 24 first reaches its output power limit and is limited. The other two DC-ESs continue to provide increasing output power with limited output voltage until they reach their power limit.

B. Maximum Loadability Considering Rated Power Capability of DC-ES and Current Limitation of DCT

To further verify the advantages and practicality of the proposed method, three cases are considered.

1) Case 1: neither the rated power capability of the DC-ES nor the current limitation of the DCT is considered.

2) Case 2: the rated power capability of the DC-ES is considered, while the current limitation of the DCT is not considered.

3) Case 3: both the rated power capability of the DC-ES and the current limitation of the DCT are considered. The evaluation results are illustrated in Fig. 13 and Fig. 14. The Bus 27 is taken as the sample. In case 3, the current limitation of the DCT is set to be 700 A on the secondary side.

The evaluated maximum loadability results in the three cases are 1.897, 1.581, and 1.122, respectively. It can be observed that the result in case 1 has a greater value than that in case 2 by more than 19.99%. Besides, the results in cases 1 and 2 are 69.07% and 40.91% greater than that in case 3, respectively. In summary, the proposed method could effec-

tively prevent the network from collapsing caused by overestimating the maximum loadability.

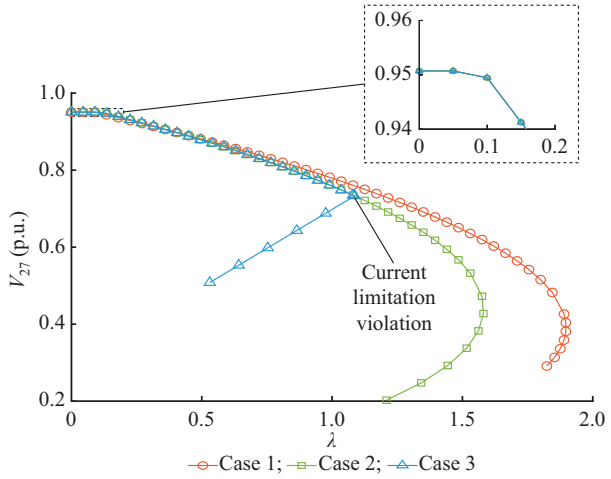


Fig. 13. Voltage curves of Bus 27 in three cases.

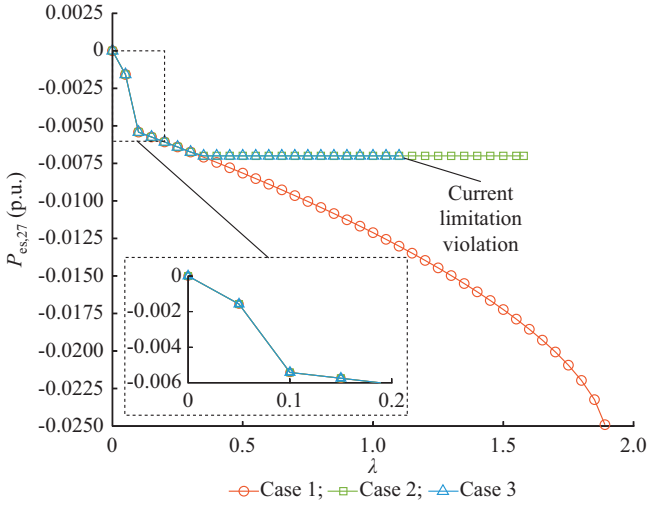


Fig. 14. Output power curves of Bus 27 in three cases.

C. Maximum Loadability Considering Rated Power Capability of DC-ES and Current Limitation of DCT in Meshed Network Powered by Multiple Power Sources

In this subsection, the effectiveness of the proposed method in a meshed network powered by multiple power sources is evaluated by closing the interconnection switches S1-S3 in Fig. 10. The output voltages of power sources I and II are kept constant. Figure 15 presents the voltage curves of the meshed network powered by multiple power sources with and without DC-ESs.

As depicted in Fig. 15, the values of λ corresponding to the bifurcation point of the voltage curve for meshed networks powered by multiple power sources with and without DC-ESs are 1.815 and 1.664, respectively. The former one is 0.151 greater than the latter. This phenomenon verifies that DC-ESs are also effective in a meshed network powered by multiple power sources, in term of enhancing the maximum loadability. In Fig. 16, the output power curves of the meshed network powered by multiple power sources are illustrated. Inflection points observed on the curves can be attributed to the same reasons that were analyzed in Section V-A.

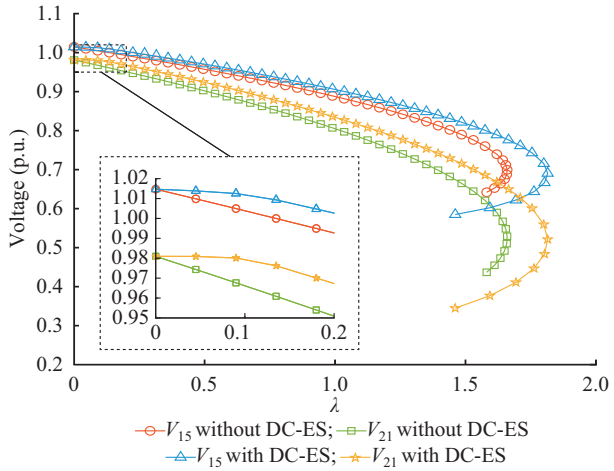


Fig. 15. Voltage curves of meshed network powered by multiple power sources with and without DC-ESs.

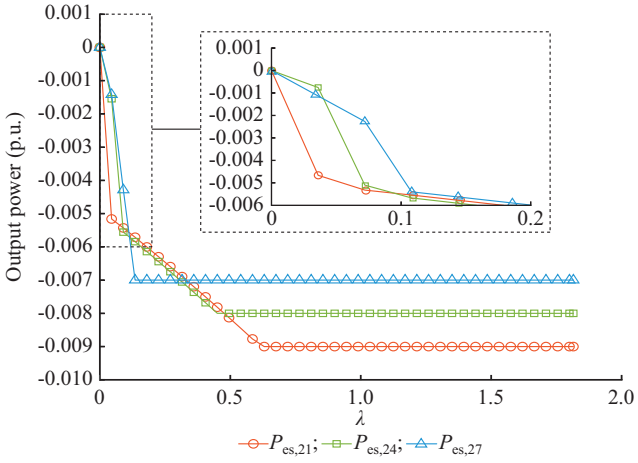


Fig. 16. Output power curves of meshed network powered by multiple power sources.

To verify the advantages of the proposed method in a meshed network powered by multiple power sources, a comparison is made with the three cases mentioned in Section V-B. The voltage and output power curves of Bus 27 for these three cases in the meshed network powered by multiple power sources are shown in Fig. 17 and Fig. 18, respectively. In Fig. 17, the maximum values of λ in the three cases are 2.197, 1.814, and 1.153, respectively. The results for cases 1 and 2 are 90.55% and 57.33% higher than those in case 3, respectively. Compared with the radial network with single power source in Section V-B, the proposed method demonstrates a clearer advantage in avoiding estimation errors here.

In general, the case studies have verified the effectiveness of the proposed method, in either radial networks with a single power source or meshed networks with multiple power sources.

D. Impact of DC-ES on Maximum Loadability of MVL-DC-DN

The impact of DC-ES on the maximum loadability is demonstrated as follows.

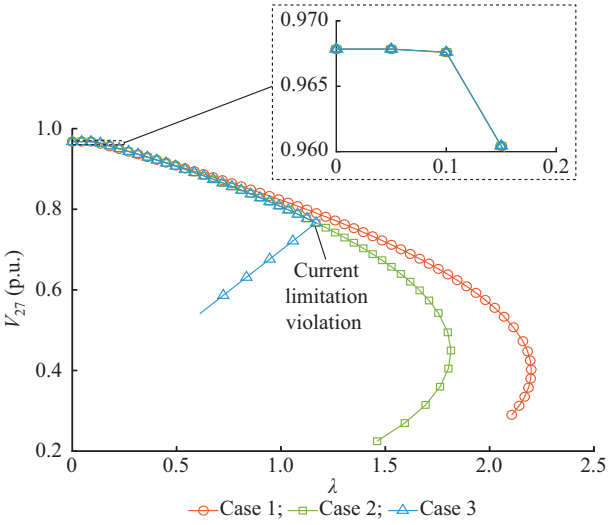


Fig. 17. Voltage curves of Bus 27 in meshed network powered by multiple power sources in three cases.

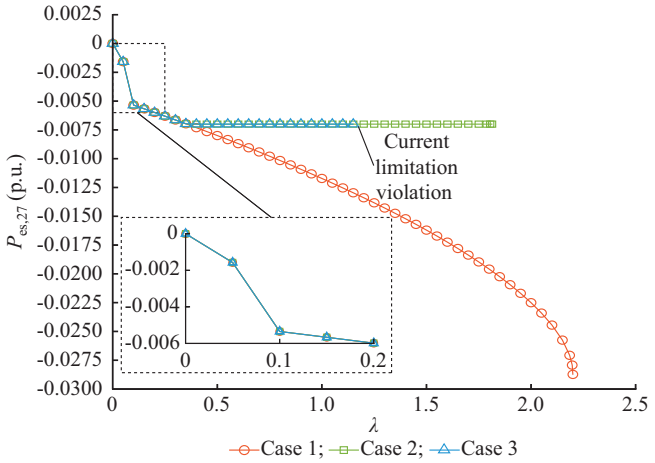


Fig. 18. Output power curves of Bus 27 in meshed network powered by multiple power sources in three cases.

Figure 19 depicts the relationship among the maximum loadability, the voltage amplitude limit V_{es}^{lim}, and the power proportion α. For the convenience of analysis within the MVL-DC-DN, only one DC-ES is connected to Bus 27, with a rated power capability of 150 kW. The ranges of V_{es}^{lim} and α are [0.1, 0.8]p.u. and [0, 1], respectively. In Fig. 19(a), the DC-ES works as an ideal voltage source. Figure 19(a) illustrates that an increase in both $\left|V_{es}^{lim}\right|$ and α leads to a larger maximum loadability, provided that the rated power capability of the DC-ES is not considered. While in Fig. 19(b), where the rated power capability of the DC-ES is considered, the maximum loadability is independent of $\left|V_{es}^{lim}\right|$ and α after the rated power capability is reached.

Figure 20 depicts the impact of V_{es}^{lim} and α on the growth rate with and without consideration of the rated power capability of the DC-ES. In Fig. 20, $\Delta\lambda_{I}^{max}$ and $\Delta\lambda_{II}^{max}$ denote the impacts of $\left|V_{es}^{lim}\right|$ and α on the growth rate of λ^{max}, respectively, which are defined as:

$$\Delta\lambda_{I}^{max}(n_1,n_2)=\lambda^{max}(V_{es,n_1+1}^{lim},\alpha_{n_2})-\lambda^{max}(V_{es,n_1}^{lim},\alpha_{n_2}) \quad (33)$$

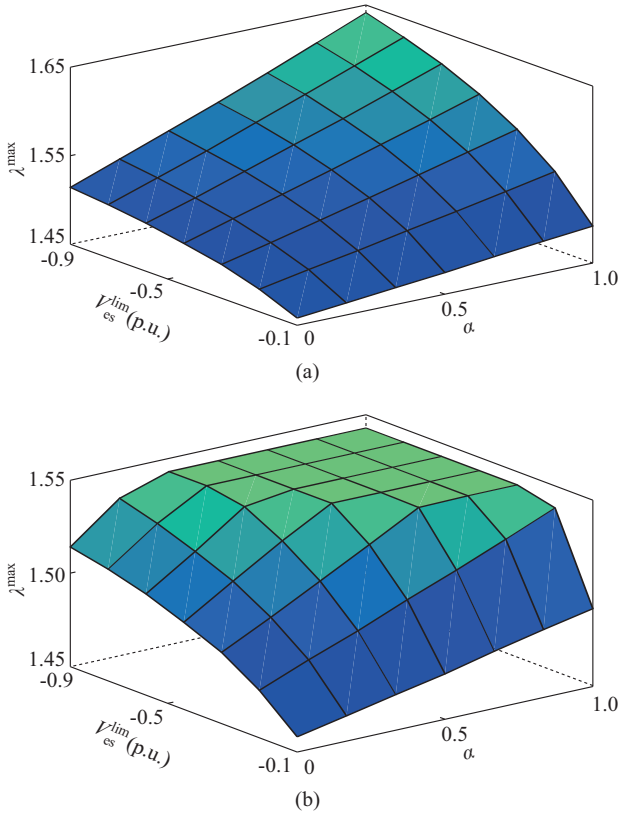


Fig. 19. Relationship among maximum loadability, V_{es}^{lim}, and α. (a) Rated power capability of DC-ES is not considered. (b) Rated power capability of DC-ES is considered.

$$\Delta\lambda_{II}^{max}(n_1,n_2)=\lambda^{max}(V_{es,n_1}^{lim},\alpha_{n_2+1})-\lambda^{max}(V_{es,n_1}^{lim},\alpha_{n_2}) \quad (34)$$

where $\lambda^{max}(V_{es,n_1+1}^{lim},\alpha_{n_2})$ denotes the value of λ^{max} with V_{es,n_1+1}^{lim} as the horizontal axis and with α_{n_2} as the vertical axis.

As shown in Fig. 20(a) and (b), the growth rate decreases as $\left|V_{es}^{lim}\right|$ increases. However, the growth rate increases with α, although the trend is not remarkable. In Fig. 20(c) and (d), the growth rate exhibits a similar pattern as observed in Fig. 20(a) and (b), respectively, until the rated power capability of the DC-ES is reached. Thereafter, the growth rate declines to 0. Therefore, to enhance the maximum loadability of the MVL-DC-DN by increasing the maximum voltage amplitude of the DC-ES, it can be inferred that when the maximum voltage amplitude exceeds a specific range, the cost effectiveness diminishes. The precise range value is determined by multiple influencing factors including load power and DC-ES location.

VI. Conclusion

The obtained conclusions from this paper are summarized as follows.

1) The maximum loadability of an MVL-DC-DN can be effectively enhanced by the DC-ES.

2) By considering the limitations of DC-ESs and current limitation of DCTs, the proposed method effectively avoids overestimating the maximum loadability of an MVL-DC-DN with DC-ESs, which is beneficial for preventing the network from collapsing.

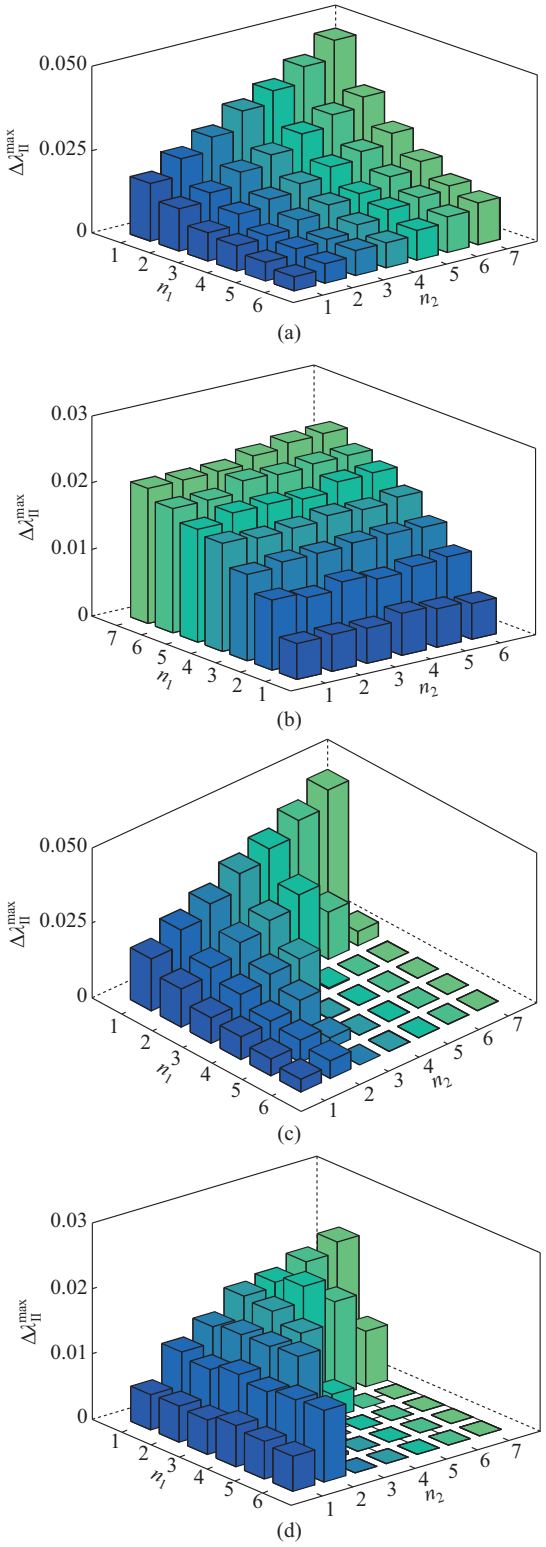


Fig. 20. Impact of V_{es}^{lim} and α on growth rate with and without consideration of rated power capability of DC-ES. (a) Impact of V_{es}^{lim} on growth rate without consideration of rated power capability of DC-ES. (b) Impact of α on growth rate without consideration of rated power capability of DC-ES. (c) Impact of V_{es}^{lim} on growth rate with consideration of rated power capability of DC-ES. (d) Impact of α on growth rate with consideration of rated power capability of DC-ES.

3) The proposed method is suitable for both the radial network with a single power source and the meshed network powered by multiple power sources.

4) The cost effectiveness of increasing the maximum voltage amplitude of the DC-ES to enhance the maximum loadability diminishes after a specific range.

This paper lays a preliminary and essential foundation for the optimal configuration for DC-ESs in an MVL-DC-DN to enhance the maximum loadability.

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Xiaolong Xu received the B.S. degree in electrical engineering and automation from China University of Petroleum, Qingdao, China, in 2021, and he is currently pursuing the Ph.D. degree with the School of Electrical Engineering, Chongqing University, Chongqing, China. His research interests include voltage stability of distribution networks.

Qianggang Wang received the B. S. and Ph. D. degrees from Chongqing University, Chongqing, China, in 2009 and 2015, respectively. He was a Research Fellow with Nanyang Technological University, Singapore, from 2015 to 2016. He is currently a Professor with the School of Electrical Engineering, Chongqing University. His research interests include analysis and operation of power systems, microgrid, and power quality.

Jianquan Liao received the B. S. degree in electrical engineering from China University of Petroleum, Qingdao, China, in 2017. He received the Ph.D. degree from Chongqing University, Chongqing, China, in 2021. He is an Associate Research Fellow at the School of Electrical Engineering, Sichuan University, Chengdu, China, since 2021. From September 2019 to September 2020, he was a Guest Researcher of the Delft University of Technology, Delft, The Netherlands. He worked in DC Systems, Energy Conversion and Storage Group in Electrical Sustainable Energy, Delft, The Netherlands. He paid attention to the application of power electronic equipment in power systems, such as DC filter, DC power flow controller, DC electric spring, and studied their design and dynamic control and fault protection. His research interests include power system protection and control, and power quality of DC distribution network.

Yuan Chi received the B. E. degree from Southeast University, Nanjing, China, in 2009, the M. E. degree from Chongqing University, Chongqing, China, in 2012, and the Ph.D. degree from Nanyang Technological University, Singapore, in 2021. From 2012 to 2016, he worked as an Electrical Engineer of Power System Planning consecutively with State Grid Chongqing Electric Power Research Institute, Chongqing, China, and Chongqing Economic and Technological Research Institute, Chongqing, China. He is currently working as a Research Associate with Chongqing University. His research interests include planning and resilience of power system and voltage stability.

Tao Huang received the Ph.D. degree from Politecnico di Torino, Turino, Italy, in 2011. He is currently a Professor with the Department of Energy, Politecnico di Torino. He is also an Adjunct Professor with Xihua University, Chengdu, China, and Polytechnic University of Henan, Jiaozuo, China. His research interests include vulnerability assessment, electricity market, smart grid, active distribution network, and artificial intelligence in power systems.

Niancheng Zhou received the B. S., M. S., and Ph. D. degrees in electrical engineering from Chongqing University, Chongqing, China, in 1991, 1994, and 1997, respectively. He worked at Chongqing Kuayue Technology Co., Ltd., Chongqing, China, from 1997 to 2003. He is a Professor at the School of Electrical Engineering, Chongqing University. From 2010 to 2011, he was a Research Fellow of Nanyang Technological University, Singapore. His research interests include analysis and operation of power systems, microgrid, and power quality.

Yiyao Zhou received the B.S. degree from Chongqing University, Chongqing, China, in 2018, and the M.E. degree from Hefei University of Technology, Hefei, China, in 2021. He is currently pursuing the Ph. D. degree in School of Electrical Engineering, Chongqing University. His research interests include modeling, optimization, and operation of distribution networks.

Xuefei Zhang received the B.S. and M.S. degrees in electrical engineering from Kunming University of Science and Technology, Kunming, China, in 2018 and 2021, respectively. He is currently pursuing the Ph. D. degree in School of Electrical Engineering, Chongqing University, Chongqing, China. His research interests include modeling, optimization, and operation of power systems.