Compound Compensation Control for Improving Low-voltage Ride-through Capability of Virtual Synchronous Generators

Zhiyuan Meng, Xiangyang Xing, *Member*, *IEEE*, Xiangjun Li, *Senior Member*, *IEEE*, and Jiadong Sun

***Abstract*—The virtual synchronous generator (VSG), utilized as a control strategy for grid-forming inverters, is an effective method of providing inertia and voltage support to the grid. However, the VSG exhibits limited capabilities in low-voltage ride-through (LVRT) mode. Specifically, the slow response of the power loop poses challenges for VSG in grid voltage support and increases the risk of overcurrent, potentially violating present grid codes. This paper reveals the mechanism behind the delayed response speed of VSG control during the grid faults. On this basis, a compound compensation control strategy is proposed for improving the LVRT capability of the VSG, which incorporates adaptive frequency feedforward compensation (AFFC), direct power angle compensation (DPAC), internal potential compensation (IPC), and transient virtual impedance (TVI), effectively expediting the response speed and reducing transient current. Furthermore, the proposed control strategy ensures that the VSG operates smoothly back to its normal control state following the restoration from the grid faults. Subsequently, a large-signal model is developed to facilitate parameter design and stability analysis, which incorporates grid codes and TVI. Finally, the small-signal stability analysis and simulation and experimental results prove the correctness of the theoretical analysis and the effectiveness of the proposed control strategy.**

***Index Terms*—Virtual synchronous generator (VSG), grid-forming inverter, low-voltage ride-through (LVRT), compensation control.**

I. Introduction

DISTRIBUTED generation systems (DGSs), consisting of renewable energy sources and grid-connected inverters, represent a booming technology for addressing the energy crisis problems [1]. In recent years, the voltage source inverters (VSIs) are increasingly integrated into the power grid [2]. However, the electrical equipment often exhibits low inertia and weak damping characteristics, thereby posing a threat to the stable operation of the power system [3]-[5]. Thereupon, the virtual synchronous generator (VSG), as a form of grid-forming (GFM) inverter, is proposed to provide inertia and voltage support for the grid [6]-[8], thereby ensuring the stable operation of VSIs.

The VSG aims to emulate the characteristics of the synchronous machines in the VSIs. However, they exhibit limitations during the grid faults, as the inverters are not built to handle prolonged overcurrent situations, reflecting a comparatively weaker overcurrent capability than that of traditional synchronous machines [9].

To equip the VSG with fault ride-through capabilities during the grid faults, various low-voltage ride-through (LVRT) strategies are developed to tackle challenges like overcurrent and rapid power tracking. Presently, two primary LVRT control strategies for VSG are prevalent. One LVRT control strategy transitions the VSG into a grid-following (GFL) inverter during the grid faults [10], [11]. The other LVRT control strategy incorporates additional control loops specifically for compensating internal potential or power angle [12]-[15].

Although GFL inverters have advantages in current limiting and tracking speed [16]-[18], mode switching causes the VSG to lose the voltage source characteristics. The use of phase-locked loops (PLLs) in GFL inverters might induce instability in systems with high penetration of renewable energy [19]. Additionally, to mitigate the effects of mode switching, a seamless switching control strategy is essential to maintain state variable consistency before and after the grid faults. This necessitates the simultaneous implementation of both GFL and GFM control modes, as detailed in [11], which significantly increases the computational demands on the controller.

The transient virtual impedance (TVI) control strategy is proposed in [12], [13], which introduces virtual impedance (VI) to effectively reduce output voltage of the VSG, thereby facilitating current limitation. Importantly, the TVI is designed to gradually decrease to zero, minimizing any negative impact on the system.

Despite significant research into LVRT control and small-signal modeling of TVI, the practical application of TVI still

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encounters several challenges. Firstly, while TVI effectively limits current, it does not enhance the power response speed of VSG during the grid faults, which is in contradiction with the existing grid codes. For example, [20] mandates that the reactive power adjustment time for VSG should not exceed 60 ms when a symmetrical fault occurs in the grid voltage. Secondly, grid codes dictate that the power output of VSG during the grid faults should be a function of the output voltage [20], [21]. This dynamic adjustment is frequently overlooked in both small-signal [22] and large-signal [12] models. To address these problems, TVI must be integrated with additional control strategies for effective fault ride-through capability, and the mathematical modeling of VSG must align with the stipulations of grid codes.

TVI can be regarded as an indirect form of internal potential compensation (IPC). References [14] and [15] explore direct IPC techniques. In [14], the output voltage of the VSG is directly incorporated into the control loop as a compensation term, which effectively addresses overcurrent problem caused by the grid faults. However, [14] does not directly control reactive power but adjusts the output voltage instead, which fails to meet the reactive power support standards required by the grid codes. Reference [15] introduces a refined IPC formula that utilizes output voltage and phase angle, and proposes a power angle compensation strategy that reacts to changes in the power angle during the grid faults. This strategy successfully mitigates steady-state overcurrent problem and decreases the regulation time of the power loops. However, [15] only resolves the steady-state overcurrent and does not suppress the transient current generated during the grid faults and fault recovery. Furthermore, the formulas for compensation in [15] are based on the condition of maximum output current, which may lead to inaccurate compensation. Additionally, the LVRT strategy described in [15] necessitates extra voltage sensors, thereby increasing equipment costs.

In summary, the current research problems can be summarized as insufficient analysis of the impact of the grid faults on the dynamic performance of VSG, inadequate accuracy of internal potential and power angle compensation, and a lack of large-signal and small-signal modeling that accounts for grid codes.

Hence, this paper introduces a compound compensation control strategy for VSG to address the outlined problems, which is aimed to improve LVRT performance of VSG. The main contributions of the proposed control strategy in this paper are as follows:

1) A virtual power angle is defined to derive accurate internal potential and direct power angle compensation (DPAC) without additional measurement equipment. The analysis via the transfer function of power loop shows that the grid faults extend the regulation time and increase overcurrent durations. Consequently, a compound compensation control strategy is proposed to enable rapid tracking of the power reference during the grid faults.

2) The effects of TVI control parameters on the dynamic performance and stability of VSG are examined through large-signal model.

3) A small-signal model is developed, which considers the reactive power support characteristics required by grid codes. The feasibility of the developed small-signal model is demonstrated through eigenvalue matrix analysis.

The rest of this paper is organized as follows. Section II derives the principle of VSG. Section III proposes the composite compensation control strategy. Sections IV and V show the simulation validation and experimental validation. Section VI concludes this paper.

II. Principle of VSG

A. VSG Control Structure

The active power control loop (APCL) is designed to generate the internal potential phase [23], which is given as:

$$\begin{cases} \omega = \omega_{\mathrm{n}} + \dfrac{1}{Js + D_{\mathrm{p}}} \dfrac{P_{\mathrm{ref}} - P}{\omega_{\mathrm{n}}} \\ \dfrac{\mathrm{d}\theta}{\mathrm{d}t} = \omega \\ \dfrac{\mathrm{d}\delta_{\mathrm{g}}}{\mathrm{d}t} = \omega - \omega_{\mathrm{n}} = \Delta\omega \end{cases} \tag{1}$$

where J is the virtual moment of inertia; D_{p} is the damping coefficient; ω and ω_{n} are the output angular frequency of the VSG and the rated angular frequency of the grid, respectively; P is the active power delivered to the point of common coupling (PCC); P_{ref} is the active power reference; θ is internal potential phase; and δ_{g} is the power angle.

The reactive power control loop (RPCL) is used to generate the internal potential signal, which is expressed as:

$$K \frac{\mathrm{d}M}{\mathrm{d}t} = Q_{\mathrm{ref}} - Q + D_{\mathrm{q}} (U_{\mathrm{Cn}} - V_{\mathrm{Cm}}) \tag{2}$$

where D_{q} is the voltage-droop coefficient; V_{Cm} and U_{Cn} are the PCC voltage magnitude and rated internal potential magnitude, respectively; Q is the reactive power delivered to the PCC; Q_{ref} is the reactive power reference; M is the variation of the internal potential relative to U_{Cn}; and K is the inertia coefficient.

Moreover, as shown in Fig. 1, the internal potential $E_{d\mathrm{ref}} = M + U_{\mathrm{Cn}}$, and $E_{q\mathrm{ref}} = 0$, where $E_{q\mathrm{ref}}$ is the q-axis reference voltage of VSG. The voltage-droop coefficient D_{q} affects the reactive power reference during the grid faults. Thus, it affects the reactive power output. Therefore, we set $D_{\mathrm{q}} = 0$ in the further analysis. Considering the RPCL is governed by an integrator, it is feasible to achieve the reactive power output target.

The power delivered to the PCC can be derived as:

$$\begin{cases} P = 1.5(v_{Cd} i_{sd} + v_{Cq} i_{sq}) \\ Q = 1.5(v_{Cq} i_{sd} - v_{Cd} i_{sq}) \end{cases} \tag{3}$$

where v_{Cd} and v_{Cq} are the PCC voltages on the synchronous dq coordinates, respectively; and i_{sd} and i_{sq} are the inverter-side currents on the synchronous dq coordinates, respectively.

Then, the PCC voltage magnitude V_{Cm} can be expressed as:

$$V_{\mathrm{Cm}} = \sqrt{v_{Cd}^2 + v_{Cq}^2} \tag{4}$$

The VI, consisting of virtual resistance R_{v} and virtual in-

ductance L_v, is designed to generate reference PCC voltages $v_{Cd\text{ref}}$ and $v_{Cq\text{ref}}$ [24]. The voltage and current control loops (VCCLs) are used to produce modulated signal e^*_{abc} for VSI. Subsequently, pulse width modulation (PWM) pulses are generated by sinusoidal PWM (SPWM).

Figure 1 shows the conventional VSG control structure, where C_f is the filter capacitor; L_g is the line inductance; i_{sabc} is the inverter-side current; v_{Cabc} is the PCC voltage; and v_{gabc} is the grid voltage.

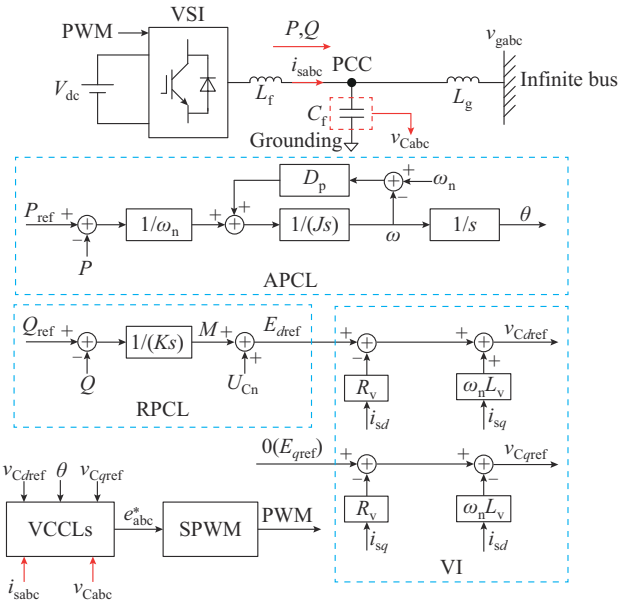

Fig. 1. Conventional VSG control structure.

B. Reactive Power Support Characteristics

The magnitude of reactive current injected into the grid depends on the severity of PCC voltage sags [20], [25], which is described as:

$$I_{q\text{ref}}=\begin{cases}0 & \dfrac{V_{\text{Cm}}}{U_{\text{Cn}}}\geq 0.9\\ -kI_{\text{N}}\left(0.9-\dfrac{V_{\text{Cm}}}{U_{\text{Cn}}}\right) & 0.2\leq\dfrac{V_{\text{Cm}}}{U_{\text{Cn}}}<0.9\\ -1.05I_{\text{N}} & \dfrac{V_{\text{Cm}}}{U_{\text{Cn}}}<0.2\end{cases}\tag{5}$$

where $I_{q\text{ref}}$ is the reactive current reference; k is the current gain and is set to be 1.5; and I_{N} is the nominal grid current magnitude.

Then, the active current injected into the grid is given as:

$$I_{d\text{ref}}=\begin{cases}\sqrt{I_{\text{N}}^2-I_{q\text{ref}}^2} & I_{\text{N}}^2-I_{q\text{ref}}^2\geq 0\\ 0 & I_{\text{N}}^2-I_{q\text{ref}}^2<0\end{cases}\tag{6}$$

where $I_{d\text{ref}}$ is the active current reference.

Thereupon, the power reference of the VSG can be derived as:

$$\begin{cases}P_{\text{ref}}=1.5V_{\text{Cm}}I_{d\text{ref}}\\ Q_{\text{ref}}=-1.5V_{\text{Cm}}I_{q\text{ref}}\end{cases}\tag{7}$$

A power-oriented reference generation method for VSG during LVRT is presented in (7). When the VI is applied, (7) remains unchanged, as mentioned in [26]. Additionally, to ensure that the current during the grid faults is consistent with (5) and (6), a current-oriented power reference generation can be used, which is discussed in detail in Supplementary Material A.

When $D_q=0$, it means that the RPCL loses droop control. Thus, the RPCL can be expressed as:

$$K\frac{\text{d}M}{\text{d}t}=Q_{\text{ref0}}+(0.9U_{\text{Cn}}-V_{\text{Cm}})\underbrace{\frac{1.5V_{\text{Cm}}kI_{\text{N}}}{U_{\text{Cn}}}}_{D_{\text{qe}}}-Q\tag{8}$$

where Q_{ref0} is the reactive power reference under the normal condition, which is set to be 0; and D_{qe} is the equivalent damping coefficient.

The RPCL expression for a conventional VSG is expressed as:

$$K\frac{\text{d}M}{\text{d}t}=Q_{\text{ref0}}+(U_{\text{Cn}}-V_{\text{Cm}})D_q-Q\quad D_q=\frac{Q_{\max}}{k_qU_{\text{Cn}}}\tag{9}$$

where $k_q\in[0.05,0.10]$ [6], [27]; and $Q_{\max}$ is the maximum reactive power reference.

Compared with (9), (8) shows that during the grid faults, the damping coefficient becomes a function of the PCC voltage. Under the normal condition, the VSG outputs little reactive power and the damping coefficient has a minimal effect. Therefore, even though D_q is set to be 0 in this paper, the VSG still possesses an equivalent damping coefficient D_{qe}.

To further demonstrate the rationale for setting D_q to be 0, simulation validation is conducted. The conventional VSG in (9) allows the VSG to support the PCC voltage during the grid faults. However, this causes the VSG to output excessive reactive power, resulting in overcurrent and inaccurate reactive power control, as illustrated in Fig. 2, where $Q_{\max}=$ 10 kvar, $k_q=0.1$, and V_g and V_{gn} are the amplitude of grid voltage and its normal value, respectively.

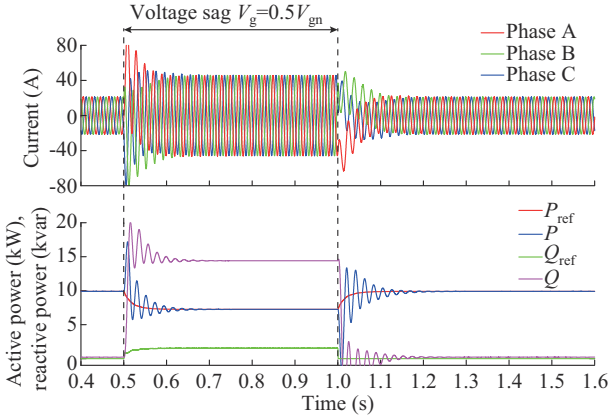

Fig. 2. Waveforms of inverter-side current and output power with conventional VSG control ($D_q=Q_{\max}/(k_qU_{\text{Cn}})$).

Furthermore, [26] indicates that the voltage mode characteristics of a GFM inverter can still be maintained by setting D_q to be 0 during a grid fault with the power references determined by the grid codes. If it is necessary to maintain the reactive power droop characteristic of the VSG under the normal condition, the strategy in [26] can be used. The de-

tailed process is shown in Supplementary Material B.

C. Performance of VSG During Grid Faults

The grid faults are categorized into symmetrical and asymmetrical faults, with symmetrical faults posing the greatest severity. Therefore, this paper primarily focuses on symmetrical faults.

The equivalent impedance from the internal potential signal to the PCC can be expressed as:

$$\begin{cases} Z_{eq} = \sqrt{R_{eq}^2 + X_{eq}^2} = \sqrt{R_v^2 + (\omega_n L_v)^2} = Z_v \\ \theta_I = \arctan \dfrac{\omega_n L_f}{R_v} \end{cases} \tag{10}$$

where L_f is the filter inductance; R_{eq}, X_{eq}, and Z_{eq} are the equivalent resistance, reactance, and impedance, respectively; θ_I is the impedance angle; and Z_v is the VI.

L_v is set equal to L_f in this paper, implying that no extra equivalent inductance is added. Consequently, $X_{eq} = \omega_n L_v = X_v$, and Z_{eq} equals the VI, i.e., Z_v.

The circuit model of VSG in Fig. 1 is simplified as Fig. 3. The active power P and reactive power Q are calculated as:

$$\begin{cases} \boldsymbol{I}_s = \dfrac{1}{\sqrt{2}} \dfrac{E_{refm}\angle\delta - V_{Cm}\angle 0°}{Z_v\angle\theta_I} \\ P = \mathrm{Re}\left(\dfrac{3V_{CM}\angle 0°}{\sqrt{2}} \bar{\boldsymbol{I}}_s \right) = \dfrac{3}{2} \dfrac{V_{Cm} E_{refm} Z_v \sin(\delta + \theta_I) - V_{Cm}^2 R_v}{Z_v^2} \\ Q = \mathrm{Im}\left(\dfrac{3V_{CM}\angle 0°}{\sqrt{2}} \bar{\boldsymbol{I}}_s \right) = \dfrac{3}{2} \dfrac{V_{Cm} E_{refm} Z_v \cos(\delta - \theta_I) - V_{Cm}^2 X_v}{Z_v^2} \end{cases} \tag{11}$$

where bold font and superscript $\overline{(\cdot)}$ represent the vector and conjugate vector, respectively; E_{refm} is the internal potential output by the VSG; $\boldsymbol{I}_s$ is the vector of inverter-side current; δ is the phase difference between the internal potential and PCC voltage; and Re(·) and Im(·) are the real and imaginary parts, respectively.

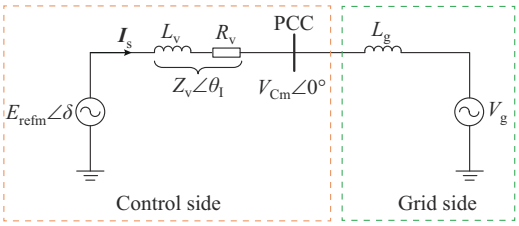

Fig. 3. Circuit model of VSG.

It is worth noting that δ in (11) represents a virtual power angle, rather than the actual power angle. The calculation of the actual power angle requires data on grid voltage and grid impedance [23], [24]. Acquiring this information typically demands additional measurement devices, which poses practical challenges and increases the costs. Therefore, this paper derives the expression of the virtual power angle by using VI and PCC voltage, which eliminates the need for extra hardware, allowing the calculations to be performed entirely through the software.

At the steady state, we set $P = P_{ref}$ and $Q = Q_{ref}$. To preserve the external characteristics of the circuit, the VI is set as $R_v << X_v$. Thus, (11) can be rewritten as:

$$\begin{cases} P \approx \dfrac{3}{2} \dfrac{E_{refm} V_{Cm}}{X_v} \sin\delta \\ Q \approx \dfrac{3}{2} \dfrac{E_{refm} V_{Cm} \cos\delta - V_{Cm}^2}{X_v} \end{cases} \tag{12}$$

$$\begin{cases} \delta \approx \arctan \dfrac{2P_{ref} X_v}{2Q_{ref} X_v + 3V_{Cm}^2} \\ E_{refm} \approx \dfrac{2X_v Q_{ref} + 3V_{Cm}^2}{3V_{Cm}\cos\delta} \end{cases} \tag{13}$$

This adjustment enables the derivation of E_{refm} and δ by means of the power references and the PCC voltage.

At the steady state, the small-signal model of the VSG is given as [22]:

$$\begin{cases} \hat{P} \approx \dfrac{3}{2} \dfrac{E_s V_{Cm} \cos\delta_s}{X_v} \hat{\delta} + \dfrac{3}{2} \dfrac{V_{Cm} \sin\delta_s}{X_v} \hat{E} \\ \hat{Q} \approx -\dfrac{3}{2} \dfrac{E_s V_{Cm} \sin\delta_s}{X_v} \hat{\delta} + \dfrac{3}{2} \dfrac{V_{Cm} \cos\delta_s}{X_v} \hat{E} \end{cases} \tag{14}$$

where the superscript $\hat{}$ represents the small perturbation; and E_s and δ_s are the value of the internal potential and the power angle, which are equal to E_{refm} and δ calculated by (13), respectively.

Neglecting the coupling between APCL and RPCL, the loop gains are obtained by combining (1), (2), and (14), which can be given as:

$$\begin{cases} T_p(s) = \dfrac{3}{2} \dfrac{E_s V_{Cm} \cos\delta_s}{X_v} \dfrac{1}{(Js + D_p)\omega_n} \dfrac{1}{s} \\ T_q(s) = \dfrac{3}{2} \dfrac{V_{Cm} \cos\delta_s}{X_v} \dfrac{1}{Ks} \end{cases} \tag{15}$$

where $T_p(s)$ and $T_q(s)$ are the loop gains of APCL and RPCL, respectively.

The bode diagram of the power control loops under different PCC voltages is shown in Fig. 4. Figure 4 illustrates that the cutoff frequencies ω_{cp} of the APCL and ω_{cq} of the RPCL decrease as the PCC voltage sags, signifying a slowdown in the response speed of the power control loops during the grid faults.

III. Compound Compensation Control Strategy

The compound compensation control strategy proposed in this paper comprises adaptive frequency feedforward compensation (AFFC), DPAC, IPC, and TVI. The proposed control strategy for LVRT is shown in Fig. 5.

A. AFFC

The proposed control strategy employs AFFC to increase the cutoff frequency of the APCL during the grid faults, thereby reducing the adjustment time of the APCL. Figure 6 presents the small-signal control block diagram of AFFC.

The adaptive compensation coefficient k_A is given as:

$$k_A = \frac{U_{Cn}^2 - E_s V_{Cm}}{E_s V_{Cm}} \tag{16}$$

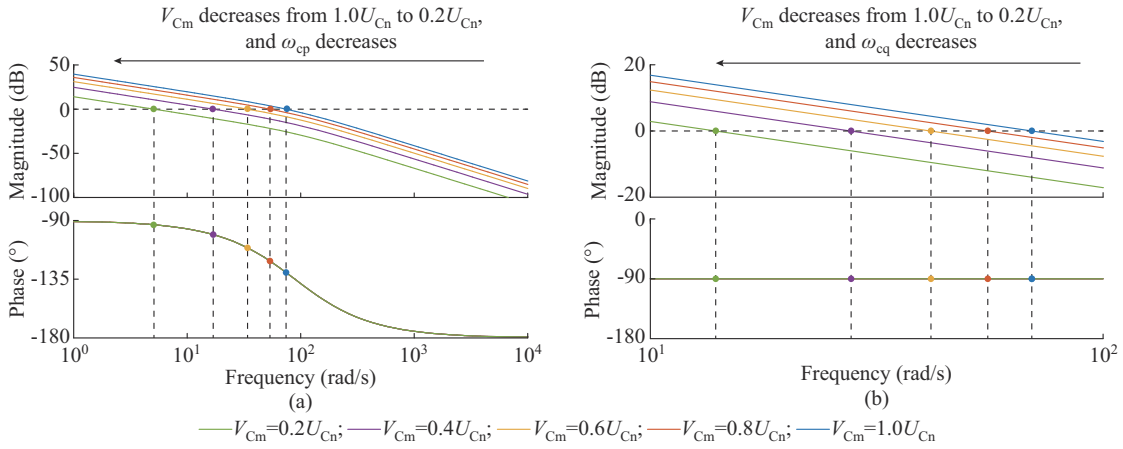

Fig. 4. Bode diagram of power control loops under different PCC voltages. (a) Bode diagram of APCL. (b) Bode diagram of RPCL.

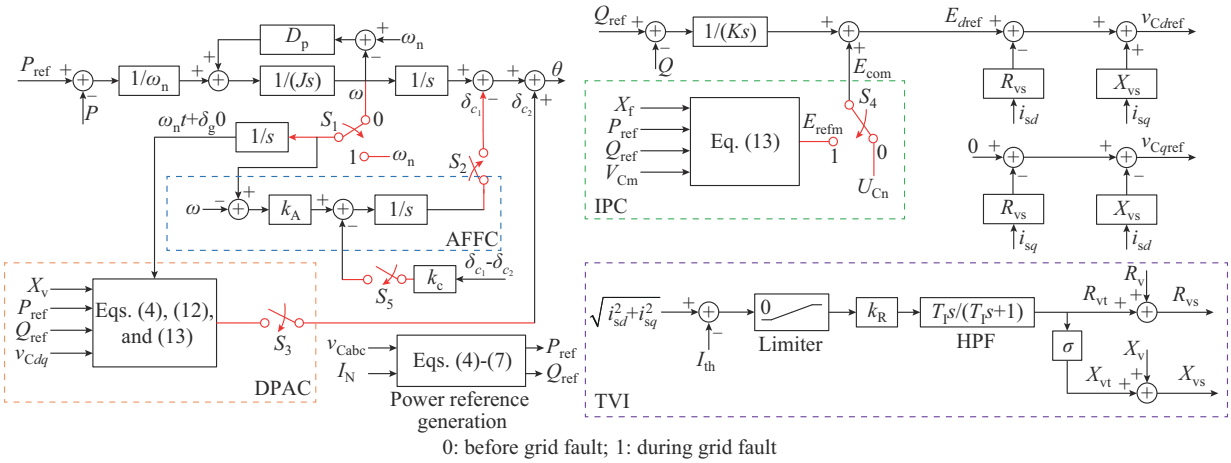

Fig. 5. Proposed control strategy for LVRT.

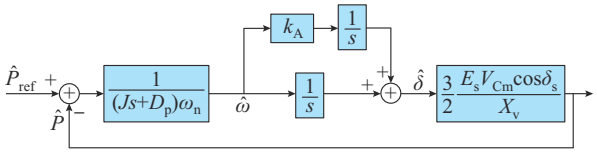

Fig. 6. Small-signal control block diagram of AFFC.

The gain loop of AFFC $T_{\mathrm{AFFC}}(s)$ is derived as:

$$T_{\mathrm{AFFC}}(s)=\frac{3U_{\mathrm{Cn}}^2\cos\delta_{\mathrm{s}}}{2s(Js+D_{\mathrm{p}})\omega_{\mathrm{n}}X_{\mathrm{v}}}\approx\frac{3U_{\mathrm{Cn}}^2}{2s(Js+D_{\mathrm{p}})\omega_{\mathrm{n}}X_{\mathrm{v}}}\tag{17}$$

where δ_{s} is approximately 0 at the steady state by (4)-(7).

AFFC raises the cutoff frequency of the APCL during the grid faults to the same level as that before the grid fault, thereby reducing the adjustment time.

B. DPAC

The vector diagram of the system before and during the grid faults is shown in Fig. 7, where the subscripts 0 and 1 represent the physical quantity before and during the grid faults, respectively; δ_{g} is the phase difference between the internal potential and grid voltage; v_{gq} is the axis with a lag of $v_{\mathrm{g0}}=90°$; δ_{Cd_0} is the phase angle of PCC voltage during grid fault on the synchronous d_0q_0 coordinates; δ_{c_2} is the change in angle of the internal potential $\boldsymbol{E}_{\mathrm{ref1}}$ relative to $\boldsymbol{E}_0$; and $\boldsymbol{v}_{\mathrm{C1}d_0}$ and $\boldsymbol{v}_{\mathrm{C1}q_0}$ are the d-axis and q-axis components of PCC voltage $\boldsymbol{v}_{\mathrm{C1}}$ on the synchronous d_0q_0 coordinates, respectively.

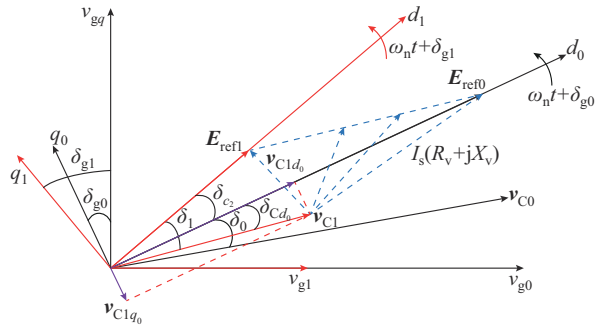

Fig. 7. Vector diagram of system before and during grid fault.

Figure 7 shows that the introduction of a compensation angle δ_{c_2} upon the detection of a grid fault enables the VSG to swiftly achieve a steady state. δ_{c_2} is calculated as:

$$\delta_{c_2}=\delta_1-\delta_{Cd_0}=\delta_1-\arctan\left|\frac{\boldsymbol{v}_{\mathrm{C1}q_0}}{\boldsymbol{v}_{\mathrm{C1}d_0}}\right|\tag{18}$$

where δ_1 is calculated by (13).

In order to derive δ_{Cd_0} in the d_0q_0 coordinates before the grid faults, Fig. 5 depicts an integrator positioned at post-switch S_1. Upon the detection of the PCC voltage sags, S_1 transitions from 0 to 1, preserving the phase angle signal before the grid fault.

In (18), performing an arctan calculation on the PCC voltage might appear to simulate an open-loop PLL. However, this does not transform the VSG in a GFL mode. At the steady state, both δ_{c_1} and δ_{c_2} are constants, with their time derivatives equal to zero. Therefore, they have no impact on the output angular frequency ω. Therefore, ω is governed by the APCL both before and during the grid faults. This feature is the characteristic of a GFM inverter.

C. IPC

The results in Fig. 4 indicate that PCC voltage sags lead to a deceleration in the response speed of the RPCL, which extends the time needed for the internal potential signal to stabilize, causing prolonged periods of overcurrent. To address this problem, the IPC is introduced.

Following the detection of the PCC voltage sags, (13) is used to compute the internal potential signal. Then, S_4 in Fig. 5 is switched from 0 to 1 to implement the IPC. The IPC acts as adaptive feedforward compensation, significantly reducing the regulatory impact on RPCL.

D. TVI

The TVI in Fig. 5 is adopted to reduce the transient current. Studies investigate the impact of the TVI on the GFM inverters through small-signal analysis [12], [22]. However, small-signal models fail to capture the nonlinear behavior of the inverters during the grid faults [22]. Therefore, this paper examines the effects of the TVI on VSG in the LVRT mode using large-signal model. To highlight the significance of the TVI, a comprehensive large-signal model that incorporates only the TVI and grid codes are developed.

The HPF is expanded to define the state variable x_{VI}, as shown in Fig. 8 and (19).

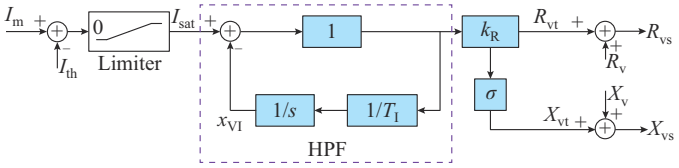

Fig. 8. Diagram of TVI control.

$$\frac{\mathrm{d}x_{VI}}{\mathrm{d}t} = -\frac{1}{T_I}x_{VI} + \frac{1}{T_I}I_{sat} \tag{19}$$

where $I_{sat} = \max(I_m - I_{th}, 0)$, I_m is the current magnitude, and I_{th} is the current threshold for starting TVI; and T_I is the time constant of the high-pass filter (HPF).

Therefore, R_{vt} and X_{vt} are expressed as:

$$\begin{cases} R_{vt} = \dfrac{\mathrm{d}x_{VI}}{\mathrm{d}t} T_I k_R \\ X_{vt} = R_{vt}\sigma \end{cases} \tag{20}$$

where k_R is the gain for TVI; R_{vt} and X_{vt} are the transient virtual resistance and inductance, respectively; and $\sigma = X_{vt}/R_{vt}$.

The gain k_R is designed to limit the current during a bolted fault [13], which is shown as:

$$\begin{cases} U_{Cn} = I_{m,max}\sqrt{R_{vs}^2 + X_{vs}^2} \\ k_R \geq \dfrac{-b + \sqrt{b^2 - 4ac}}{2a} \end{cases} \tag{21}$$

where $I_{m,max}$ is the maximum current magnitude, which is set to be $1.5I_N$, i.e., $I_{m,max}$=30 A; a, b, and c are shown in (SA1) in Supplementary Material A; and $R_{vs} = R_v + R_v$ and $X_{vs} = X_v + X_{vt}$ are the equivalent virtual resistance and equivalent virtual reactance, respectively.

Generally, σ should be greater than 3 to ensure that TVI exhibits inductive characteristics [22]. The lower bound of k_R is determined by setting $\sigma = 6$. Therefore, k_R is calculated as 0.2 Ω/A, and in subsequent analyses, k_R might not be recalculated to simplify the analysis under various σ.

Generally, the bandwidth of the power loop is set much lower than that of the VCCL [26]. Consequently, only the power loops and the TVI are considered during the establishment of the large-signal model of the VSG. The detailed large-signal model of the LCL circuit is derived in (SA2) in Supplementary Material A.

Then, the large-signal model of the VSG is formulated by combining (1), (2), (19), and (S2). The "ode45" command in MATLAB [24] is used to solve the large-signal model with various TVI parameters during the grid faults. The current magnitude I_m with various TVI parameters during the grid faults is illustrated in Fig. 9, where the grid voltage sags to $0.5V_{gn}$ at 2 s.

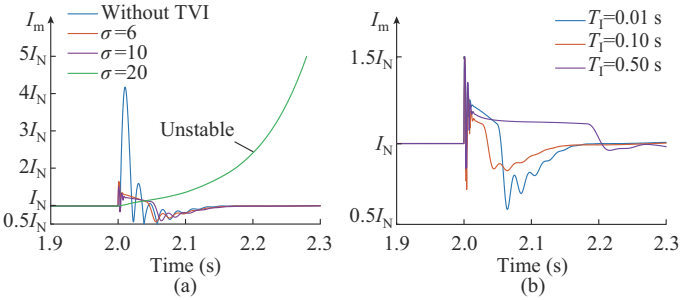

Fig. 9. Current magnitude with various TVI parameters during grid faults. (a) With various σ and without TVI. (b) With various T_I.

Figure 9(a) reveals that without TVI, the VSG experiences significant transient current. As σ increases, there is a notable reduction in both the magnitude and oscillation duration of the transient current. However, an excessively high σ leads to a loss of the stability. Then, Fig. 9(b) illustrates that a moderate increase in T_I can effectively mitigate the transient current and shorten the regulation time.

E. Description for Control Flow

Figure 10 presents the flowchart of the proposed control strategy. Upon detecting the PCC voltage sags ($V_{Cm} \leq 0.9U_{Cn}$), the VSG switches to the LVRT mode. Therefore, S_2 and S_3 are closed and S_1 and S_4 are switched from 0 to 1. This triggers the activation of AFFC, DPAC, and IPC, with TVI automatically engaging in response to the current levels. Follow-

ing the fault recovery, the VSG is switched to the voltage recovery mode. Initially, S_4 is switched from 0 to 1 to mitigate the overcurrent. A timer is then initiated to manage the transient process of the VSG and lessen the negative impacts of sudden removal of the compensation terms. The condition for the end of the voltage recovery mode is expressed as:

1) $T \geq T_{\text{set}}$, where T and T_{set} are the operation duration and preset time of the timer, respectively.

2) $|P_{\text{ref}} - P| \leq P_{\text{th}}$ and $|Q_{\text{ref}} - Q| \leq Q_{\text{th}}$, where P_{th} and Q_{th} are the active power and reactive power threshold, respectively.

After the voltage recovery mode ends, S_1 is switched from 1 to 0. Yet, the power angle compensation $\delta_{c_2} - \delta_{c_1}$ continues because S_2 and S_3 remain engaged. As S_1 is switched to 0, the input of the AFFC drops to 0. Thereupon, the power angle compensation value is used as feedback for the AFFC, facilitating a smooth exit from the power angle compensation. The specific process can be described as follows.

If $\delta_{c_1} > \delta_{c_2} > 0$ and $k_c|\delta_{c_2} - \delta_{c_1}| > \delta_{\text{th}}$, we should close S_5, where δ_{th} is the power angle threshold, and k_c is the power angle compensation gain. Since the feedback quantity $\delta_{c_1} - \delta_{c_2}$ is positive, δ_{c_1} gradually decreases under the integrator in AFFC. Once $|\delta_{c_2} - \delta_{c_1}| \leq \delta_{\text{th}}$, we should open S_2, S_3, and S_5, which means to end the power angle compensation smooth exit (PACSE) mode. The analytical approach for other conditions mirrors the above.

The flag for each switch is detailed in Supplementary Material B Table SBI.

Additionally, the proposed control strategy spans the entire LVRT process, rather than being limited to a specific segment. Consequently, the transition between these modes in Fig. 10 necessitates the switches and corresponding algorithms, inevitably increasing the complexity of the proposed control strategy. Despite this complexity, further sections present small-signal stability analysis and simulation results to demonstrate its feasibility and practicability.

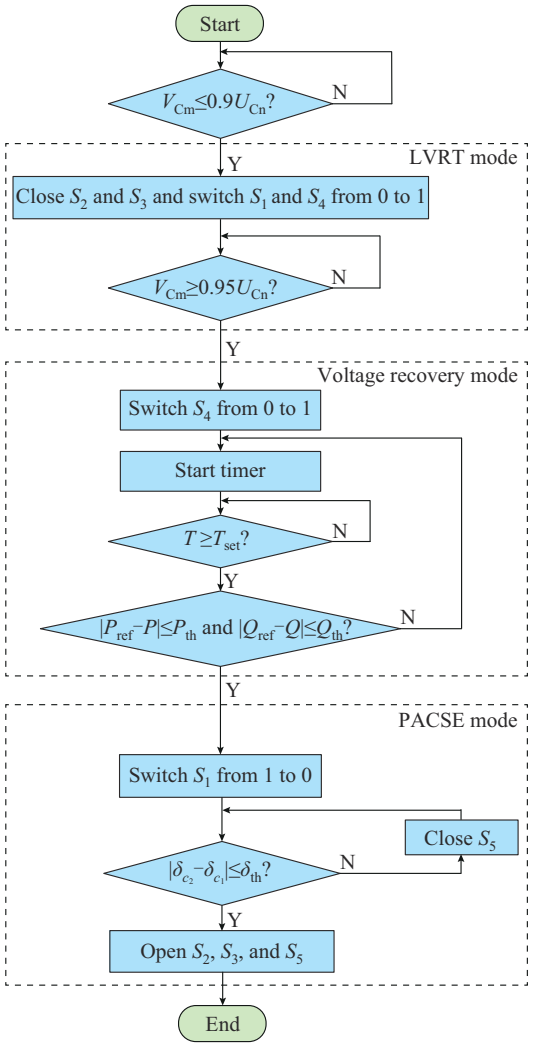

Fig. 10. Flow chart of proposed control strategy.

IV. Simulation Validation

In this section, a small-signal model of the VSG is established to analyze the impact of the proposed control strategy on the stability of the VSG and to detail the design of control parameters. Based on this, the proposed control strategy is validated through simulations during both symmetrical and asymmetrical grid faults, and is compared with existing strategies.

A. Small-signal Stability Analysis and Design of Control Parameters

To ensure the generality of the results, the small-signal model is confined to the conditions where the PCC voltage sags within the range of [0.2, 0.9]U_{Cn}. By applying local linearization techniques, the small-signal modeling process is detailed in (SA3)-(SA10) in Supplementary Material A.

The selected analysis condition involves a grid voltage sag to $0.5V_{\text{gn}}$. The trajectory of the eigenvalue variations of the state matrix formed by (SA3)-(SA10) in Supplementary Material A under different conditions is shown in Fig. 11.

Specifically, the simulation results from large-signal model in Fig. 9 show that the VSG becomes unstable when σ is set to be 20 during the grid faults. Conversely, Fig. 11 demonstrates that even σ increases to 28, the VSG remains stable. As previously mentioned, the small-signal model cannot capture the nonlinear behavior induced by large disturbances. Therefore, the obtained stability boundaries may not be applicable. Nonetheless, the eigenvalue trajectories still reflect the dynamic performance of the VSG under different conditions, providing a basis for parameter design. Thereupon, σ is finally designed as 10 to balance the stability and VSG performance.

k_{R} and σ are determined by the previous analysis. Then, this subsection continues to elaborate on the design of the remaining control parameters.

In deriving the power angle and IPC formulas, i.e., (13), it is assumed that R_{v} is much smaller than X_{v} with $X_{\text{v}} = X_{\text{s}} = 0.94\ \Omega$. Therefore, R_{v} is designed as $0.02\ \Omega$.

The current that the inverter can withstand should not exceed 1.5 times its rated current [15]. This implies that the overcurrent suppression threshold I_{th} must be lower than this threshold, which is specified here as 24 A.

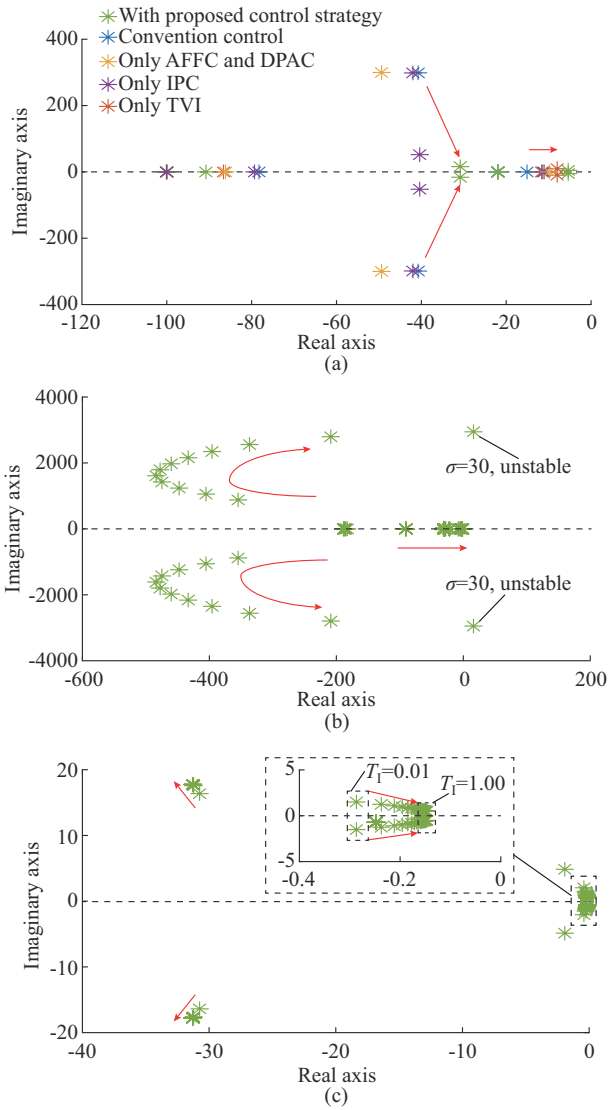

Fig. 11. Trajectory of eigenvalue variations of state matrix under different conditions. (a) With different control strategies. (b) With proposed control strategy (σ increases from 6 to 30 with an interval of 2). (c) With proposed control strategy (T_I increases from 0.01 to 1.00 with an interval of 0.05).

The peak fault current emerges approximately half a cycle post-fault and decays to steady state within approximately 10 cycles. Therefore, the time constant T_I is set as half a grid voltage cycle, i.e., 0.01 s, which is used to suppress the maximum fault current. Upon the fault clearance, the preset time of the timer T_{set} is set to be 0.3 s, leaving sufficient time for the exit of the power angle compensation term.

Under the normal conditions, VSG power fluctuations are less than $0.05P_n$ [28], where P_n is the rated power of 10 kW. Therefore, P_{th} and Q_{th} are set to be 500 W and 500 var, respectively. Then, by using the power angle formula presented in (13), when the output power changes by $0.05P_n$, (22) is derived to calculate the power angle variation, which is denoted as $\Delta\delta$. In the PACSE mode, the calculated $\Delta\delta$ is approximately 0.003 rad when $V_{Cm} \approx U_{Cn}$. Therefore, δ_{th} should be less than 0.003 rad. In addition, δ_{th} is designed to be 0.001 rad in this study.

$$\Delta\delta \approx \arctan\frac{2(1.05P_{ref})X_v}{3V_{Cm}^2} - \arctan\frac{2P_{ref}X_v}{3V_{Cm}^2} \tag{22}$$

When initiating the PACSE mode, the VSG already reaches the steady state and $\delta_{c_2} \approx 0$. Thus, the simplification of PACSE mode is shown in Fig. 12, where $\delta_{c_1,ini}$ is the initial value of the integrator. Therefore, k_c determines the duration of the PACSE mode. Considering the smoothness of this mode, k_c is designed as 5.

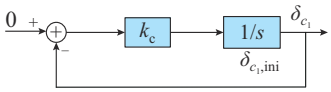

Fig. 12. Simplification of PACSE mode.

The parameters J, D_p, and K are designed according to the guidelines provided in [6] and [27]. Thus, they are not detailed in this paper.

B. Simulation Results During Symmetrical Grid Fault

To demonstrate the effectiveness of the proposed control strategy, a simulation verification is carried out. The simulation parameters are detailed in Table II.

TABLE II
SIMULATION PARAMETERS

Parameter	Symbol	Value
Normal grid voltage magnitude	V_{gn}	311 V
Nominal grid current amplitude	I_N	20 A
Rated angular frequency	ω_n	314 rad/s
Rated internal potential magnitude	U_{Cn}	311 V
DC-link voltage	V_{dc}	700 V
Filter inductance	L_f	3 mH
Filter capacitance	C_f	20 μF
Line inductance	L_g	6 mH
Virtual moment of inertia	J	0.06 kg·m^2
Damping coefficient	D_p	5 N·m·s
Inertia coefficient	K	7 A·s

During the period when the grid voltage sags to $0.5V_{gn}$, Fig. 13 illustrates the waveforms of PCC voltage, inverter-side current, and output power with the conventional VSG control. The results reveal that conventional VSG control results in considerable transient current and prolonged adjustment periods for both active power and reactive power during the symmetrical grid faults and voltage recovery mode, which complicates the codes for LVRT.

In contrast, Fig. 14 presents the simulation results with the proposed control strategy. The results illustrate the successful mitigation of transient current and swift achievement of target values for output power during the symmetrical grid faults. In addition, the PCC voltage can also quickly enter the steady state.

Additionally, Fig. 14 shows that the timer stops at 1.3 s, initiating the PACSE mode, which ends by approximately 1.4 s.

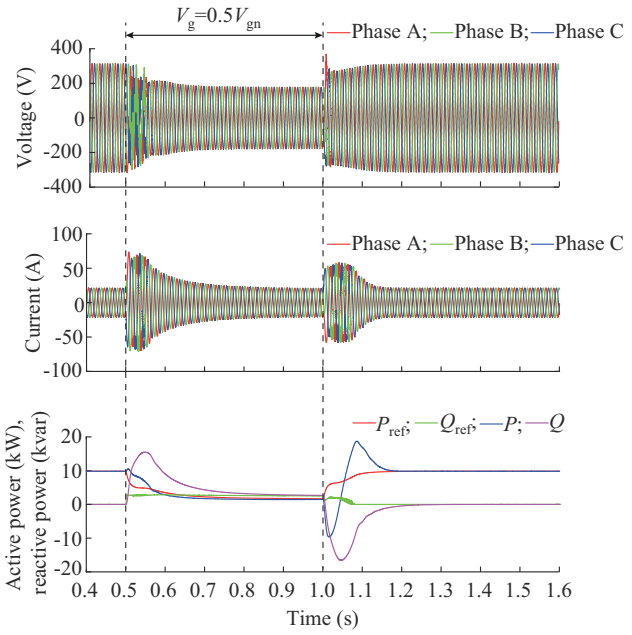

Fig. 13. Waveforms of PCC voltage, inverter-side current, and output power with conventional VSG control (V_g=0.5V_{gn}).

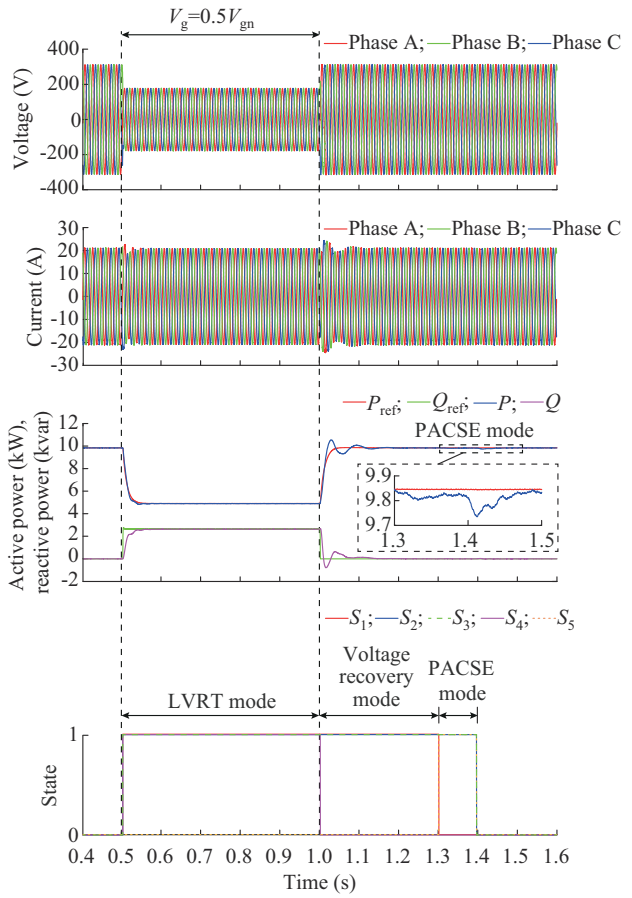

Fig. 14. Waveforms of PCC voltage, inverter-side current, output power, and switches with proposed control strategy (V_g=0.5V_{gn}).

The minimal impact on active power and current from PACSE mode proves the effectiveness of the proposed control strategy. Also, each switch operates accurately by the flowchart shown in Fig. 10.

The waveforms of IPC and power angle compensation are shown in Fig. 15, where E_{com} is the output of IPC.

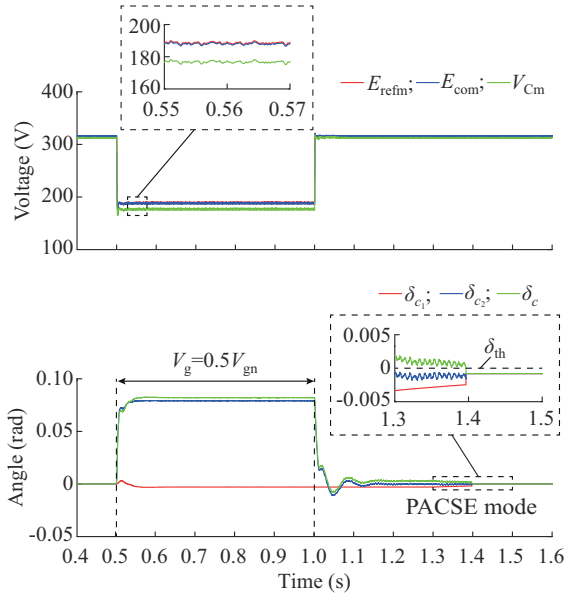

Fig. 15. Waveforms of IPC and power angle compensation (V_g=0.5V_{gn}).

In Fig. 15, E_{com} is coincident with E_{refm}, indicating that the IPC can accurately calculate the PCC voltage and compensate it to the RPCL, which effectively reduces the adjustment time. The DPAC visibly contributes to power angle compensation as $|\delta_{c_2}| >> |\delta_{c_1}|$ during the symmetrical grid faults. In the PACSE mode, δ_c gradually decreases to the threshold δ_{th}.

Figure 16 provides waveforms of PCC voltage, inverter-side current, output power, and switch with the proposed control strategy (V_g=0.2V_{gn}). The proposed control strategy demonstrates remarkable performance in suppressing transient currents and achieving fast power tracking.

Furthermore, the calculation of the power angle compensation δ_{c_2} is based on the PCC voltage. The simulation results shown in Figs. 14-16 indicate that the proposed control strategy can quickly stabilize the PCC voltage, thereby ensuring the calculation of δ_{c_2}.

The simulation results in Figs. 14-16 demonstrate the effectiveness of the proposed control strategy, which directly compensates the power angle and internal potential to reduce the regulatory effect of the power loop. Subsequently, Figs. 17 and 18 feature simulation results under various grid impedances and grid voltage sags. The proposed control strategy exhibits robust adaptability, ensuring that both output power and current comply with the grid codes for LVRT.

The waveforms in Figs. 14-18 show a large overshoot and slow recovery process. The main reasons are as follows: ① since the APCL continues to operate in the voltage recovery mode, its inertia characteristic leads to power overshoot and prolonged recovery time; and ② the power angle compensation term remains even after the end of the voltage recovery mode and cannot be cleared until at least the time T_{set} elapses.

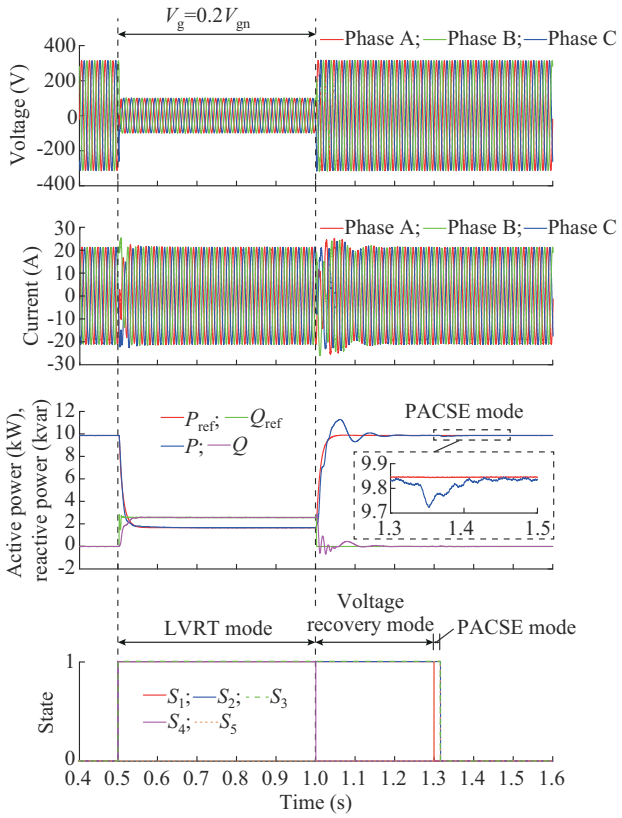

Fig. 16. Waveforms of PCC voltage, inverter-side current, output power, and switch with proposed control strategy (V_g=0.2V_{gn}).

Considering that changing the control structure or parameters of the APCL requires additional switches or algorithms, which would further increase the control complexity, the recovery performance is improved by adjusting the preset time T_{set}. The simulation results are illustrated in Supplementary Material C Fig. SC1. It is evident that reducing T_{set} allows the power angle compensation term to exit quickly, reducing both overshoot and recovery time of active power.

It should be noted that the transient synchronization stability is also an important index for the VSG. After adopting the power-oriented reference generation method described in (5)-(7), as the PCC voltage magnitude V_{Cm} decreases, the active power reference P_{ref} also decreases. This contributes to improving the transient stability of the VSG [24]. Subsequently, to further demonstrate that the power-oriented reference generation method can ensure the transient synchronous stability of the VSG, the phase portraits of the VSG during different symmetrical grid faults under different grid inductance are plotted through simulation, as shown in Fig. 19, where point A is the initial operating point. It should be noted that the transient stability problems caused by the grid faults often occur under weak grid conditions. Thereupon, a larger grid-side inductance is selected, resulting in a lower short-circuit ratio (SCR) [24].

In Fig. 19, even when the grid voltage sags to 0.1V_{gn} under weak grid conditions, the operating point starting from point A can still reach a steady state, i. e., $\Delta\omega = 0$ and δ remains constant. This indicates that the proposed control strategy can effectively ensure the transient synchronous stability of VSG.

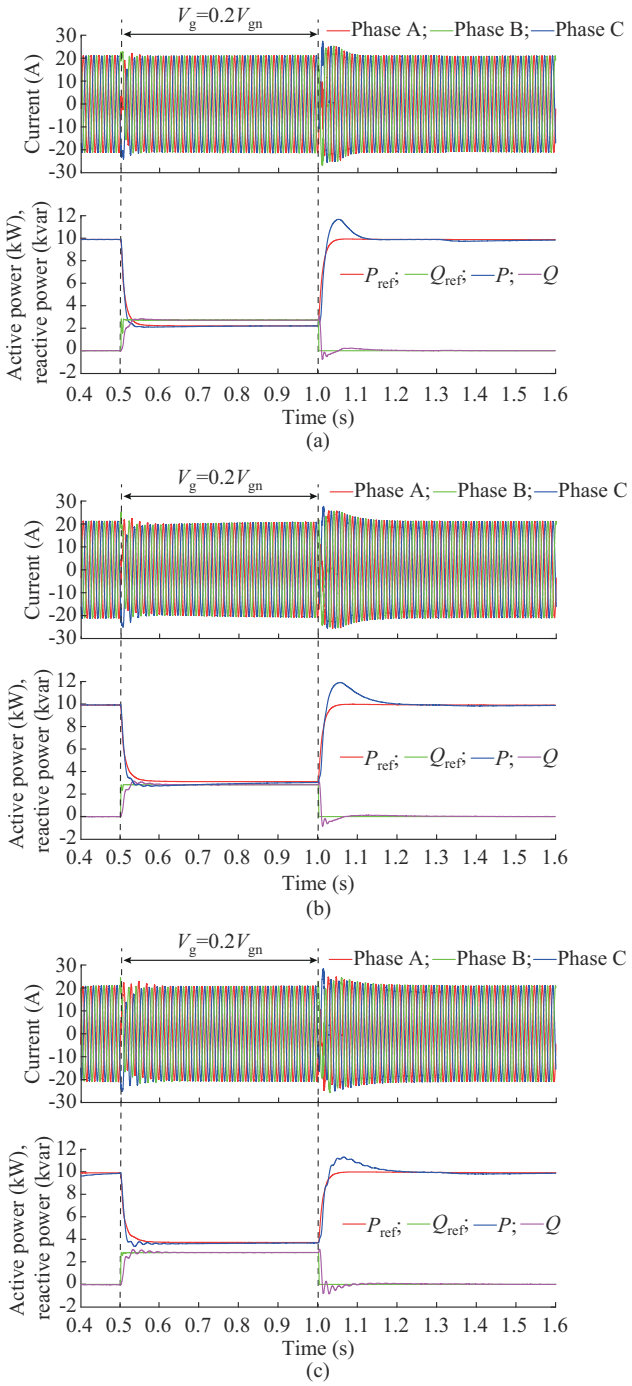

Fig. 17. Current and power waveforms under different grid impedances during LVRT. (a) L_g = 9 mH. (b) L_g = 15 mH. (c) L_g = 20 mH.

C. Comparisons with Different LVRT Control Strategies

The control strategies of the VSG during LVRT using internal potential and phase angle compensation are proposed in [14], [15]. The innovation of this paper is to propose a more precise compensation formula, as shown in (13) and (18). To demonstrate the innovation, comparative simulations are depicted in Fig. 20, where subscripts 1, 2, and 3 are the control strategies in [14], [15], and this paper, respectively. Moreover, to ensure a fair comparison, the parameters of the power control loops and VCCL in the simulations for [14] and [15] are kept consistent with those used in this paper.

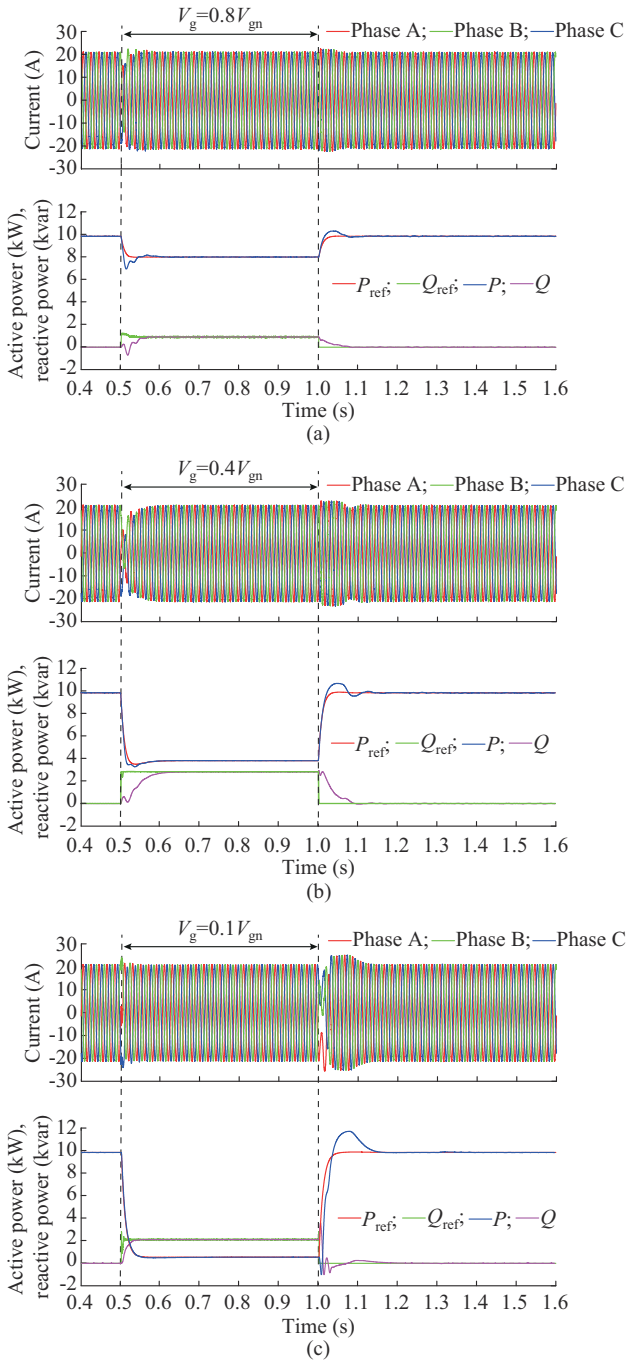

Fig. 18. Current and power waveforms under different grid voltage sags during LVRT. (a) $V_g = 0.8V_{gn}$. (b) $V_g = 0.4V_{gn}$. (c) $V_g = 0.1V_{gn}$.

These parameters are well tuned and the parameters involved in the strategies proposed in [14] and [15] are also adjusted by the recommended strategies.

In [14], compensation is only done when $E_{com} = V_{Cm}$. However, due to the reactive power requirements during the grid faults and the effects of VI, V_{Cm} does not match E_{dref} at the steady state, which is also validated in Fig. 15. Therefore, the RPCL still requires a longer time to reach the steady state.

In [15], a control strategy involving both IPC and power angle compensation is employed.

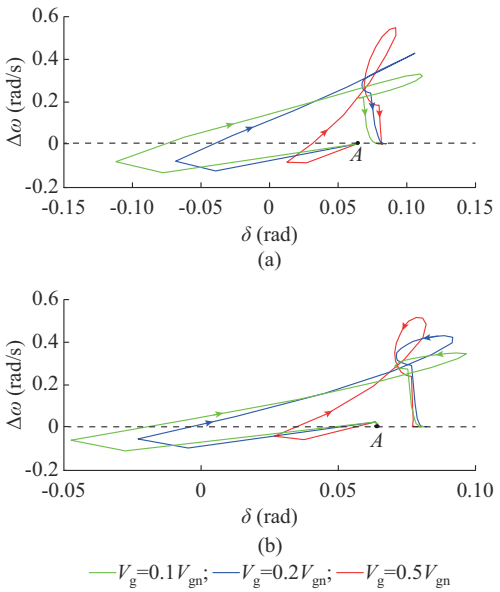

Fig. 19. Phase portraits of VSG during different symmetrical grid faults under different grid inductance. (a) $L_g = 20$ mH and $SCR = 2.3$. (b) $L_g = 30$ mH and $SCR = 1.5$.

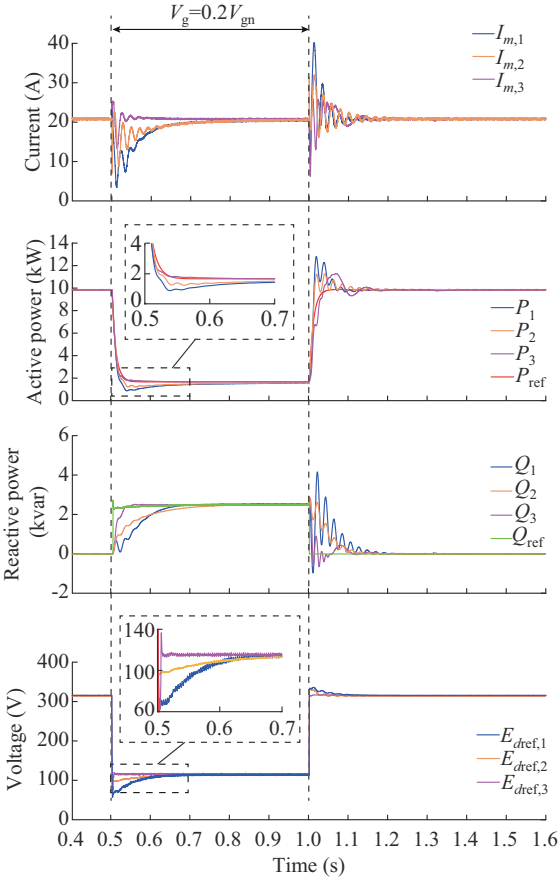

Fig. 20. Waveforms of current magnitude, output power, and RPCL output voltage with different LVRT control strategies.

The circuit and compensation formula are shown in Fig. 21 and (SC1) in Supplementary Material C, respectively, where i_{gabc} is the grid-side current, L_2 is the grid-side inductance of the LCL filter, and v_{Labc} is the output voltage of the LCL filter.

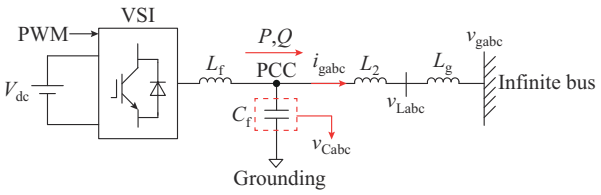

Fig. 21. Circuit in [15].

The IPC in [15] primarily serves to limit the current rather than directly estimate E_{dref} in the steady state. As a result, the control strategy in [15] does not significantly enhance the response speed of the RPCL compared with the control strategy in [14]. When calculating δ_{cd_0}, it is crucial to use the capacitor voltage components of the *dq* coordinates before the grid faults, as illustrated in Fig. 7. However, [15] does not change the coordinates during the grid faults, leading to inaccurate power angle compensation. This prevents the active power from swiftly tracking the setpoint. Additionally, [15] requires an additional set of voltage sensors to measure the output voltage of the LCL filter, which increases the equipment costs and overall complexity of the system setup.

In contrast to earlier control strategies shown in Fig. 20, the internal potential and power angle compensation formulas proposed in this paper offer enhanced accuracy without the need for additional voltage sensors. This refinement allows the output power to swiftly track the setpoint during the grid faults and maintain robust dynamic characteristics in the voltage recovery mode. Furthermore, the incorporation of TVI effectively reduces the transient current.

D. Simulation Results During Asymmetrical Grid Faults

The proposed control strategy also tackles the LVRT challenges presented by asymmetrical grid faults through the implementation of positive- and negative-sequence separation controls.

Supplementary Material C Fig. SC2 depicts the control diagram for the proposed control strategy equipped the positive- and negative-sequence separation controls. Figure 22 presents simulation results of the proposed control strategy during the asymmetric grid faults, where the positive-sequence components of the active power and reactive power are denoted as P_p and Q_p, respectively. Specifically, Fig. 22 shows a simultaneous voltage sag in phases A and B to $0.2V_{gn}$. The proposed control strategy effectively maintains the rapid power tracking and transient current suppression, underscoring its capability to efficiently address the asymmetrical grid faults.

V. Experimental Validation

To prove the effectiveness of the proposed control strategy, experimental validation is carried out. The experimental parameters are shown in Table III. The experimental hardware platform is shown in Fig. 23. The grid impedance is composed of series inductors. In addition, the grid simulator is used to achieve the grid faults.

Figure 24 presents the experimental results with conventional VSG control during grid fault ($V_g = 0.2V_{gn}$).

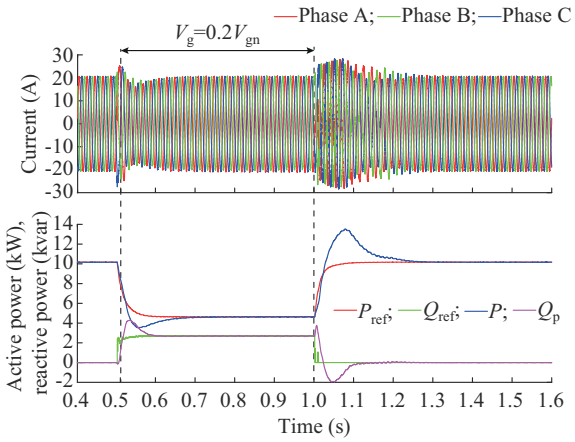

Fig. 22. Waveforms of inverter-side current and output power during asymmetrical grid faults.

TABLE III
Experimental Parameters

Parameter	Symbol	Values
Normal grid voltage magnitude	V_{gn}	100 V
Rated internal potential magnitude	U_{Cn}	100 V
DC-link voltage	V_{dc}	250 V
Virtual moment of inertia	J	0.005 kg·m^2
Damping coefficient	D_p	0.76 N·m·s
Inertia coefficient	K	3.3 A·s
Current threshold	I_{th}	12 A
Nominal grid current amplitude	I_N	10 A
Power thresholds	P_{th}, Q_{th}	100 W, 100 var

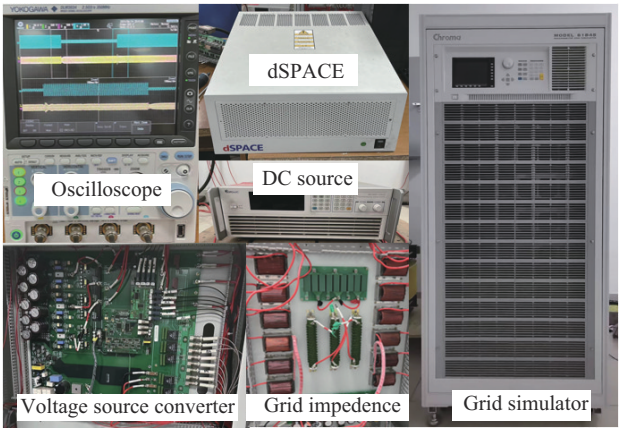

Fig. 23. Experimental hardware platform.

The VSG exhibits slow response within the power loop, coupled with considerable transient current. Conversely, Fig. 25 illustrates the experimental results with proposed control strategy during grid faults ($V_g = 0.2V_{gn}$). The proposed control strategy enables swift stabilization of the VSG and effective transient current suppression.

The above results validate the theoretical derivation and confirm the effectiveness of the proposed control strategy for improving the LVRT performance of VSG.

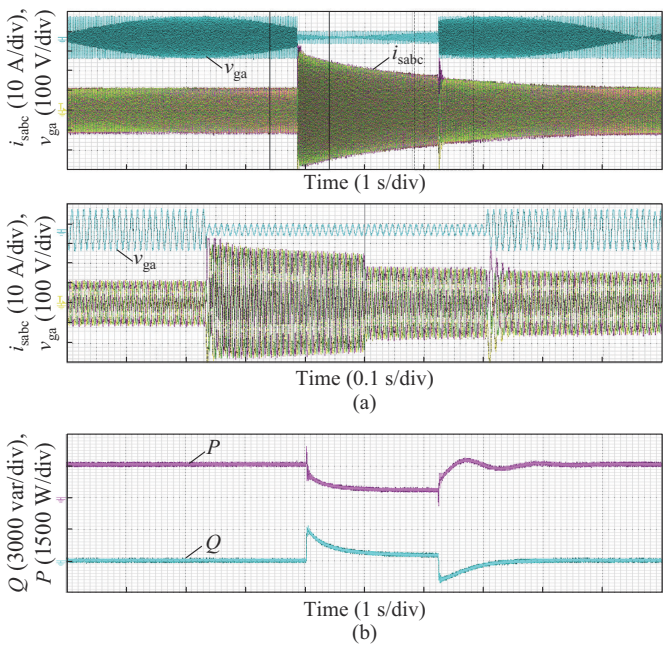

Fig. 24. Experimental results with conventional VSG control during grid faults ($V_g = 0.2V_{gn}$). (a) Grid voltage and inverter-side current. (b) PCC power.

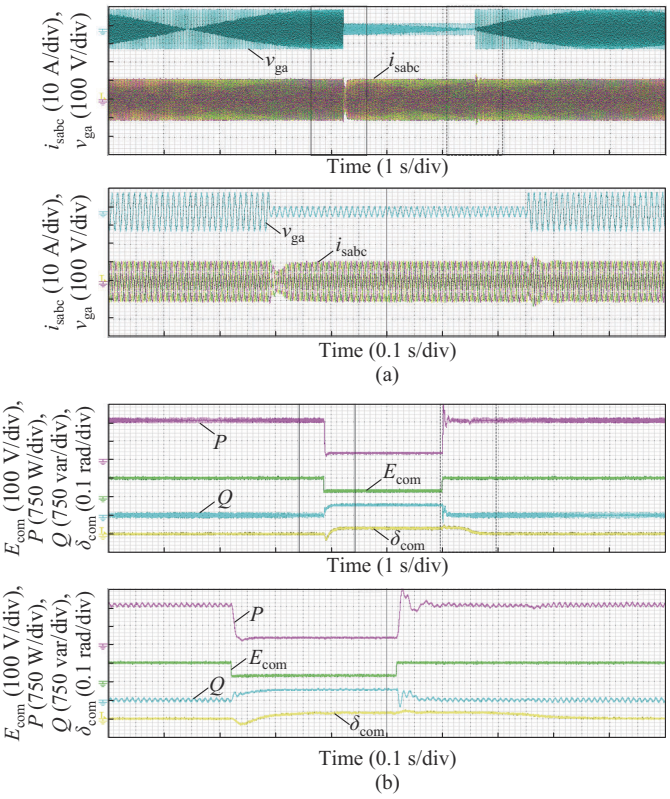

Fig. 25. Experimental results with proposed control strategy during grid faults ($V_g = 0.2V_{gn}$). (a) Grid voltage and inverter-side current. (b) PCC power, IPC, and power angle compensation.

VI. Conclusion

This paper examines the variations in power angle and PCC voltage of VSG during the grid faults and introduces a compound compensation control strategy. The conclusions of this paper are as follows:

1) The grid faults cause a reduction in the cutoff frequency of the power loop, thus leading to extended periods of power regulation and overcurrent.

2) The application of the internal potential and power angle compensation, which are derived from changes in the PCC voltage, active and reactive power references, and power angle, allows for rapid compensation of the power loop to its value in the steady state. This ensures that the VSG swiftly tracks the power references during grid faults.

3) Eigenvalue analysis and simulation studies confirm that the proposed control strategy effectively mitigates transient oscillations in the VSG during LVRT. The proposed control strategy demonstrates robust adaptability under different conditions. Furthermore, the large-signal model analysis reveals that TVI is instrumental in suppressing transient disturbances.

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