Self-adaptive Action and Parameter Optimization of DC Series-parallel Power Flow Controller for Fault Current Limiting in Bipolar DC Distribution Systems

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***Abstract*—DC series-parallel power flow controller (SP-PFC) is a highly efficient device to solve the problem of uncontrolled line current in the bipolar DC distribution system. However, its potential in fault current limiting is not fully explored. In this paper, a self-adaptive action strategy (SAAS) and a parameter optimization method of SP-PFC in bipolar DC distribution systems are proposed. Firstly, the common- and different-mode (CDM) equivalent circuits of the bipolar DC distribution system with SP-PFC in different fault stages are established, which avoids the line coupling inductance. Based on this, the influence of different parameters and line coupling inductance on the fault current limiting capability are investigated. It is found that the SP-PFC has the best fault current limiting capability when the capacitance and inductance of filter are inversely proportional. To realize the adaptability of fault current limiting capability under different fault severities, the SAAS of SP-PFC is proposed. The validity of the CDM equivalent circuits and parameter optimization method, and the effectiveness of the SAAS are verified by simulations and experiments.**

***Index Terms*—DC distribution system, series-parallel power flow controller (SP-PFC), line coupling inductance, parameter optimization, fault current limiting.**

I. Introduction

DUE to the advantages of flexibility and controllability, the voltage source converter (VSC) based DC distribution system technology is widely recognized as a promising one for the grid integration of renewable energy and DC load [1]. The low-voltage DC (LVDC) distribution systems are particularly appealing due to their efficiency, especially in data centers of various sizes, and their aptness for connecting distributed renewable energy sources [2], [3]. However, during a short-circuit fault, the fault current rapidly reaches the blocking threshold of the converter due to the discharge of DC bus capacitors [4]. The quick and selective detection and interruption of DC faults within milliseconds are crucial for ensuring the safety and power supply reliability in the LVDC distribution systems [5]. Therefore, the LVDC distribution systems should be equipped with high-speed DC circuit breakers (DCCBs) such as solid-state and hybrid circuit breakers to isolate DC faults [6]. However, the response speed of the existing fault detection and isolation methods is significantly slower than that of DC faults, making it inadequate to rely solely on high-speed DCCBs to isolate DC faults [7]. Appropriate fault current limiting measures are essential in DC distribution systems to reduce the demands on the protection system for high-speed action and effectively decrease the required interrupting capacity of DCCBs [8].

Nowadays, the fault current limiting reactors (CLRs) are often utilized to suppress fault currents. However, integrating a large CLR directly into DC systems can dampen the dynamic characteristics and operational stability, and slow down the isolation speed of DCCB. Its fault current limiting capability rapidly decreases with the increase of inductance value [9]. Therefore, various specialized solid-state fault current limiters (SSFCLs) and superconducting fault current limiters (SFCLs) are designed for DC distribution systems [10]. SSFCLs commonly utilize bridge circuits and modified topologies to transition to fault current limiting branches under fault conditions [10]-[12], which aim to safeguard the normal operation of DC distribution systems from the adverse effects of fault current limiters (FCLs). SFCLs swiftly respond after DC faults and recover rapidly upon isolation, showing extensive potential [13], [14]. Meanwhile, there are

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a variety of DCCBs with fault current limiting capability in the DC distribution system [15]-[17]. DCCBs with integrated FCLs enhance the fault clearing reliability and efficiency but may increase the cost of fabrication. The application of FCL in DC distribution systems is mature and becomes increasingly widespread. However, equipping each line in the multi-terminal DC distribution system with an FCL can significantly increase the costs. Therefore, a more cost-effective application is to utilize the available device in the DC distribution system to suppress the fault current in multi-terminal DC distribution systems. Active devices such as power flow controllers (PFCs) can regulate the power flow [18]. The PFC can be used to suppress the fault current by outputting a reverse voltage during a short-circuit fault, which can obviate the need for an FCL. Therefore, the utilization of PFC can eliminate additional investments.

The comparison of advantages and disadvantages of different fault current limiting devices are shown in Table I. The PFCs are notably advantageous due to the low cost, no impact on system, and the fault current limiting capability is medium. In [19], an H-bridge inter-line current flow controller (CFC) with fault current limiting and interrupting capability is proposed. In fault stages, the fault current limiting is achieved through the usage of thyristor-controlled inductive inputs. In [20], a modular multi-terminal DC current controller with fault current limiting capacity designed for high-voltage levels is discussed, emphasizing its effectiveness in high-capacity scenarios. There are many prestigious studies that utilize the potential capability of power flow controllers to simultaneously control power flow under normal conditions and manage faults under fault conditions [21]-[24]. The system efficiency is enhanced, costs are reduced, and rapid fault response is achieved through dual-function devices. These dual-function devices that resemble series CFCs are promising for multi-terminal high-voltage DC (HVDC) systems. However, the CFCs regulate power flow by sharing a series capacitor between two independent DC lines, which can lead to current ripple [25]. CFCs are predominantly employed in high-voltage and large-capacity transmission systems to optimize costs due to their structural characteristics.

TABLE I
COMPARISON OF ADVANTAGES AND DISADVANTAGES OF DIFFERENT FAULT CURRENT LIMITING DEVICES

Fault current limiting device	Impact on system	Fault current limiting capability	Complexity	Cost	Power loss
CLR	Dampen dynamic characteristics	Decrease with increase of inductance	Low	Low	Low
SFCL	No impact	High	Medium	High	High
SSFCL	No impact	High	High	High	Low
SSCB	No impact	Medium	High	High	Low
PFC	No impact	Medium	Low	Low	Low

For LVDC distribution systems, a combined device of a series-parallel power flow controller (SP-PFC) integrated with a DCCB is proposed in [26]. The application of SP-PFC in DC distribution systems exhibits certain benefits in terms of size, power loss, and cost [18]. However, its potential in fault current limiting capability remains underexploited. In [27], a coordination strategy of SP-PFC and hybrid DCCB is proposed to suppress the fault current in medium-voltage DC distribution systems, and a fault current calculation model is derived. However, the derived model in [27] is only suitable for monopolar systems.

An emergency control of SP-PFC is proposed to suppress fault currents. However, the activation of emergency control relies on commands of DC protection system, which will introduce detection delay [28]. This can easily lead to a mismatch between the speed of the fault current limiting action and fault severity [29]. Therefore, it is imperative to investigate a self-adaptive action strategy (SAAS) of SP-PFC with its own fault detection system. Additionally, the parameter optimization method of SP-PFC is proposed to improve its fault current limiting capability. The symmetric bipolar design offers advantages over the monopolar structure in terms of bulk power transmission, DC fault tolerance, and control [30]. However, the influence of line coupling inductance on both the fault current and the fault current limiting characteristics cannot be ignored.

To fill the above research gaps, this paper explores the fault current limiting characteristics of SP-PFC in bipolar DC distribution systems considering line coupling inductance. An SAAS and a parameter optimization method of SP-PFC for fault current limiting are obtained. The contributions of this paper are as follows.

1) The common- and different-mode (CDM) equivalent circuits of the bipolar DC distribution system with SP-PFC in different fault stages are established. The CDM equivalent circuits not only enable the decoupling calculation of fault currents but also quantify the fault current limiting contribution of SP-PFC.

2) Based on the CDM equivalent circuits, the influence of different parameters on the fault current limiting contribution of SP-PFC are rigorously analyzed. Then, a parameter optimization method is proposed to improve the fault current limiting capability of SP-PFC.

3) The SAAS of SP-PFC is proposed to improve the adaptability of its fault current limiting capability in different fault stages, which enhances the fault current limiting efficiency by adaptively adjusting the emergency control activation time based on the fault severity.

The remainder of this paper is organized as follows. Section II derives the fault modulus analysis model of bipolar DC distribution system with SP-PFC. Section III shows analysis of the fault current limiting characteristics and the parameter optimization method of SP-PFC. Section IV investigates the SAAS of SP-PFC. Section V presents the simula-

tion and experimental results. The conclusions are illustrated in Section VI.

II. Fault Modulus Analysis Model of Bipolar DC Distribution System with SP-PFC

A. Topology and Operating Modes of SP-PFC

Figure 1 shows the schematic diagram of the bipolar DC distribution system with SP-PFC, including its topology [18]. The SP-PFC consists of the dual active bridge (DAB), DCCB, and the full-bridge converter (FBC). The main parameters in Fig. 1 are listed in Supplementary Material A. The fundamental principle of using the SP-PFC for fault current limiting involves generating a reverse voltage by adjusting the DAB and FBC. The DAB employs constant voltage control to sustain the output voltage at a steady level [27]. Figure 2 shows different switching modes of the FBC, which correspond to different operating modes of SP-PFC. When a fault occurs, the operating mode of the SP-PFC transitions from Mode 1 to Mode 2, and finally to Mode 3. Specifically, the fault isolation is achieved by opening the main circuit branch of the DCCB and switching the FBC to bypass control mode.

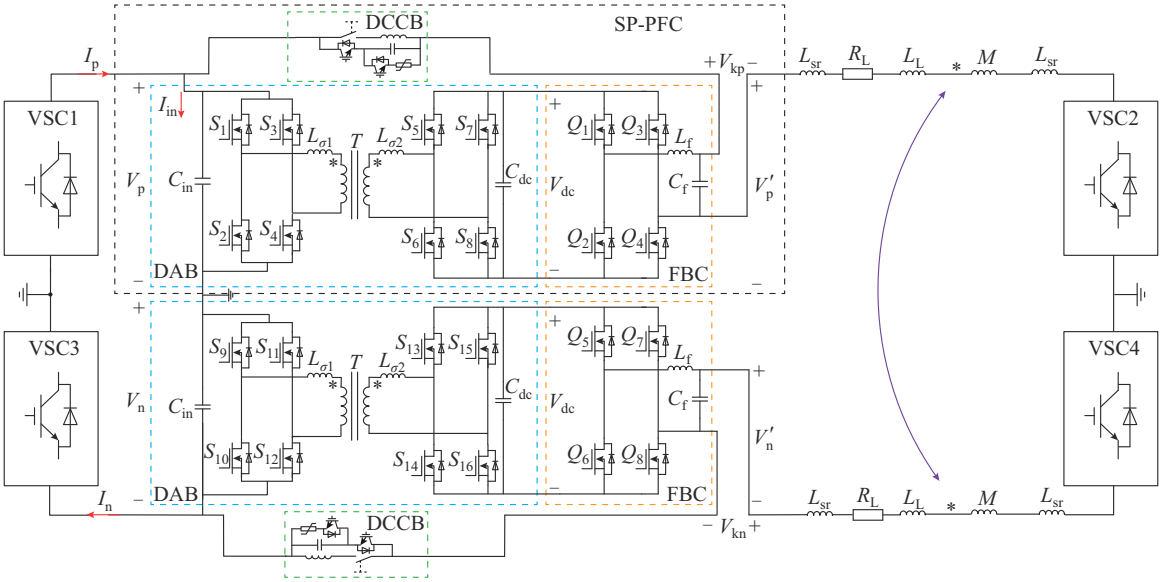

Fig. 1. Schematic diagram of bipolar DC distribution system with SP-PFC.

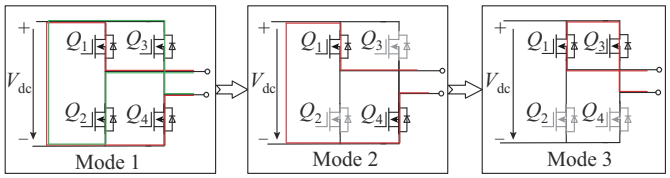

Fig. 2. Different operating modes of SP-PFC.

In Mode 1, although a fault occurs, the emergency control is not triggered. The SP-PFC remains in power flow control mode, managing the line power flow without switching to emergency operating modes.

In Mode 2, the emergency control is activated. Switches Q_1 and Q_4 are turned on, while switches Q_2 and Q_3 are blocked. Consequently, the SP-PFC generates a reverse voltage to limit the fault current.

In Mode 3, the bypass control is activated. Switches Q_1 and Q_3 are turned on. Meanwhile, the emergency control is deactivated.

B. Frequency-domain Equivalent Circuit in Different Fault Stages with SP-PFC

Taking the unipolar short-circuit fault as an example, the corresponding equivalent circuit is obtained. Within milliseconds after the fault, the VSC can be equated to a capacitor discharge [31], which can be modeled in the frequency-domain as an equivalent voltage source $U_{dc}(s)$ in series with an equivalent impedance $Z_a(s)$:

$$\begin{cases} U_{dc}(s) = \dfrac{U_{dc}}{s} \\ Z_a(s) = \dfrac{1}{sC_a} \end{cases} \tag{1}$$

where U_{dc} and C_a are the initial voltage and equivalent capacitance of VSC, respectively.

This paper focuses on analyzing the fault current limiting stage prior to the tripping of DCCB. According to Mode 1 and Mode 2 of the SP-PFC described above, the fault current limiting stage can be divided into two stages: the natural response stage (stage I) and the emergency control stage (stage II). The equivalent circuit for the bypass control stage is not included in the analysis conducted in this paper.

In stage I, the SP-PFC operates in Mode 1. The output power equals the input power, with the assumption that the switching loss of SP-PFC is ignored. Therefore, the output voltage V_k satisfies:

$$\begin{cases} V_p I_{in} = V_k I_f + I_{in}^2 R_\sigma \\ I_{in} = \dfrac{I_f}{n} \end{cases} \tag{2}$$

where V_p is the positive line voltage on the input side of the SP-PFC; R_σ is the leakage resistance of the isolation transformer; n is the ratio of the isolation transformer; and I_f is the line fault current.

According to (2), the expression of the output voltage $V_k(s)$ can obtained as:

$$V_k(s)=\frac{1}{n}V_p(s)-\frac{R_\sigma}{n^2}I_f(s) \tag{3}$$

The frequency-domain equivalent circuit with SP-PFC in stage I is shown in Fig. 3.

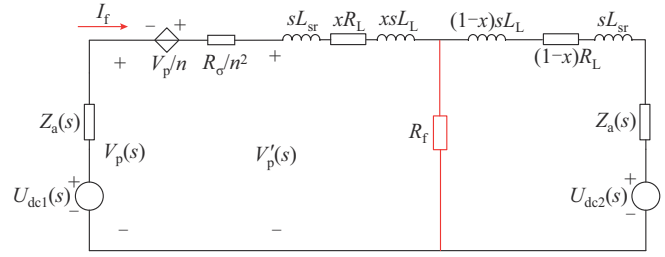

Fig. 3. Frequency-domain equivalent circuit with SP-PFC in stage I.

In stage II, the SP-PFC operates in Mode 2. The input voltage of FBC equals the voltage on the secondary side of the isolation transformer U_{T2}, and the filter inductor L_f and capacitor C_f are connected to the circuit. The equivalent model simplification process for SP-PFC in stage II is shown in Fig. 4.

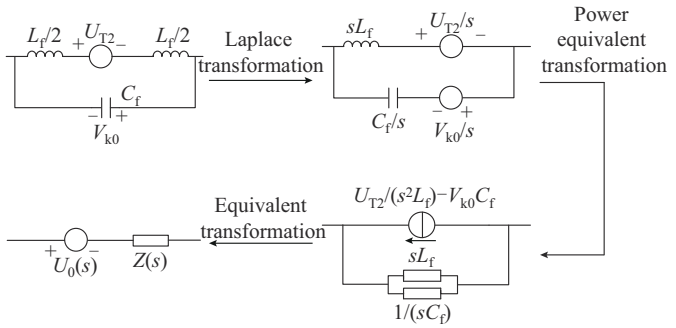

Fig. 4. Equivalent model simplification process for SP-PFC in stage II.

The frequency-domain equivalent circuit with SP-SFC in stage II is shown in Fig. 5.

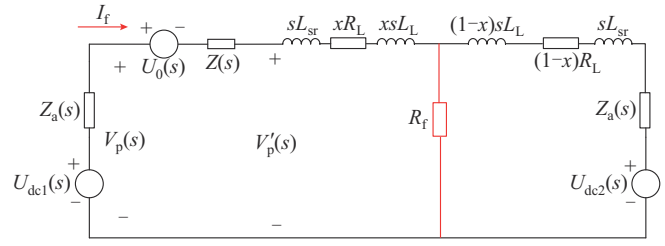

Fig. 5. Frequency-domain equivalent circuit with SP-PFC in stage II.

Therefore, the expression of the output voltage of SP-PFC in stage II is given as:

$$V_k(s)=U_0(s)+I_f(s)Z(s) \tag{4}$$

$$\begin{cases} U_0(s)=\left(\dfrac{U_{T2}}{2s^2L_f}-V_{k0}C_f\right)Z(s)=-\dfrac{sL_f}{1+L_fC_fs^2}V_{k0}C_f+ \\ \qquad\dfrac{U_{T2}}{s(1+L_fC_fs^2)} \\ Z(s)=sL_f//\dfrac{1}{sC_f}=\dfrac{sL_f}{1+s^2L_fC_f} \end{cases} \tag{5}$$

where V_{k0} is the initial voltage of capacitance.

C. Equivalent Modulus Model of Bipolar DC Distribution Systems with SP-PFC

Directly including line coupling inductance in the two-pole line equations complicates the model and makes it challenging to solve. Meanwhile, ignoring the line coupling inductance inevitably leads to inaccurate calculation of fault current. Therefore, this paper utilizes the decoupling matrix $\boldsymbol{A}$ in [32] to convert the positive and negative electrical quantities into CDM components, thereby realizing the decoupling of the calculation of fault current and analysis of fault current limiting characteristics of SP-PFC. By eliminating the line coupling inductance of bipolar DC distribution system, the equivalent modulus model becomes simpler and the computation time is significantly reduced. This improvement is crucial for more precise threshold setting for fault current limiting measures and better parameter selection.

The influence of line coupling inductance on pole-to-ground (PTG) faults varies depending on the fault location. It is important to note that this influence is significantly less than that observed in pole-to-pole (PTP) faults [33]. Therefore, the derived equivalent circuit of unipolar fault is suitable to analyze PTG faults. However, for analyzing PTP faults in bipolar DC distribution systems with SP-PFC, it is essential to derive the CDM equivalent circuit that includes SP-PFC. In this paper, the single-end common-mode (CM) and different-mode (DM) currents in the CDM equivalent circuit are utilized for fault discrimination. $D(I_0)$ and $D(I_1)$ are the differential quantities of CM and DM currents, respectively; and D_{set} is the protection threshold. If $D(I_1)$ exceeds D_{set}, it indicates an internal fault, followed by the utilization of D_{set} for faulty pole selection. If the absolute value of $D(I_0)$ falls below D_{set}, it indicates the presence of PTP faults. In such cases, the emergency control of both positive and negative SP-PFCs is activated, and the CDM equivalent circuits are employed to determine their activation time. Conversely, if the absolute value of $D(I_0)$ exceeds D_{set}, it indicates the presence of PTG faults. In such cases, only the SP-PFC on the fault line activates its emergency control, and the equivalent circuit of unipolar fault is employed to determine its activation time.

To derive the CDM equivalent circuit, it is necessary to derive the CDM circuits of VSC, line, fault port, and SP-PFC. The CDM circuits of VSC, line, and fault port in modal component space can be found in [32]. Therefore, the aim is to obtain the equivalent models of SP-PFC in modal component space in different fault stages.

In stage I, the voltages at two ports of SP-PFC, analyzed in the polar component space, can be derived through (3), which are given as:

$$\begin{bmatrix} V_{\mathrm{p}}'(s) \\ V_{\mathrm{n}}'(s) \end{bmatrix} = \frac{n+1}{n}\begin{bmatrix} V_{\mathrm{p}}(s) \\ V_{\mathrm{n}}(s) \end{bmatrix} - \frac{R_\sigma}{n^2}\begin{bmatrix} I_{\mathrm{p}}(s) \\ I_{\mathrm{n}}(s) \end{bmatrix} \tag{6}$$

where $V_{\mathrm{p}}'(s)$ and $V_{\mathrm{n}}'(s)$ are the positive and negative line voltages on the output side of SP-PFC, respectively; $V_{\mathrm{p}}(s)$ and $V_{\mathrm{n}}(s)$ are the positive and negative line voltages on the input side of SP-PFC, respectively; and $I_{\mathrm{p}}(s)$ and $I_{\mathrm{n}}(s)$ are the positive and negative line currents, respectively.

Then, the voltages at two ports, analyzed in modal component space, can be derived through (6), which satisfy:

$$\begin{bmatrix} V_0'(s) \\ V_1'(s) \end{bmatrix} = \boldsymbol{A}\begin{bmatrix} V_{\mathrm{p}}'(s) \\ V_{\mathrm{n}}'(s) \end{bmatrix} = \frac{n+1}{n}\begin{bmatrix} V_0(s) \\ V_1(s) \end{bmatrix} - \frac{R_\sigma}{n^2}\begin{bmatrix} I_0(s) \\ I_1(s) \end{bmatrix} \tag{7}$$

where $V_0'(s)$ and $V_1'(s)$ are the CM and DM line voltages on the output side of SP-PFC, respectively; $V_0(s)$ and $V_1(s)$ are the CM and DM line voltages on the input side of SP-PFC, respectively; and $I_0(s)$ and $I_1(s)$ are the CM and DM line currents, respectively.

Figure 6 shows the equivalent models of the SP-PFC in stage I.

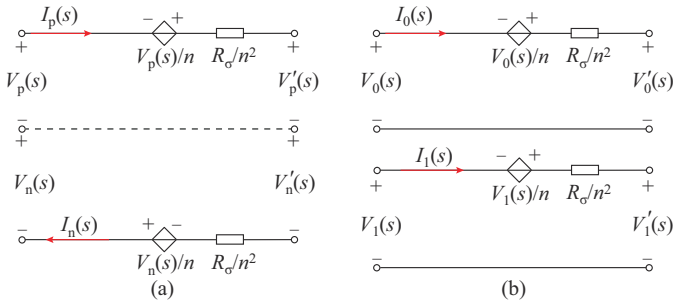

Fig. 6. Equivalent models of SP-PFC in stage I. (a) In polar component space. (b) In modal component space.

In stage II, the voltages at two ports of SP-PFC in polar component space can be derived through (4), which satisfy:

$$\begin{bmatrix} V_{\mathrm{p}}(s) \\ V_{\mathrm{n}}(s) \end{bmatrix} - \begin{bmatrix} V_{\mathrm{p}}'(s) \\ V_{\mathrm{n}}'(s) \end{bmatrix} = U_0(s)\begin{bmatrix} 1 \\ 1 \end{bmatrix} + Z(s)\begin{bmatrix} I_{\mathrm{p}}(s) \\ I_{\mathrm{n}}(s) \end{bmatrix} \tag{8}$$

The voltages at two ports, analyzed in modal component space, can be derived through (8), which satisfy:

$$\begin{bmatrix} V_0(s) \\ V_1(s) \end{bmatrix} - \begin{bmatrix} V_0'(s) \\ V_1'(s) \end{bmatrix} = \begin{bmatrix} U_0(s) \\ 0 \end{bmatrix} + Z(s)\begin{bmatrix} I_0(s) \\ I_1(s) \end{bmatrix} \tag{9}$$

Figure 7 shows the equivalent models of the SP-PFC in stage II.

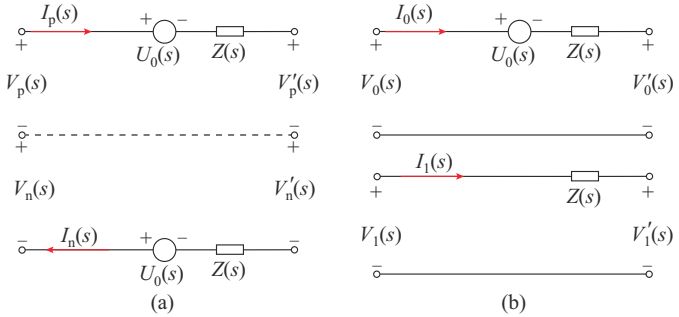

Fig. 7. Equivalent models of SP-PFC in stage II. (a) In polar component space. (b) In modal component space.

The CDM equivalent circuits in different fault stages are shown in Fig. 8, where $I_{0,1}$ and $I_{1,1}$ are the CD and DM line currents in modal space in stage I, respectively; and $I_{0,2}$ and $I_{1,2}$ are the CD and DM line currents in modal space in stage II, respectively. As shown in Fig. 8, the CDM equivalent circuits are shown to operate independently without any coupling. During PTP faults, the positive and negative poles are symmetrical, resulting in equal fault currents in the positive and negative pole lines, which correspond to the DM line currents [32].

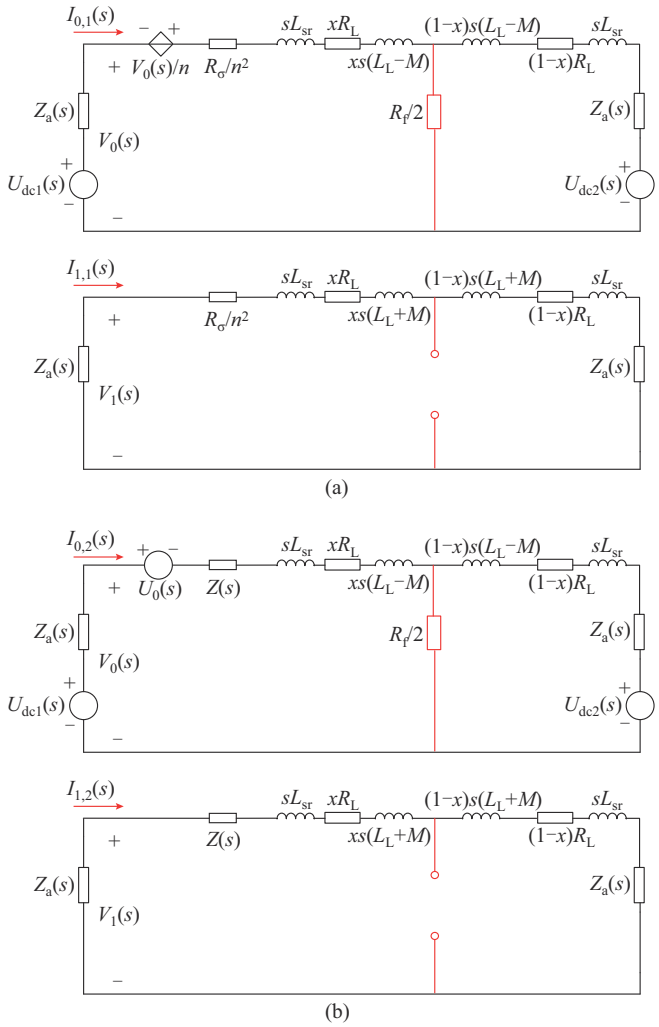

Fig. 8. CDM equivalent circuits in different fault stages. (a) In stage I. (b) In stage II.

As shown in Fig. 8(a), the fault current in stage I is given as:

$$I_{\mathrm{f},1}(s) = \frac{\frac{n+1}{n}U_{\mathrm{dc1}}(s)}{Z_{1,1}+Z_{2,1}/\!/\frac{R_{\mathrm{f}}}{2}} + \frac{U_{\mathrm{dc2}}(s)}{Z_{2,1}+Z_{1,1}/\!/\frac{R_{\mathrm{f}}}{2}}\frac{R_{\mathrm{f}}}{2Z_{1,1}+R_{\mathrm{f}}} \tag{10}$$

$$\begin{cases} U_{\mathrm{dc1}}(s) = \dfrac{U_0}{s} \\ Z_{1,1} = \dfrac{(n+1)Z_{\mathrm{a}}(s)}{n} + \dfrac{R_\sigma}{n^2} + sL_{\mathrm{sr}} + sx(L_{\mathrm{L}}-M) + xR_{\mathrm{L}} \\ Z_{2,1} = Z_{\mathrm{a}}(s) + sL_{\mathrm{sr}} + s(1-x)(L_{\mathrm{L}}-M) + (1-x)R_{\mathrm{L}} \end{cases} \tag{11}$$

where R_f is the fault transition resistance; M is the line coupling inductance; L_{sr} is the fault transition inductance; R_L is the line resistance; x is the proportion of distance between the fault point and VSC 1 to the total line length; and $U_{dc1}(s)$ is the power supply voltage of VSC 1.

The influence of $U_{dc2}(s)$ on the fault current is very small and can be ignored. And the SP-PFC output voltage in stage I $V_{k,1}(s)$ is given as:

$$V_{k,1}(s)=-\frac{U_{dc1}(s)-I_{0,1}(s)Z_a(s)}{n}+\frac{R_\sigma}{n^2}I_{0,1}(s) \tag{12}$$

As shown in Fig. 8(b), the fault current in stage II is given as:

$$I_{f,2}(s)=\frac{U_{dc1}(s)-U_0(s)}{Z_{1,2}+Z_{2,2}//\dfrac{R_f}{2}}+\frac{U_{dc2}(s)}{Z_{2,2}+Z_{1,2}//\dfrac{R_f}{2}}\frac{R_f}{2Z_{1,2}+R_f} \tag{13}$$

$$\begin{cases}Z_{1,2}=Z_a(s)+Z(s)+sL_{sr}+sx(L_L-M)+xR_L\\ Z_{2,2}=Z_a(s)+sL_{sr}+s(1-x)(L_L-M)+xR_L\end{cases} \tag{14}$$

The output voltage of SP-PFC in stage II $V_{k,2}(s)$ can be expressed as:

$$V_{k,2}(s)=U_0(s)+I_{0,2}(s)Z(s) \tag{15}$$

The fault current limiting contribution of SP-PFC in the fault current limiting stage is closely related to the integral value of its output voltage [9]. To theoretically analyze the fault current limiting characteristics of SP-PFC in stage II, the fault current is assumed to increase linearly. The time-domain expression of the fault current in stage II can be expressed as:

$$I_{f,2}(t)=kt+b \tag{16}$$

where k and b are the rise rate and initial value of fault current in stage II, respectively.

According to (15) and (16), $V_{k,2}(t)$ can be expressed as:

$$V_{k,2}(t)=U_{T2}+kL_f+\frac{L_f b\sin\dfrac{t}{\sqrt{L_fC_f}}}{\sqrt{C_f}}-(U_{T2}+V_{k0}+kL_f)\cos\frac{t}{\sqrt{L_fC_f}} \tag{17}$$

Assuming the duration of stage II is Δt, the fault current limiting contribution S_{PFC} in stage II can be expressed as:

$$S_{PFC}=(U_{T2}+kL_f)\Delta t+L_f b\left(1-\cos\frac{\Delta t}{\sqrt{L_fC_f}}\right)-(U_{T2}+V_{k0}+kL_f)\sqrt{L_fC_f}\sin\frac{\Delta t}{\sqrt{L_fC_f}} \tag{18}$$

III. Analysis of Fault Current Limiting Characteristics and Parameter Optimization Method of SP-PFC

The CDM equivalent circuits shown in Fig. 8 are utilized in this section. The parameters of VSC and SP-PFC in CDM equivalent circuits are shown in Table II.

TABLE II
Parameters of VSC and SP-PFC in CDM Equivalent Circuits

Parameter	Value	Parameter	Value
U_{dc}	380 V	n	10
C_a	3 mF	C_f	0.8 mF
L_L	3.5 mH	L_f	0.5 mH
R_L	1.8 Ω	U_{T2}	35 V
M	0.9 mH	R_σ	0.1 Ω

A. Influence of R_f and L_{sr} on Current Limiting Characteristics of SP-PFC

Firstly, the influence of R_f and L_{sr} on current limiting characteristics of SP-PFC is analyzed. Figure 9 shows I_f and V_k under different R_f and L_{sr}. As shown in Fig. 9, when R_f and L_{sr} change, the amplitude of I_f changes significantly but the amplitude of V_k is slightly affected. Therefore, the fault current limiting contribution of SP-PFC is little affected by the circuit parameters.

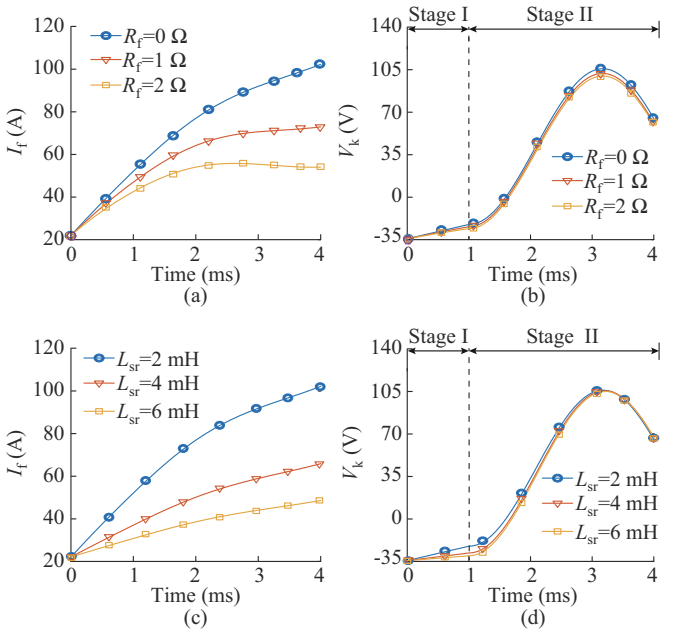

Fig. 9. I_f and V_k under different R_f and L_{sr}. (a) I_f under different R_f. (b) V_k under different R_f. (c) I_f under different L_{sr}. (d) V_k under different L_{sr}.

B. Influence of Different Parameters on Current Limiting Characteristics of SP-PFC

According to (15), the output voltage of SP-PFC in stage II is given as:

$$V_{k,2}(s)=U_0(s)+I_{f,2}(s)Z(s)=-\frac{L_fC_fs}{1+L_fC_fs^2}V_{k0}+\frac{U_{T2}}{s(1+L_fC_fs^2)}+\frac{L_fs}{1+L_fC_fs^2}I_{f,2}(s) \tag{19}$$

Accordingly, the output voltage is influenced by C_f and L_f. Figure 10 shows I_f and V_k under different C_f and L_f. As shown in Fig. 10(b) and (d), the response speed of SP-PFC is faster with smaller C_f, and the maximum output voltage increases with L_f. Therefore, matching the parameters of C_f

and L_f is crucial to increase the fault current limiting contribution of SP-PFC. This is precisely the key to enhancing fault current limiting contribution through parameter optimization.

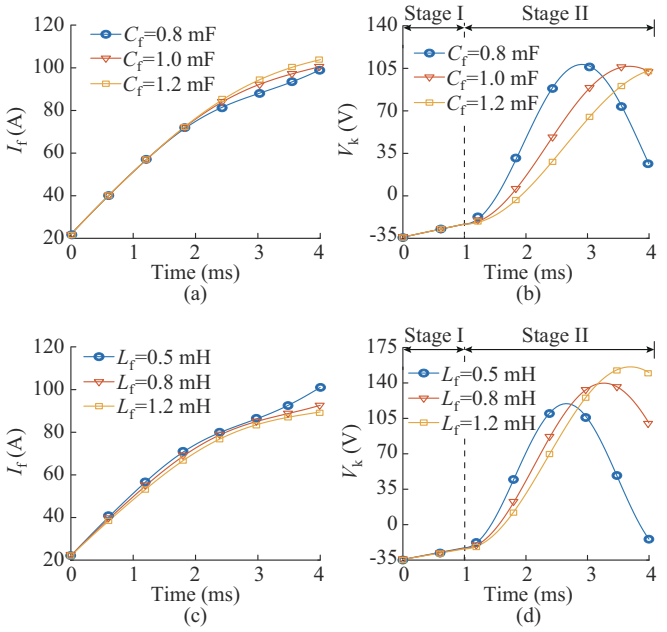

Fig. 10. I_f and V_k under different C_f and L_f. (a) I_f under different C_f. (b) V_k under different C_f. (c) I_f under different L_f. (d) V_k under different L_f.

The DCCB interrupting current and the fault current limiting contribution of SP-PFC under different C_f and L_f are shown in Fig. 11.

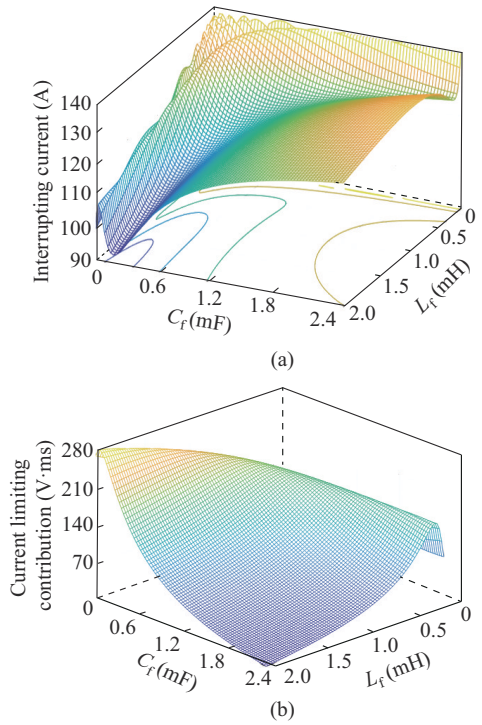

Fig. 11. DCCB interrupting current and fault current limiting contribution under different L_f and C_f. (a) DCCB interrupting current. (b) Fault current limiting contribution.

Once L_f is determined, there exists only an unique value of C_f that minimizes the DCCB interrupting current while maximizing the fault current limiting contribution of SP-PFC. The data points in Fig. 12 are fitted in two dimensions to obtain a fitted curve with a high degree of 95%. The expression of fitted curve is given as:

$$C_f = \frac{a}{L_f} \tag{20}$$

where a is an optimal parameter.

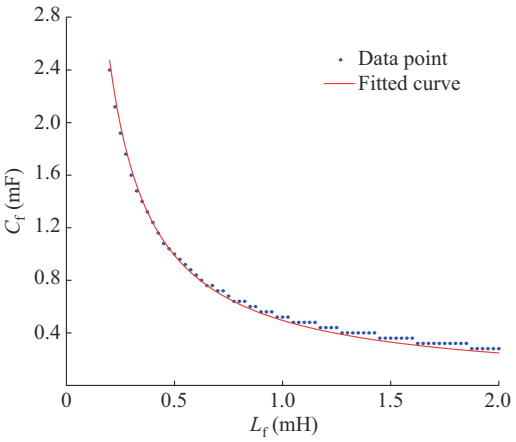

Fig. 12. Optimization of data points and fitted curve.

The parameter optimization method can be theoretically validated by assessing the fault current limiting contribution of SP-PFC. To Satisfy the fitted curve proposed in (20), S_{PFC} according to (18) is given as:

$$S_{PFC} = (U_{T2} + kL_f)\left(\Delta t - \sqrt{a}\sin\frac{\Delta t}{\sqrt{a}}\right) + bL_f\left(1 - \cos\frac{\Delta t}{\sqrt{a}}\right) - V_{k0}\sqrt{a}\sin\frac{\Delta t}{\sqrt{a}} \tag{21}$$

According to (21), there is an optimal parameter a within a reasonable range of 0.3-0.5 mH, which maximizes S_{PFC} and remains unchanged regardless of different L_f. Meanwhile, S_{PFC} increases with the increase of L_f after the optimization, which is fully consistent with the results shown in Fig. 11(b).

Based on the above analysis, it is recommended to configure C_f according to (20), which is the principle of the parameter optimization method. Under this principle, the fault current limiting contribution of SP-PFC can be increased by appropriately increasing L_f. However, it should not be overlooked that the power electronics of SP-PFC will face higher voltage stress. Besides, when C_f is very small, its voltage regulation capability is inevitably affected during normal operation. According to (17), the maximum voltage that the SP-PFC can withstand is given as:

$$V_{max} = U_{T2} + kL_f + \frac{L_f b}{\sqrt{a}}\sqrt{L_f} \tag{22}$$

Therefore, the selection of L_f must guarantee that the maximum voltage V_{max} remains within the voltage tolerance range of its power electronic devices during faults. Consider-

ing the corner frequency of LC filter, it effectively attenuates harmonics beyond the cutoff frequency. However, excessively low cutoff frequencies may adversely affect the dynamic performance of the system. To mitigate the influence of parameter optimization method on both the filtering capability and dynamic performance of LC filters, this paper evaluates the switching frequency and filtering needs of the FBC. Consequently, the corner frequency is set to be 220 Hz. As a result, parameter a is chosen within the range of 0.42-0.52 mH·mF.

C. Influence of Line Coupling Inductance on Current Limiting Characteristics of SP-PFC

With the CDM equivalent circuits, the influence of the line coupling inductance M on I_f and V_k can be analyzed. The fault position determines the influence of M [33]. Figure 13 shows the influence of M on I_f and V_k at different fault positions.

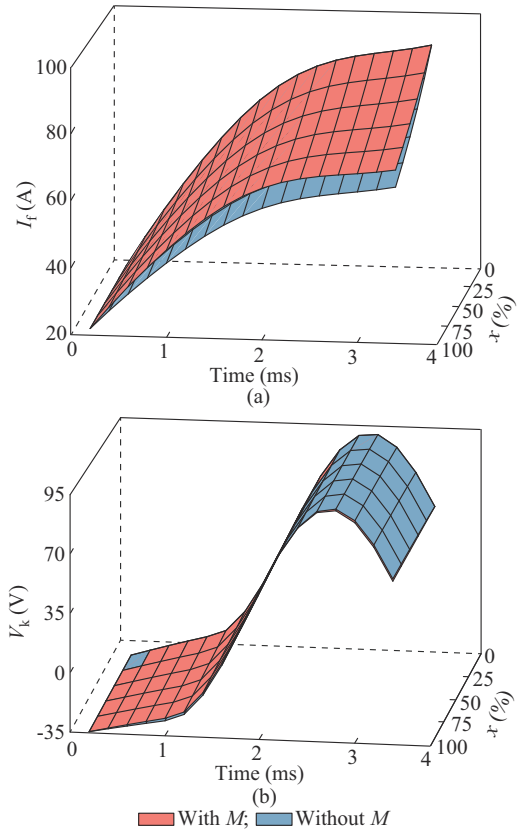

Fig. 13. Influence of M on I_f and V_k at different fault positions. (a) I_f. (b) V_k.

In Fig. 13(a), it is shown that M plays a role in amplifying I_f during PTP faults. Additionally, the magnitude of the influence of M on the fault current varies with the fault positions along the line: at the beginning of the line, M provides only a slight increase to the fault current; whereas at the end of the line, its influence on amplifying the fault current is more pronounced. As shown in Fig. 13(b), M has little influence on V_k, so the fault current limiting contribution of SP-PFC is hardly affected by the line coupling inductance according to the analysis.

IV. SAAS OF SP-PFC

According to the above analysis, the fault current limiting contribution of SP-PFC is single and does not vary if the emergency control activation time T_w is fixed. Figure 14(a) and (b) shows I_f and V_k under different T_w of SP-PFC, respectively. If T_w is reduced, the fault current limiting contribution will be larger, but the voltage that SP-PFC can withstand will also be larger. Therefore, the fault current limiting contribution of SP-PFC can be regulated by changing T_w in this paper.

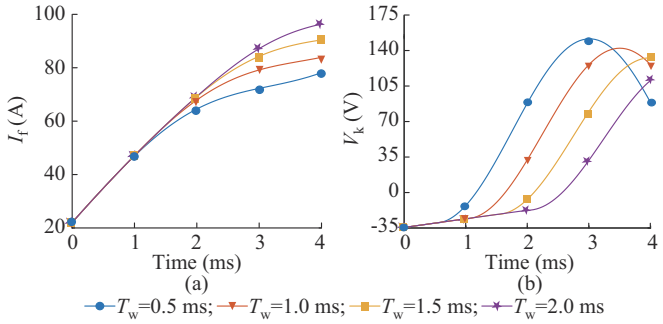

Fig. 14. I_f and V_k under different T_w of SP-PFC. (a) I_f. (b) V_k.

An SAAS of SP-PFC is proposed in this paper to match the different fault severities. The SAAS of SP-PFC operates independently of the command of DC protection system and utilizes the fault detection signal of SP-PFC instead, which enables a faster response. The fault current limiting characteristics under two typical fault severities are shown in Fig. 15, where I_n and I_{max} are the rated current and the maximum DCCB interrupting current, respectively.

Figure 15(a) shows the fault current under serious faults with different strategies. The fault current is higher than I_{max} if the SP-PFC acts according to the fixed logic, hence the SAAS accelerates the action in this case. Figure 15(b) shows the fault current under minor faults with different strategies. The fault current is lower than I_{max} if the emergency control is not activated, hence the SAAS adjusts SP-PFC to maintain bypassed in this case to reduce its voltage stress. The core goal of SAAS of SP-PFC is to dynamically adjust the emergency control activation time according to the fault severity.

Figure 16 shows the flowchart of coordination of SP-PFC and DCCB. Once a fault is detected, it is evaluated whether the emergency control of SP-PFC should be triggered. The SP-PFC switches to Mode 2 to suppress the fault current, thereby reducing the tripping speed and lessening the interrupting capacity requirements of DCCB. The issuance of the protection command of DC protection system requires further fault discrimination because it has higher selectivity and reliability requirements. Furthermore, once the DCCB is fully tripped, a bypass command is issued to disengage the SP-PFC from the circuit. Given that SP-PFC and DCCB are integrated into a developed building block, a unified set of controllers are employed to issue instructions for both systems, which minimizes potential overlap issues arising from communication delays between the SP-PFC and DCCB.

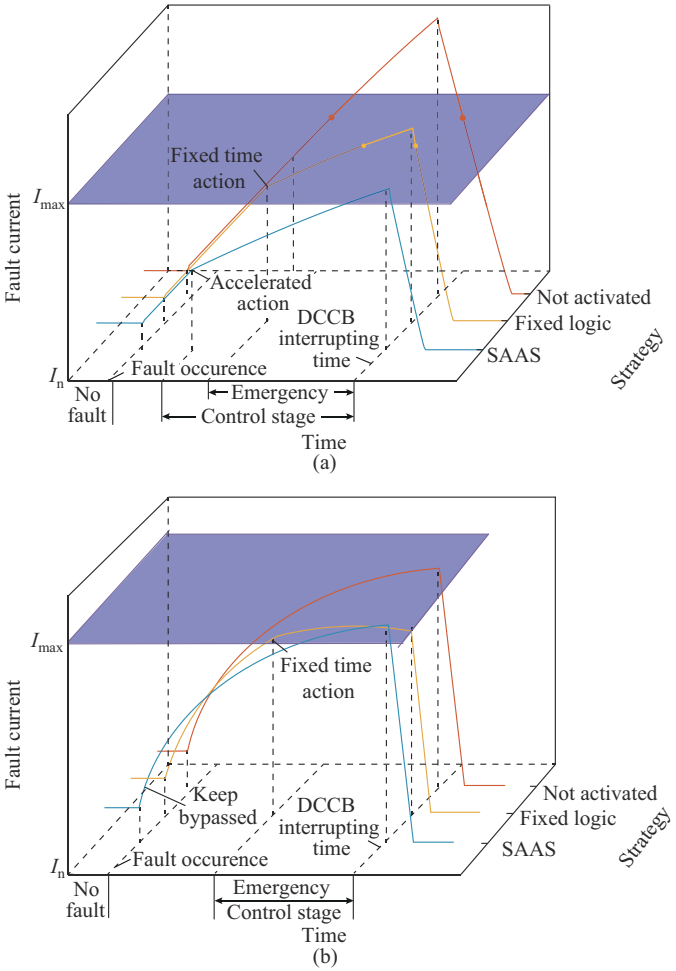

Fig. 15. Fault current limiting characteristics under two typical fault severities. (a) Serious fault. (b) Minor fault.

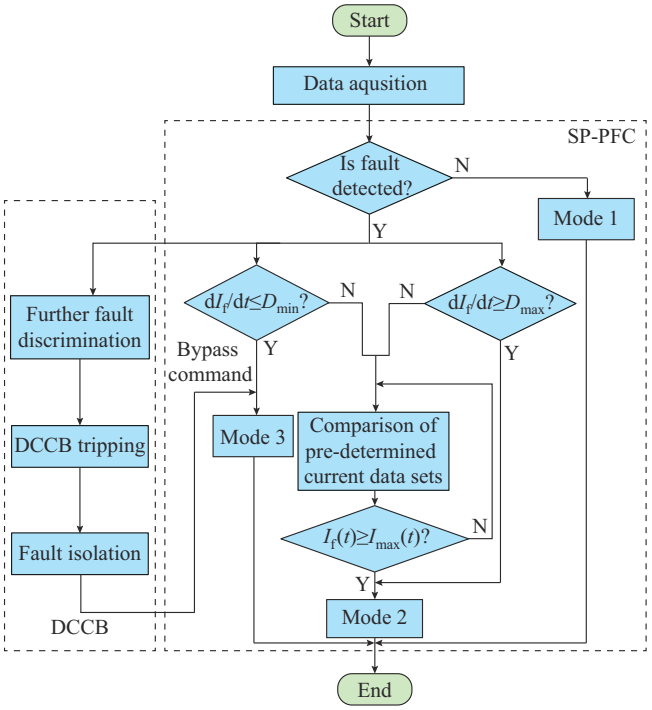

Fig. 16. Flowchart of coordination of SP-PFC and DCCB.

In Fig. 16, D_{max} and D_{min} are the fault current change rate thresholds used to distinguish serious faults and minor faults, respectively; and $I_{max}(t)$ is a pre-determined current time-varying threshold, which is used to determine the emergency control activation time in case of a general fault. D_{max}, D_{min}, and $I_{max}(t)$ are determined based on the CDM equivalent circuits. The change in fault severity is simulated by varying R_f in MATLAB. Firstly, the most serious fault that the DCCB can tolerate with the fixed logic of SP-PFC is recorded, and the initial current change rate in this case is calculated as D_{max}. Secondly, the most minor fault that the DCCB can tolerate with no activated action logic of SP-PFC is recorded, and the average current change rate in this case is calculated as D_{min}. To obtain $I_{max}(t)$, the emergency control is activated at a specific moment δ, while the fault severity is varied until the DCCB interrupting current reaches the desired interrupting value I_g. Therefore, by recording the current data at moment δ as $I_{max}(\delta)$, it is possible to obtain $I_{max}(t)$ for different time instances. The algorithm of SP-PFC for fault current limiting is provided in Supplementary Material A.

V. Simulation and Experiment Results

To verify the validity of the CDM equivalent circuits, parameter optimization method, and SAAS of SP-PFC, a three-terminal DC grid simulation model is established in MATLAB/Simulink and a fault current limiting experiment with SP-PFC is implemented. The structure and parameters of the simulation model are provided in Supplementary Material A. All converter stations are directly grounded, configured in a bipolar arrangement without neutral line. DC reactors are installed at the beginning and end of the lines. The distribution line parameters are as follows: the unit resistance of the distribution line is 0.188 Ω/km, the unit inductance of the distribution line is 0.358 mH/km, and the unit coupling inductance of the distribution line is 0.18 mH/km.

A. Validation of CDM Equivalent Circuits

FP 1, FP 2, and FP 3 are the fault positions at the beginning, middle, and end of Line 12, respectively. The DC fault occurs at 0.6 s, and the fault location is FP 1. DCCB trips at 0.604 s. Firstly, the feasibility of fault current limiting in a three-terminal bipolar DC distribution system based on SP-PFC is verified. Set $R_f = 0$ Ω, $L_{sr} = 3$ mH, and $T_w = 1$ ms. Figure 17 shows the simulation results of the three-terminal bipolar DC distribution system with and without SP-PFC, where V_{bus} is the bus voltage at Node 1.

With the SP-PFC in operation, the maximum value of I_f decreases significantly from 125.3 A to 98.6 A, indicating a significant reduction in fault current. Furthermore, the SP-PFC induces notable changes in the power flow distribution of the DC lines, rendering the power flow fully controllable in the three-terminal bipolar DC distribution system. The voltage drop of V_{bus} is also suppressed by SP-PFC, as shown in Fig. 17(b). It can be concluded that the SP-PFC is effective in suppressing fault currents and optimizing power flow distribution in larger and more complex DC distribution sys-

tems. The inclusion of SP-PFC holds promise for enhancing the stability and reliability in practical applications.

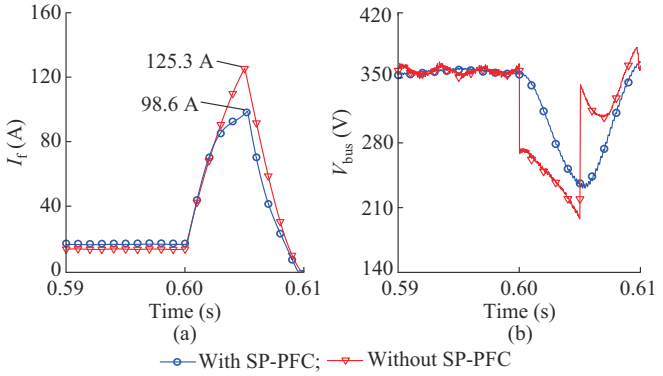

Fig. 17. Simulation results of three-terminal DC distribution system with and without SP-PFC. (a) I_f. (b) V_{bus}.

Then, the correctness of the CDM equivalent circuit is verified. Parameters remain unchanged and the fault location is set at FP 3. The calculation results are obtained by analytical calculation based on the CDM equivalent circuit. Figure 18 shows the calculation and simulation results with the line coupling inductance, as well as simulation results without line coupling inductance. The calculation results with line coupling inductance are very close to the simulation results, which confirms that the CDM equivalent circuit can be used as a reliable fault current limiting characteristic analysis model of SP-PFC considering line coupling inductance.

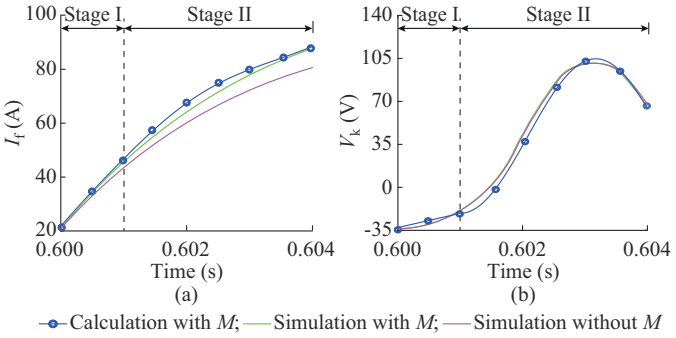

Fig. 18. Calculation and simulation results with and without line coupling inductance M. (a) I_f. (b) V_k.

B. Validation of Parameter Optimization Method

Figure 19(a) shows the simulation results under different R_f, which varies from 0 Ω to 4 Ω. Figure 19(b) shows the simulation results under different L_{sr}, which varies from 2 mH to 4 mH. It is shown that R_f and L_{sr} have a significant influence on I_f but a minor influence on V_k. The simulation results are consistent with Fig. 9.

The fault position is set at FP 1 and parameters are the same as those in Section V-A. Table III shows the fault current limiting contribution S_{PFC} of SP-PFC and the DCCB interrupting current I_{DCCB} under different L_f and C_f. Once L_f is determined, S_{PFC} does not vary monotonically with C_f but has a maximum value. L_f is varied and the corresponding optimal C_f is determined by repeated experiments. L_f and the optimal C_f are recorded, and it is concluded that the fault current limiting capability is relatively optimal when the product of L_f and C_f is about 0.45 mH/mF. This conclusion is consistent with the parameter selection criteria and theoretical analysis outlined in Section III-B.

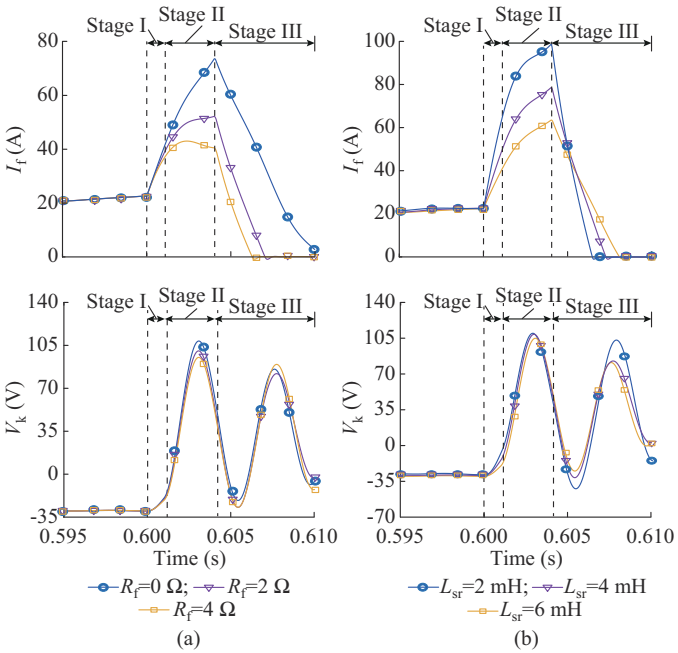

Fig. 19. Simulation results under different R_f and L_{sr}. (a) Under different R_f. (b) Under different L_{sr}.

TABLE III
SIMULATION RESULTS UNDER DIFFERENT C_f AND L_f

L_f (mH)	C_f (mF)	S_{PFC} (V·ms)	I_{DCCB} (A)
0.25	1.6	147.9	119.0
	1.4	145.3	115.3
	1.2	154.7	100.3
	1.0	148.0	110.0
0.50	1.2	155.0	99.5
	1.0	172.2	94.0
	0.8	168.0	100.9
	0.6	145.0	110.0
0.75	1.0	175.5	100.0
	0.8	180.5	90.0
	0.6	190.6	84.0
	0.5	175.0	98.0
1.00	1.0	174.5	100.0
	0.8	190.1	87.0
	0.5	201.5	85.0
	0.3	168.5	94.0
1.25	0.7	198.6	84.0
	0.5	222.6	73.0
	0.4	223.9	72.0
	0.3	205.0	84.0
1.50	0.5	227.3	73.0
	0.4	230.4	69.0
	0.3	238.0	65.0
	0.2	189.6	85.0

After the parameter optimization, L_f is set to be 0.9 mH and C_f is set to be 0.5 mF. Figure 20 shows the simulation results before and after parameter optimization. The fault current limiting contribution of SP-PFC is effectively improved after the parameter optimization, as shown in Fig. 20(b).

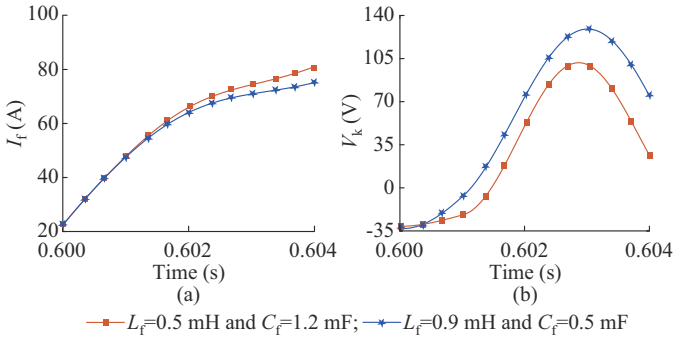

Fig. 20. Simulation results before and after parameter optimization. (a) I_f. (b) V_k.

Figure 21 shows the influence of M on I_f and V_k at different fault positions. It is obvious that M contributes to the development of I_f but has little influence on V_k. The characteristic of the influence of M at different fault positions is consistent with Fig. 13.

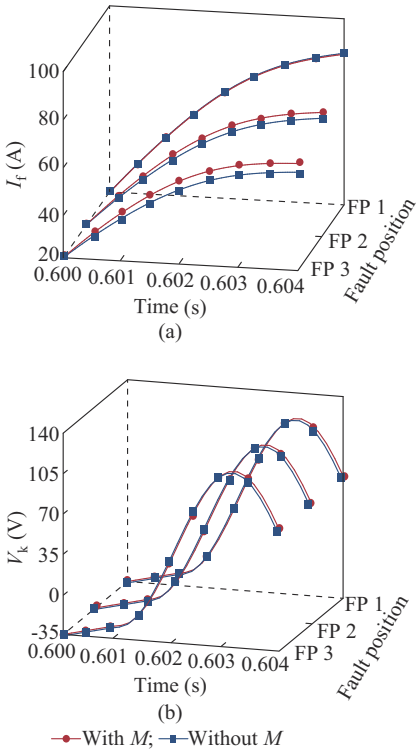

Fig. 21. Influence of M on I_f and V_k at different fault positions. (a) I_f. (b) V_k.

C. Validation of SAAS of SP-PFC

The simulation results under different T_w are shown in Fig. 22. It is apparent that the smaller the T_w, the larger the fault current limiting contribution and the peak value of V_k. The simulation results are consistent with Fig. 14, which provides theoretical support for the study of the SAAS of SP-PFC to match the fault severity.

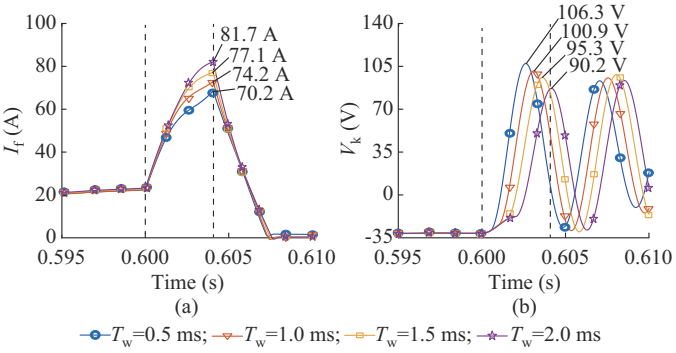

Fig. 22. Simulation results under different T_w. (a) I_f. (b) V_k.

Figure 23 shows simulation results under different faults with different action strategies. In the case of a serious fault (i.e., a short metallic circuit at FP 1), the SAAS regulates SP-PFC to perform greater fault current limiting capability compared to the fixed logic. In the case of a general fault, the SAAS adaptively regulates the DCCB interrupting current to about I_g, which achieves the fault current limiting target while reducing the peak value of output voltage. In the case of a minor fault (i.e., a high-resistance fault at FP 3), the DCCB interrupting current is lower than I_g if the emergency control is not activated. Therefore, the SAAS regulates SP-PFC to keep it bypassed, thereby subjecting the SP-PFC to only small voltage stress. It is indicated that the SAAS adaptively regulates the fault current limiting contribution of SP-PFC according to the fault severity.

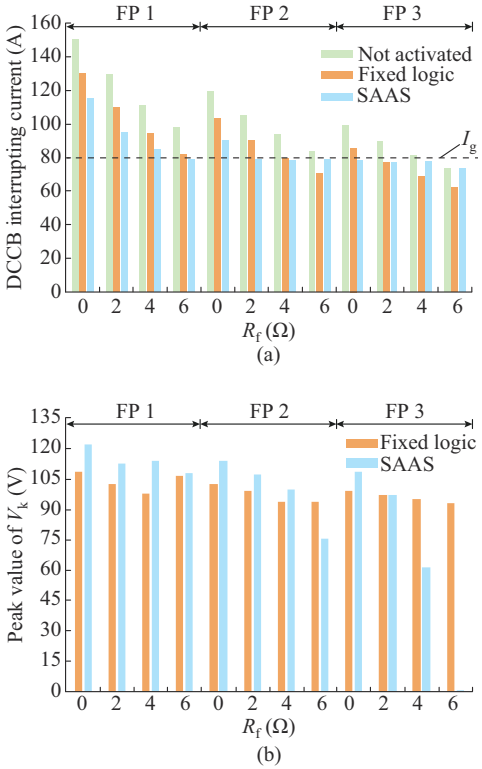

Fig. 23. Simulation results under different faults with different action strategies. (a) DCCB interrupting current. (b) Peak value of V_k.

D. Comparison with Series PFC

It is crucial to clarify that the contemporary research on CFCs and their application for fault current limiting is predominantly focused on high-voltage scenarios. Given the distinct differences in system characteristics between HVDC and LVDC systems, direct comparisons of fault current limiting effects may not be entirely straightforward. To address this, the CFC-based fault current limiting strategies in [19] and [20] are applied to LVDC distribution systems, and the structure of simulation model is provided in Supplementary Material A. While there are differences in the specific topology structures, the fault current limiting characteristics and fundamental principles remain the same. The series CFC inserts its capacitors to the faulty line to absorb fault energy and suppress the fault current [20]. The fault position is set at FP 1, and the fault transition resistance is set to be 0 Ω. Other simulation parameters are consistent with those in Section V-A. The fault current limiting control of CFC is activated 1 ms after the fault occurs.

Figure 24 shows the simulation results of the three-terminal bipolar DC distribution system with and without CFC within 4 ms after the fault occurs, where I_{cfc} is the current of Line 12; V_{CFC} is the output voltage of CFC; and time 0 represents the time of fault occurrence. Compared with the fault current at 4 ms after the fault occurs, as shown in Fig. 17 (a), the fault current is only suppressed to 104.2 A with the CFC. This indicates that the fault current limiting capability of the CFC is less effective compared to that of the SP-PFC.

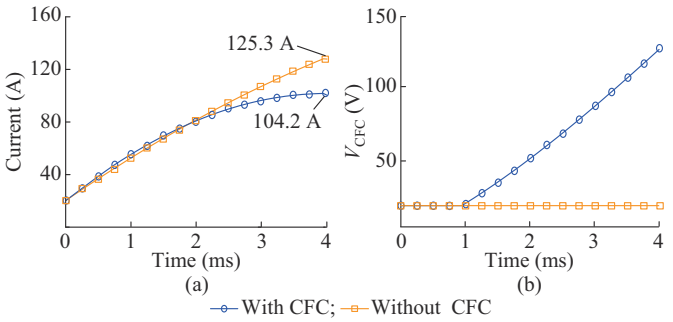

Fig. 24. Simulation results of three-terminal DC bipolar distribution system with and without CFC. (a) I_f. (b) V_{CFC}.

The fault current limiting capability of both SP-PFC and CFC depend on their output voltage characteristics. After the activation of current limiting control, CFC behaves as a capacitor, while SP-PFC is equivalent to a voltage source connected in series with an inductor and then connected in parallel with the capacitor. Figure 25 shows the schematic diagram of the output voltage characteristics of SP-PFC and CFC during short-circuit faults, where U_0 and U_{max} are the initial voltage and upper limit for the output voltage of PFC, respectively; and S_1 and S_2 are the integral values of the output voltage of SP-PFC and CFC during short-circuit faults, respectively. It can be observed from Fig. 25 that S_1 is larger than S_2 when U_0 and U_{max} of SP-PFC and CFC are the same. Meanwhile, the output voltage stress integral of the fault current limiting device corresponds to the amplitude suppression ability of the fault current [9]. Therefore, the SP-PFC exhibits superior current limiting capability compared to CFC at the same withstand voltage limit.

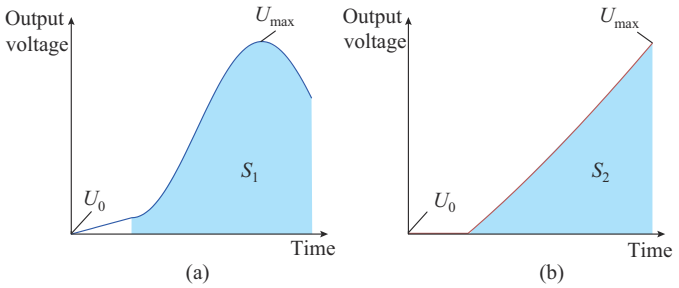

Fig. 25. Schematic diagram of output voltage characteristics during short-circuit fault of SP-PFC and CFC. (a) SP-PFC. (b) CFC.

E. Experiment Verification

The experimental platform of the bipolar DC distribution system with SP-PFC is built, as shown in Fig. 26. The parameters of experimental platform are provided in Supplementary Material A. The STM32H750 control is adopted in SP-PFC. The STM32 header board utilized is based on the STM32F407VGT6 microcontroller. The analog-to-digital converter (ADC) peripheral is set with a sampling rate of 240000 samples per second, which is critical for capturing high-resolution data from our sensors in a short time frame. The pulse width modulation (PWM) modules are configured with a switching frequency of 10 kHz. This subsection meticulously aligns the hardware setup with the corresponding software processes to ensure a cohesive experimental execution. Local loads are mainly constant impedance loads in the ring-shaped bipolar DC distribution system. The local load is a constant resistive load and the positive and negative load equivalent resistances are set to be 20 Ω. The fault transition resistance is set to be 0.5 Ω.

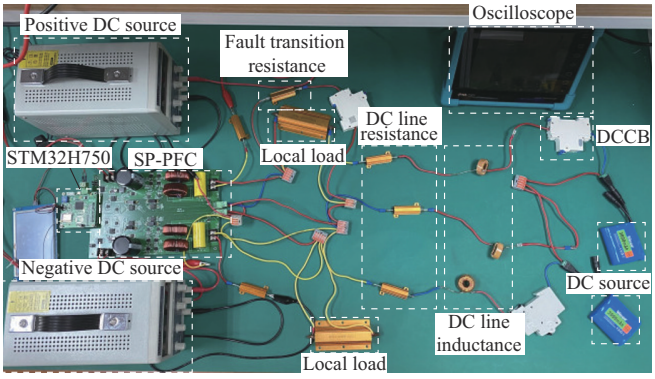

Fig. 26. Experimental platform of DC distribution system with SP-PFC.

The fault current I_f of SP-PFC with and without emergency control is shown in Fig. 27. It can be found that the emergency control can effectively reduce the DCCB interrupting current.

Experimental results under different fault transition resistances are shown in Fig. 28. It can be found that changing the fault transition resistance has a large influence on the fault current but has little influence on the SP-PFC output voltage.

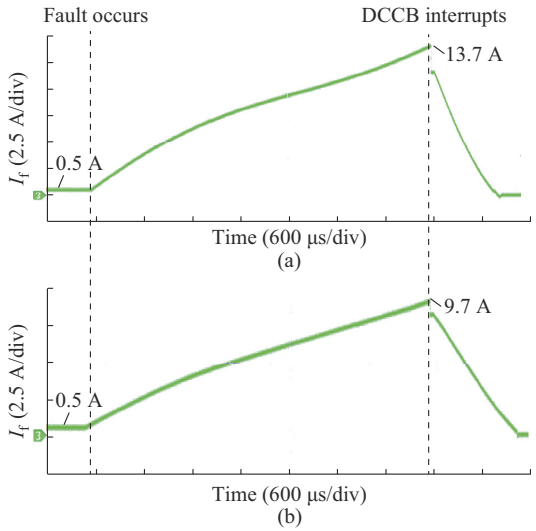

Fig. 27. Fault current I_f of SP-PFC with and without emergency control. (a) With emergency control. (b) Without emergency control.

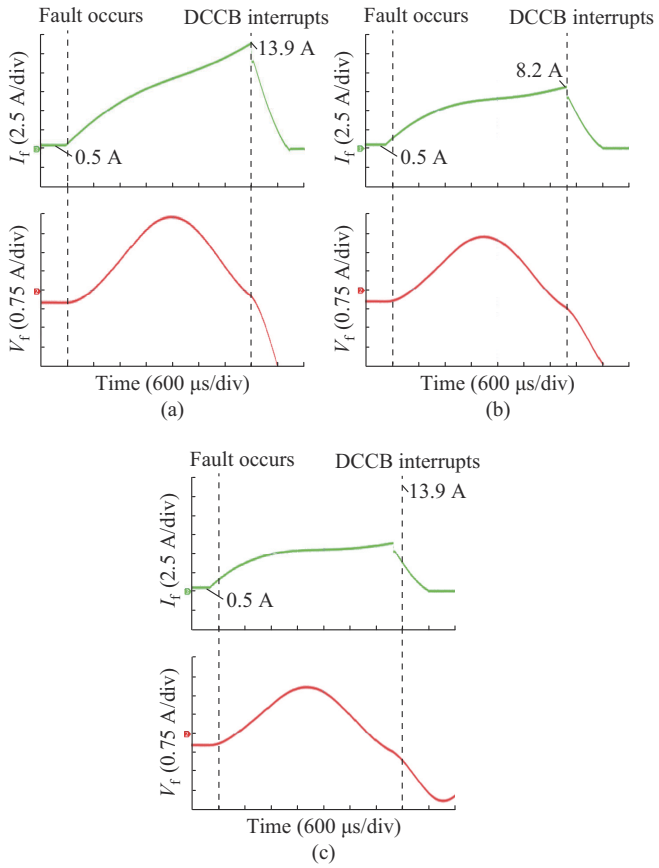

Fig. 28. Experimental results under different fault transition resistances. (a) 0.1 Ω. (b) 1 Ω. (c) 2 Ω.

The filter capacitance and inductance parameters of the SP-PFC are optimized by using the parameter optimization method. The optimized parameters are as follows: $L_f = 1$ mH and $C_f = 8$ μF. The experimental results before and after parameter optimization are shown in Fig. 29. It is observed that the parameter optimization significantly enhances the fault current limiting capability of the SP-PFC.

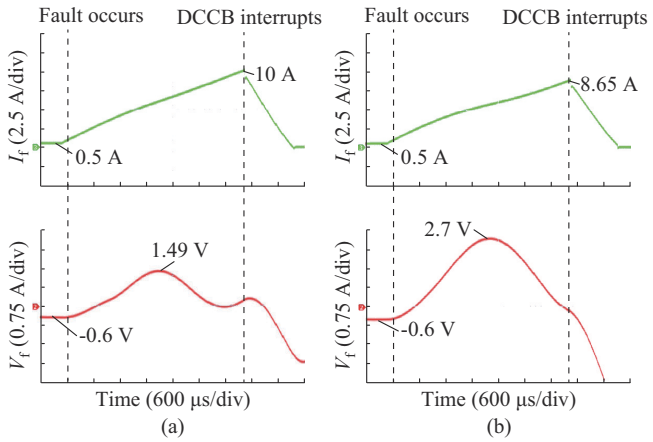

Fig. 29. Experimental results before and after parameter optimization. (a) Before parameter optimization. (b) After parameter optimization.

To verify the feasibility of SAAS of SP-PFC, the emergency control activation time of SP-PFC is varied, and the experimental results under different activation time of emergency control of SP-PFC are shown in Fig. 30. It can be observed that the shorter the activation time, the better the fault current limiting capability. Therefore, the SAAS of SP-PFC is proven to be a viable solution for adaptive fault current limiting in bipolar DC distribution systems.

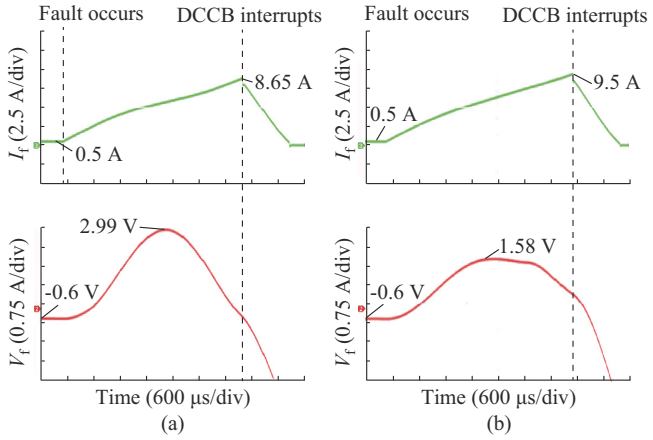

Fig. 30. Experimental results under different activation time of emergency control of SP-PFC. (a) 0.5 ms. (b) 2 ms.

VI. Conclusion

This paper proposes an SAAS and a parameter optimization method of SP-PFC to achieve the fault current limiting target more effectively in bipolar DC distribution systems. To clearly analyze the fault current limiting characteristics of SP-PFC, the CDM equivalent circuits considering line coupling inductance are derived for bipolar DC distribution systems with SP-PFC in different fault stages. An analysis is conducted on the influence of different parameters on the fault current limiting contribution of SP-PFC. The analysis reveals that the fault current limiting contribution of SP-PFC is little affected by fault transition resistance, line inductance, and line coupling inductance. The greatest fault current limiting contribution is observed when the filter capacitance and inductance are inversely proportional. The SAAS

of SP-PFC is proposed to match different fault severities. Theoretical analysis and simulation results show that the CDM equivalent circuit can achieve accurate decoupling calculations for fault currents, and the parameter optimization method enhances the fault current limiting contribution of SP-PFC by approximately 15%. The SAAS of SP-PFC adaptively activates emergency control according to the fault severity, which achieves the fault current limiting target as much as possible while minimizing its fault current limiting pressure to extend its lifespan.

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