Subsequent Commutation Failure Suppression Considering Negative-sequence Voltage Caused by Symmetrical Fault at AC Side of Inverter

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***Abstract*—The negative-sequence voltage is often caused by the asymmetrical fault in the AC system, as well as the harmonics after the symmetrical fault at the AC side of inverter in line commutated converter based high-voltage DC (LCC-HVDC). The negative-sequence voltage affects the phase-locked loop (PLL) and the inverter control, thus the inverter is vulnerable to the subsequent commutation failure (SCF). In this paper, the analytical expression of the negative-sequence voltage resulting from the symmetrical fault with the commutation voltage is derived using the switching function and Fourier decomposition. The analytical expressions of the outputs of the PLL and inverter control with respect to time are derived to quantify the contribution of the negative-sequence voltage to the SCF. To deal with the AC component of the input signals in the PLL and the inverter control due to the negative-sequence voltage, the existing proportional-integral controls of the PLL, constant current control, and constant extinction angle control are replaced by the linear active disturbance rejection control against the SCF. Simulation results verify the contributing factors to the SCF. The proposed control reduces the risk of SCF and improves the recovery speed of the system under different fault conditions.**

***Index Terms*—Line commutated converter, high-voltage direct current, subsequent commutation failure, negative-sequence voltage, inverter control, phase-locked loop (PLL), linear active disturbance rejection control (LADRC).**

I. Introduction

THE line commuted converter based high-voltage DC (LCC-HVDC) system is widely used for long-distance and bulk power transmission, since it has the merits of the high capacity, low loss, and fast and flexible power control [1], [2]. The LCC-HVDC applies thyristor valves without the self-turn-off ability, thus the AC fault at the inverter side may cause the commutation failure (CF) [3]. Specifically, the subsequent CF (SCF) after the first CF leads to the large fluctuations of the voltage and current, which is detrimental to the safe and stable operation of the power system [4], [5].

According to the statistical data [6], about 1400 CFs occurred in the LCC-HVDC owned by State Grid Corporation of China in the past 14 years, averagely 9 CFs per LCC-HVDC per year, and at most more than 20 CFs in the LCC-HVDC connecting the weak grid. In July 2020, a single-phase-to-ground (SPG) fault tripped a 500 kV line near Guquan station, resulting in the SCF of Changji-Guquan ultra-high voltage direct current (UHVDC) system, with power loss of 3000 MW.

To date, several methods are proposed to suppress the SCF: ① modifying the topology of the inverter, which is limited by the technical difficulty and construction cost [7]; ② applying the var compensator, which increases the investment cost [8]; and ③ improving the control strategy, which has the notable advantages in both economy and realizability [9] such as improved voltage-dependent current order limiter (VDCOL), constant extinction angle (CEA) control, and CF prevention (CFPREV) control.

The SCF is affected by the coupling of the DC current, the AC voltage at the inverter side, the control behaviors, the error of the synchronous phase, etc, which is to be considered in the suppression strategy design. To mitigate the impact of electrical quantity coupling on the SCF, [10] defines the fault security region in an inverter station under the effects of multi-electrical quantities, and [11] derives the mathematical models considering different durations and severities of the fault and the system strength to find the DC current reference against the SCF. In [12], a compensation control strategy to the extinction angle is proposed to improve the dynamic performance of CEA control against the SCF. The excessive advancing of the firing angle in the traditional CFPREV leads to more SCFs [13], and the rate limiter is added to the CFPREV to adjust the firing angle. The improper switching of the controllers is studied in [14] and [15], and a dynamic extinction angle control to improve the sensitivity and rapidity of the control system against the SCF is proposed. In [16], the phase shift of the commutation voltage affects the synchronization of the phase-locked loop (PLL) under asymmetrical faults, hence an improved synchronous firing control with the order switching and the phase compensation is proposed to suppress the SCF. In [17], the error between the phase of the AC voltage and PLL is added to the extinction angle against the SCF. Besides,

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the harmonic interaction at the AC and DC sides after the fault causes the SCF, and an improved firing angle control including the harmonics is proposed against the SCF [18].

Although above research works study the mechanisms and the control methods of SCF from different aspects, the impact of negative-sequence voltage on the SCF and its suppression strategy are seldom studied. After the AC fault, the negative-sequence voltage is caused by not only the asymmetrical fault in the AC system, but also the harmonics under the symmetrical fault [19], [20]. If the negative-sequence voltage is regarded as the system disturbance, which is observed and compensated by improving the control strategies of the PLL and control system, the SCF may be avoided. Reference [21] presents a positive reference for designing an active disturbance rejection control against the SCF, but the control law is difficult to adapt to the fault severities.

This paper studies the SCF suppression due to the negative-sequence voltage under the symmetrical fault at the AC side of the inverter. The novelties are: ① considering the harmonics of positive-sequence voltage, the analytical expression of the negative-sequence voltage with respect to commutation voltage is derived by the switching function and Fourier decomposition; ② the dynamic outputs of the PLL and inverter controls with the proportional-integral (PI) control are analytically derived to find the contribution of the negative-sequence voltage to the SCF; ③ an improved linear active disturbance rejection control (LADRC) to replace the PI control in the PLL, constant current control (CCC) at the rectifier side, and CEA at the inverter side are proposed to suppress the SCF. The imbalance degree of the negative-sequence voltage with the commutation voltage is defined to adjust the parameters of the LADRC with the fault severity.

The rest of this paper is organized as follows. In Section II, the analytical expression to cause negative-sequence voltage under symmetrical fault is newly derived. In Section III, contributions of negative-sequence voltage to SCF under the AC fault are found. Section IV presents the suppression strategy to SCF with improved PLL and control system based on LARDC. In Section V, the proposed control is verified by the simulations. Some conclusions are given in Section VI.

II. Analytical Expression to Cause Negative-sequence Voltage Under Symmetrical Fault

A. Control of LCC-HVDC System

Figure 1 shows the structure and the control of the monopole of the LCC-HVDC system based on the CIGRE HVDC model [22], where U_{dc} is the DC voltage; I_{dc} is the DC current; u_a, u_b, and u_c are the three-phase voltages; α is the firing angle; γ is the extinction angle; θ_{PLL} is the output phase of the PLL; $\Delta\gamma$ is the variation of γ compensated by the CEC; ΔI_{dc} is the current variation input to the CCC; G and T are the gain and time constant of the inertial link, respectively; and the subscripts r, i, ref, mes, and act denote the rectifier, the inverter, the reference value, the measured value, and the actual value, respectively.

In the PLL and at rectifier and inverter sides, the traditional control strategies are the PI control. At the AC side, the PLL is applied to track the phase of the AC voltage α_{act} and yield the firing signal of the valves with the equidistant pulse control [23]. At the DC side, the CCC with the constant α_{min} control is applied at the rectifier side, where the subscript min denotes the minimum value. The CEA is applied at the inverter side to yield α_{ref}. The CCC and the VDCOL are applied to yield $I_{dc,ref}$. The current error control (CEC) is used to realize the smooth switching between the CCC and CEA.

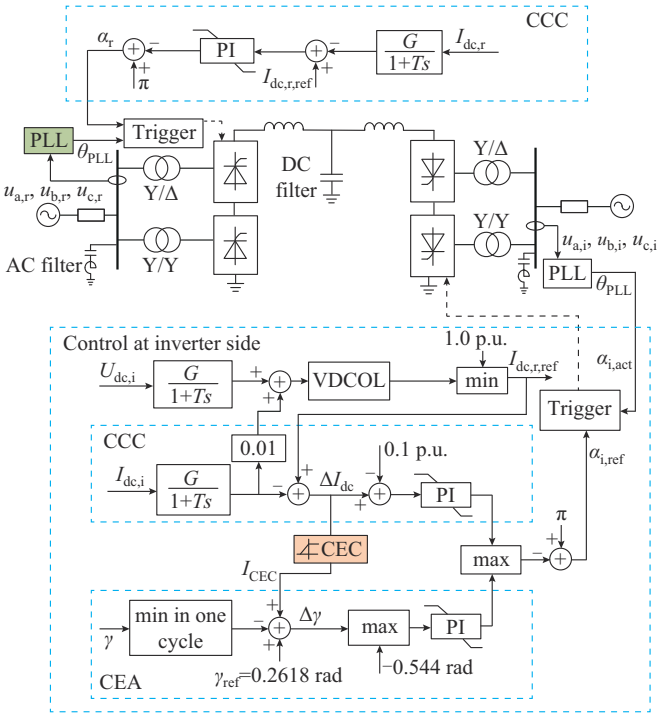

Fig. 1. Structure and control of monopole pole of LCC-HVDC system.

It should be noted that the control structure of the existing LCC-HVDC often adopts the control strategy of CIGRE, SIEMENS, or ABB. All of them have the VDCOL control. The difference lies in the cooperation of the controllers at the inverter side and the mode of CEA (measured or predicted).

B. Deriving Analytical Expression of Negative-sequence Voltage with Commutation Voltage Under Symmetrical Fault

The equivalent circuit of the AC/DC system at the inverter side is shown in Fig. 2, where Z_{dc} is the equivalent impedance of the DC system including the DC line, smoothing reactor, DC filter, and Thevenin equivalent impedance of the AC system at the rectifier side; Z_{ac} is the equivalent impedance from inverter side to AC system; and U_{ac} is the commutation voltage of AC system.

Since the zero-sequence voltage is isolated by the Y/△ and Y/Y transformers, it is not considered in this paper [24]. Due to the discrete switching characteristics of inverter, the switching function method is applied to quantify its input-output relationship [25]. With the switching functions, S_a, S_b, and S_c, U_{dc} is modulated by the AC voltage, and the AC current is modulated by I_{dc}:

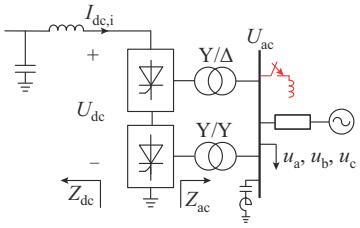

Fig. 2. Equivalent circuit of AC/DC system at inverter side.

$$\begin{cases} U_{dc} = u_a S_{ua} + u_b S_{ub} + u_c S_{uc} \\ i_a = I_{dc} S_{ia} \\ i_b = I_{dc} S_{ib} \\ i_c = I_{dc} S_{ic} \end{cases} \tag{1}$$

where subscripts u and i denote the AC voltage and AC current, respectively; and i_a, i_b, and i_c are the three-phase currents.

The AC voltage including its harmonic is the dominant factor to derive the relation of U_{dc} modulated by the inverter with U_{ac}. After symmetrical fault, it is assumed that the AC harmonic voltage of a specific order at the inverter bus is given by:

$$\begin{cases} u_a = U_{ac,n} \cos\left(\omega_n t + \varphi_n\right) \\ u_b = U_{ac,n} \cos\left(\omega_n t + \varphi_n - \dfrac{2\pi}{3}\right) \\ u_c = U_{ac,n} \cos\left(\omega_n t + \varphi_n + \dfrac{2\pi}{3}\right) \end{cases} \tag{2}$$

where φ is the phase angle; ω is the angular speed; and the subscript n denotes the order of the AC component.

The switching function of the DC voltage in (1) is expanded by (A1) in Appendix A with the Fourier decomposition, and the three-phase voltages in (2) are re-expressed by (A2) with the symmetrical component method. By substituting (A2) into (A1), the DC voltage modulated is derived in (3) with the 1st term of the Fourier decomposition. After the Fourier decomposition, only the coefficients of the terms of 1, 2,…, $6k \pm 1$ $(k = 1, 2, 3, \ldots)$ are not zero, indicating that the calculation result has the AC components of $1, 5, 7, 11, 13, \ldots$ orders. The sum of the high-order components is small, which has little impact on the calculation accuracy, hence these components are eliminated.

$$U_{dc}^{+} = U_{ac,n}^{+} \frac{3\sqrt{3}}{\pi} \cos\frac{\mu}{2} \cos\left(\left(\omega_n - \omega_1\right)t + \varphi_n\right) \tag{3}$$

where μ is the overlap angle; and the superscript + denotes the positive-sequence component.

From (3), the positive-sequence commutation voltage with the harmonic is modulated by the inverter to yield the dominant harmonic voltage with the frequency of $\omega_n - \omega_1$ at the DC side. The harmonic voltage yields the harmonic current of the same frequency with the analytical expression of (4).

$$I_{dc,f1} = \frac{3\sqrt{3}\, U_{ac,n} \cos\left(\omega_{f1} t + \varphi_n - \angle Z_{dc,f1}\right) \cos\dfrac{\mu}{2}}{\pi \left| Z_{dc,f1} \right|} \tag{4}$$

where the subscript fl denotes the 1st term of the Fourier decomposition.

The switching function of the AC current in (1) is expanded by (A3) with the Fourier decomposition. By substituting (4) into (A3), i_a, i_b, and i_c are derived in (5) with the 1st term of the Fourier decomposition, where $\omega_n - 2\omega_1$ is denoted by ω_{f2} and the coefficient A is given in (6).

$$\begin{cases} i_a = A U_{ac,n} \cos\left(\left(\omega_n t + \varphi_n - \angle Z_{dc,f1}\right) + \left(\omega_{f2} t + \varphi_n - \angle Z_{dc,f1}\right)\right) \\ i_b = A U_{ac,n} \cos\left(\left(\omega_n t + \varphi_n - \angle Z_{dc,f1} - \dfrac{2\pi}{3}\right) + \left(\omega_{f2} t + \varphi_n - \angle Z_{dc,f1} + \dfrac{2\pi}{3}\right)\right) \\ i_c = A U_{ac,n} \cos\left(\left(\omega_n t + \varphi_n - \angle Z_{dc,f1} + \dfrac{2\pi}{3}\right) + \left(\omega_{f2} t + \varphi_n - \angle Z_{dc,f1} - \dfrac{2\pi}{3}\right)\right) \end{cases} \tag{5}$$

$$A = \frac{9\sin\mu}{\pi^2 \mu \left| Z_{dc,f1} \right|} \tag{6}$$

From (5), $I_{dc,f1}$ is modulated by the inverter to yield 2 kinds of harmonic currents at the AC side. For the positive-sequence current with the frequency ω_n, phase a leads phase b by $2\pi/3$, and phase b leads phase c by $2\pi/3$. The negative-sequence current with the frequency ω_{f2} has the opposite phase sequence. By multiplying the negative-sequence current and impedance, the negative-sequence voltage is derived in (7).

$$\begin{cases} u_{a,\omega_{f2}}^{-} = U_{ac,\omega_{f2}} \cos\left(\omega_{f2} t + \varphi_n - \angle Z_{dc,f1} + \angle Z_{ac,\omega_{f2}}\right) \\ u_{b,\omega_{f2}}^{-} = U_{ac,\omega_{f2}} \cos\left(\omega_{f2} t + \varphi_n - \angle Z_{dc,f1} + \angle Z_{ac,f2} + \dfrac{2\pi}{3}\right) \\ u_{c,\omega_{f2}}^{-} = U_{ac,\omega_{f2}} \cos\left(\omega_{f2} t + \varphi_n - \angle Z_{dc,f1} + \angle Z_{ac,f2} - \dfrac{2\pi}{3}\right) \end{cases} \tag{7}$$

where $U_{ac,\omega_{f2}} = A U_{ac,n} \left| Z_{ac,f2} \right|$; and the superscript – denotes the negative-sequence component.

Due to the nonlinear modulation of the inverter even under the symmetrical fault, the commutation bus has the negative-sequence voltage, as shown in Fig. 3.

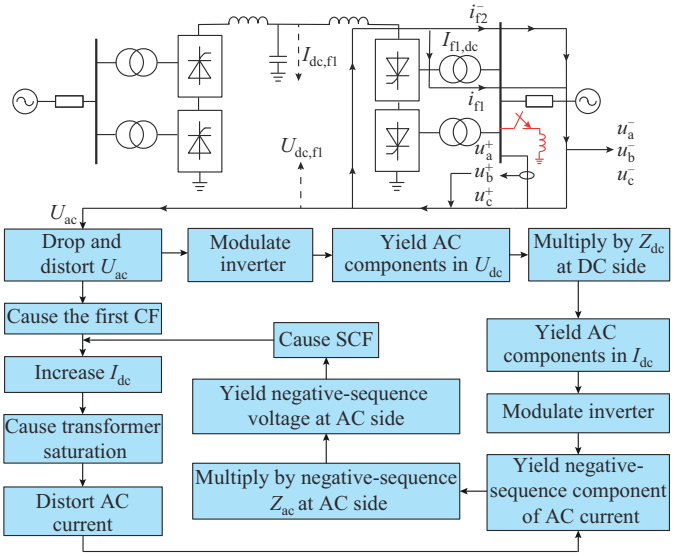

Fig. 3. Cause of negative-sequence voltage under symmetrical fault.

The harmonics cause the distortion of the AC voltage. This distortion is modulated by the inverter, yielding negative-sequence voltage, and causing the first CF. Then, I_{dc} increases due to the first CF, causing the transformer saturation to yield the harmonic currents. The harmonic currents interact with the harmonic impedances at the AC side and yield the harmonic voltages, contributing to the negative-sequence components. Thus, the harmonics and the subsequent negative-sequence components cause the SCF together.

III. Contributions of Negative-sequence Voltage to SCF Under AC Fault

At the AC side, the negative-sequence voltage causes the phase shift of the AC voltage, affecting the dynamic response of the PLL. At the DC side, it is converted to the AC component of I_{dc}, affecting the switching of the inverter controllers.

A. Impact of Negative-sequence Voltage at AC Side

To prevent the CF caused by the harmonic instability, the equidistant pulse control is often used to yield the firing signal of the 12-pluse LCC based on the output phase of synchronous reference frame (SRF)-PLL [23], as shown in Fig. 4, where $\theta_{PLL,ref}$ is the reference phase of the fundamental frequency positive-sequence voltage; α_{act} is the actual value of firing angle; and α_{ref} is the reference value of firing angle.

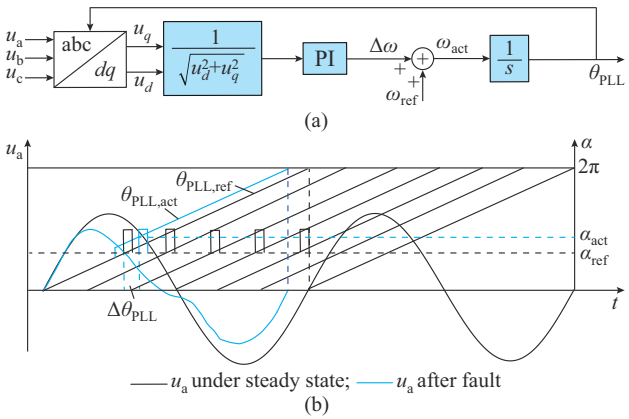

Fig. 4. Impact of negative-sequence voltage on PLL. (a) Traditional SRF-PLL. (b) Impact of phase advance on firing phase.

The inputs of SRF-PLL, i.e., u_a, u_b, and u_c, are converted to the dq domain that ensures the tracking of the voltage phase by the unit vectors. The q-axis voltage, i.e., u_q, is regulated to 0 using the feedback control with the PI control. The normalized u_q is amplified by the PI control to get the frequency deviation $\Delta\omega$. $\Delta\omega$ is added to the fundamental frequency ω_{ref} to get the actual frequency ω_{act}. ω_{act} is applied to the integral link to yield the actual synchronous phase $\theta_{PLL,act}$. Then, $\theta_{PLL,act}$ is fed back to the dq domain that forces u_q to 0. When $\theta_{PLL,act}$ is equal to $\theta_{PLL,ref}$, the firing signal of the valve is yielded.

In the steady state, since $\theta_{PLL,ref}$ obtained by the SRF-PLL is consistent with the phase of AC voltage at the inverter side, α_{act} is matched with α_{ref}. During the transient process, when the phase of AC voltage at the inverter side is changed, the PLL can not track the actual phase in very short time due to its slow response, causing the deviation between α_{act} and α_{ref}.

Considering the negative-sequence components of u_a, u_b, and u_c during the transient, (2) is rewritten by (8). Then, the dq transformation is applied to (8), then (9) is obtained.

$$\begin{cases} u_a = U_{ac}^+ \cos\left(\omega_n t+\varphi_n^+\right) + U_{ac}^- \cos\left(\omega_n t+\varphi_n^-\right) \\ u_b = U_{ac}^+ \cos\left(\omega_n t+\varphi_n^+-\dfrac{2\pi}{3}\right) + U_{ac}^- \cos\left(\omega_n t+\varphi_n^-+\dfrac{2\pi}{3}\right) \\ u_c = U_{ac}^+ \cos\left(\omega_n t+\varphi_n^++\dfrac{2\pi}{3}\right) + U_{ac}^- \cos\left(\omega_n t+\varphi_n^--\dfrac{2\pi}{3}\right) \end{cases} \tag{8}$$

$$\begin{cases} u_d = U_{ac}^+ \cos\left[\left(\omega_n-\omega\right)t+\varphi_n^+\right] + U_{ac}^- \cos\left[\left(\omega_n+\omega\right)t+\varphi_n^-\right] \\ u_q = U_{ac}^+ \sin\left[\left(\omega_n-\omega\right)t+\varphi_n^+\right] - U_{ac}^- \sin\left[\left(\omega_n+\omega\right)t+\varphi_n^-\right] \end{cases} \tag{9}$$

u_a, u_b, and u_c including the negative-sequence voltage are converted by the dq transformation, and only the positive-sequence voltage of the fundamental frequency becomes the DC component. The n^{th}-order AC component of the positive-sequence voltage becomes the $(n-1)^{th}$-order AC component, and the n^{th}-order AC component of the negative-sequence voltage becomes the $(n+1)^{th}$-order AC component, which causes the fluctuation of $\theta_{PLL,act}$. Since the PI control cannot cope with the adverse effect of the negative-sequence voltage on u_q and has a slow dynamic response, the output of the PLL can not be updated in time, hence $\theta_{PLL,ref}$ lags behind $\theta_{PLL,act}$, as shown in Fig. 4(b). However, the control system still uses $\theta_{PLL,ref}$ to trigger the subsequent valve, thus risking SCFs.

B. Impact of Negative-sequence Voltage at DC Side

When a fault occurs at the inverter side, the control system responds quickly to restore the post-fault I_{dc} to a new stable point. As shown in Fig. 5, the dynamic process is divided into five stages with the switching of the controllers, i.e., the first CF, recovery climbing, recovery consolidation, SCF, and new steady-state stages.

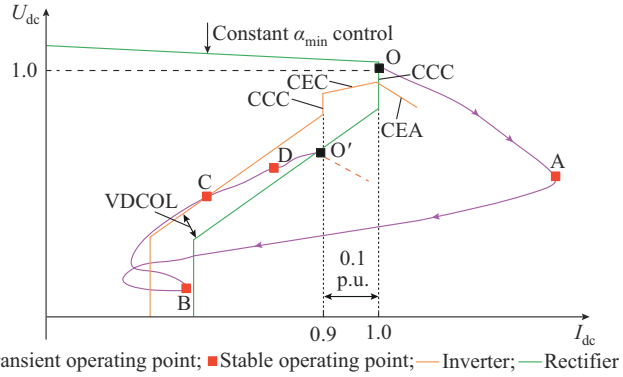

Fig. 5. Post-fault dynamic characteristics of LCC-HVDC.

1) Stage 1: in the steady state, the system is at point O. The rectifier side is controlled by the CCC, and the inverter side is controlled by the CEA. After the fault, the system enters stage 1. The drop of DC current U_{dc} increases I_{dc} due to the short circuit of valve group, causing the first CF, so the system moves to point A (the maximum I_{dc} operating point). Then, $I_{dc,act}$ begins to decrease due to the VDCOL. When

$I_{dc,act}$ is less than $I_{dc,ref}$, the CEC is activated.

2) Stage 2: with the decrease of I_{dc}, the commutation of the inverter recovers, thus the system moves to point B. It is the transient point when the CEA switches to the CCC, which means that the system enters stage 2. U_{dc} increases with the recovery of the commutation. Since α_{CEA} derived from the CEA is less than that in the steady state, the CEA begins to act under the PI control, thus γ decreases gradually. The decrease of γ helps increase U_{dc}. Hence, the recovery of U_{dc} is mainly dependent on that of the commutation process, and the CEA has an auxiliary contribution. Next, the system moves to point D, which is the transient point when the CCC switches to the CEA. I_{dc} is affected by both the rectifier and inverter controls.

3) Stage 3: with the increase of U_{dc}, α_{CCC} derived from the CCC is increased to equal α_{CEA}, thus the CCC is switched to CEA, meaning that the system enters stage 3. I_{dc} is controlled by the rectifier control.

Containing the negative-sequence voltage and its harmonics, ΔI_{dc}, is derived by (10).

$$\Delta I_{dc} = \Delta I_{dc,0} + \sum_{n=2}^{\infty} \Delta I_{dc,n} \cos\left(n\omega t + \varphi_{dc,n}\right) \tag{10}$$

where the subscript 0 denotes the DC component.

By multiplying the transfer function of the PI control by the Laplace transform of (10), the output of CCC, i. e., $\alpha_{CCC}(s)$, is derived as:

$$\alpha_{CCC}(s) = \pi - \left(K_{CCC} + \frac{1}{sT_{CCC}}\right)\left[\frac{\Delta I_{dc,0}}{s} + \sum_{n=2}^{\infty} \Delta I_{dc,n} \frac{s\cos\varphi_{dc,n} - n\omega\sin\varphi_{dc,n}}{s^2 + (n\omega)^2}\right] \tag{11}$$

where K and T are the PI parameters.

By solving the inverse Laplace transform of (11), $\alpha_{CCC}(t)$ is analytically expressed in (12). Hence the CCC is affected by the negative-sequence voltage, which leads to the fluctuation of α_{ref} at the rectifier and inverter sides.

$$\alpha_{CCC}(t) = K_{CCC}\Delta I_{dc,0} + \frac{\Delta I_{dc,0}}{T_{CCC}}t + \sum_{n=2}^{\infty} K_{CCC}\Delta I_{dc,n}\cos\left(n\omega t + \varphi_{dc,n}\right) + \sum_{n=2}^{\infty} \frac{\Delta I_{dc,n}}{n\omega T_{CCC}}\sin\left(n\omega t + \varphi_{dc,n}\right) - \sum_{n=2}^{\infty} \frac{\Delta I_{dc,n}\sin\varphi_{dc,n}}{n\omega T_{CCC}} \tag{12}$$

For the CEA, the variation of γ compensated by the CEC, i.e., $\Delta\gamma$, is derived by (13). Similar to (12), $\alpha_{i,CEA}(t)$ is analytically expressed in (14). The output of the CEA has the frequency components with the n^{th} order, causing the fluctuation of α_{ref}.

$$\Delta\gamma = \gamma_{ref} - \gamma_{mes} + K_{CEC}\left(\Delta I_{dc,0} + \sum_{n=2}^{\infty} \Delta I_{dc,n}\cos\left(n\omega t + \varphi_{dc,n}\right)\right) \tag{13}$$

$$\alpha_{CEA}(t) = \pi - K_{CEA}\left(\gamma_{ref} - \gamma_{mes} + m\right) - \frac{\gamma_{ref} - \gamma_{mes} + m}{T_{CEA}}t + \sum_{n=2}^{\infty} \frac{m\sin\varphi_{dc,n}}{n\omega T_{CEA}} - \sum_{n=2}^{\infty} K_{CEA} m\cos\left(n\omega t + \varphi_{dc,n}\right) - \sum_{n=2}^{\infty} \frac{m}{n\omega T_{CEA}}\sin\left(n\omega t + \varphi_{dc,n}\right) \tag{14}$$

where K_{CEA} and T_{CEA} are the PI parameters for CEA control; and $m = K_{CEC}\Delta I_{dc,0}$, and K_{CEC} is the coefficient of CEC.

4) Stage 4: when α_{act} is larger than α_{ref}, the SCF occurs, which means that the system enters stage 4. When the fault is cleared, the system reaches a new steady-state stage (stage 5).

The contribution of the negative-sequence voltage to the SCF is given in Fig. 6. The distorted three-phase voltages after the fault are modulated by the inverter and yield the negative-sequence voltage. The PI control in the control system cannot deal with the adverse effect of the negative-sequence voltage on the AC voltage and the DC current. At the AC side, the phase shift of the PLL due to the negative-sequence voltage yields the deviation of the firing phase. At the DC side, α_{act} including the firing phase deviation is larger than α_{ref}, which causes the CCC to be switched to the CEA, then the SCF occurs.

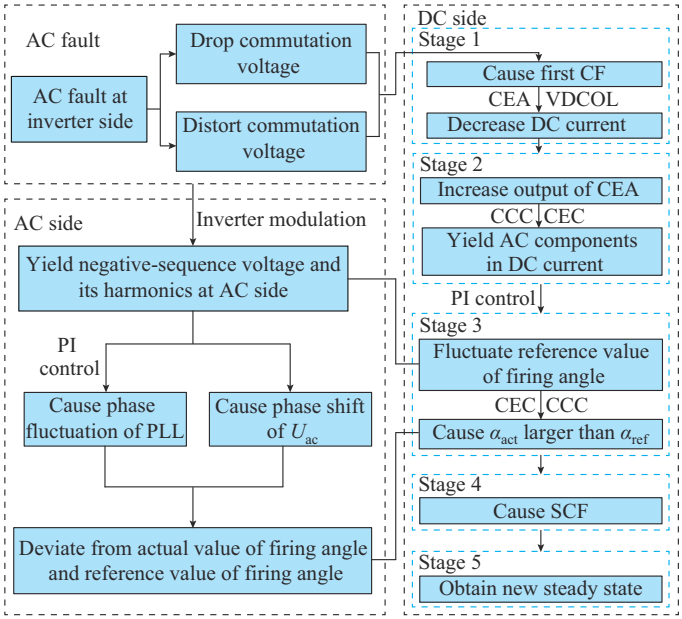

Fig. 6. Contribution of negative-sequence voltage to SCF.

IV. Suppression Strategy to SCF with Improved PLL and Control System Based on LARDC

With the findings in Section III, the PI controls of the PLL and inverter control enhance the contribution of the negative-sequence voltage to the SCF, hence they may be improved to suppress the SCF. As a disturbance, the impact of the negative-sequence voltage on the SCF may be alleviated by observing and compensating it. Besides, the suppression effect on the SCF is affected by many disturbances such as the measurement noise and the system uncertainty. Considering the difficulty of parameter tuning, the LARDC strategy against the SCF is proposed to replace the PI control of the PLL, the CCC at the rectifier side, and the CEA at the inverter side.

A. Improved PLL at AC Side with LADRC

Considering the negative-sequence voltage of commutation bus, (8) is rewritten by (15).

$$\begin{bmatrix} u_d \\ u_q \end{bmatrix} \cong \begin{bmatrix} u_d^+ \\ u_q^+ \end{bmatrix} + \begin{bmatrix} \tilde{u}_d \\ \tilde{u}_q \end{bmatrix} \tag{15}$$

where $\tilde{u}_d$ and $\tilde{u}_q$ are the AC voltage components of the *d*- and *q*-axis except for the fundamental-frequency positive-sequence voltage, respectively. By setting the reference input of the PLL $u_{q,\mathrm{ref}}$ to 0, the standard form of the controlled plant is derived by (16).

$$\frac{\mathrm{d}u_q}{\mathrm{d}t} = \underbrace{\omega_{\mathrm{act}} + \frac{\mathrm{d}\theta_{\mathrm{PLL}}}{\mathrm{d}t} + \frac{\mathrm{d}u_q^-}{\mathrm{d}t} + d}_{d_{\mathrm{tol}}} - \underbrace{\Delta\omega}_{x} = d_{\mathrm{tol}} + x \tag{16}$$

where d_{tol} is the total disturbance considering the negative-sequence voltage and its harmonics, uncertainty, and the measurement noise; and x is the control signal of the system.

According to (16), the improved PLL is the 1st-order system. The state space equation of (16) is derived by (17).

$$\begin{cases} \begin{bmatrix} \dot{u}_q \\ \dot{d}_{\mathrm{tol}} \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} u_q \\ d_{\mathrm{tol}} \end{bmatrix} + \begin{bmatrix} b_{\mathrm{PLL}} & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} x \\ \dot{d}_{\mathrm{tol}} \end{bmatrix} \\ y_{\mathrm{PLL}} = u_q \end{cases} \tag{17}$$

where y_{PLL} is the output signal of the system; and b_{PLL} is the system gain.

With the given state space of (17), the linear extended state observer (LESO) is derived by (18).

$$\begin{bmatrix} \dot{z}_{1,\mathrm{PLL}} \\ \dot{z}_{2,\mathrm{PLL}} \end{bmatrix} = \begin{bmatrix} -h_{1,\mathrm{PLL}} & 1 \\ -h_{2,\mathrm{PLL}} & 0 \end{bmatrix} \begin{bmatrix} z_{1,\mathrm{PLL}} \\ z_{2,\mathrm{PLL}} \end{bmatrix} + \begin{bmatrix} b_{\mathrm{PLL}} & h_{1,\mathrm{PLL}} \\ 0 & h_{2,\mathrm{PLL}} \end{bmatrix} \begin{bmatrix} x_{\mathrm{PLL}} \\ y_{\mathrm{PLL}} \end{bmatrix} \tag{18}$$

where $z_{1,\mathrm{PLL}}$ and $z_{2,\mathrm{PLL}}$ are the estimated values of u_q and d_{tol}, respectively; and $h_{1,\mathrm{PLL}}$ and $h_{2,\mathrm{PLL}}$ are the LESO gains.

By compensating the disturbances observed by the LESO to x, the feedback control law, i.e., the linear state error feedback (LSEF) is designed as:

$$x = -\Delta\omega = \frac{K_{\mathrm{PLL}}\left(u_{q,\mathrm{ref}} - z_{1,\mathrm{PLL}}\right) - z_{2,\mathrm{PLL}}}{b_{\mathrm{PLL}}} \tag{19}$$

where K_{PLL} is the feedback gain.

Therefore, there are three parameters to be tuned, i. e., $h_{1,\mathrm{PLL}}$, $h_{2,\mathrm{PLL}}$, and K_{PLL}. Based on the bandwidth-tuning method [26], we can obtain:

$$\begin{cases} h_{1,\mathrm{PLL}} = 2w_{\mathrm{ESO,PLL}} \\ h_{2,\mathrm{PLL}} = w_{\mathrm{ESO,PLL}}^2 \\ K_{\mathrm{PLL}} = w_{\mathrm{LSEF,PLL}} \end{cases} \tag{20}$$

where $w_{\mathrm{ESO,PLL}}$ is the bandwidth of the LESO; and $w_{\mathrm{LSEF,PLL}}$ is the bandwidth of the LSEF.

b_{PLL} has a direct effect on the PLL and may be changed with the fault severity against the SCF. Hence, the imbalance degree of negative-sequence voltage with respect to the commutation voltage ε is defined in (21) to adjust the output of LADRC. Then, ε is multiplied by the drop degree of voltage, which is added to the pre-fault b_{PLL} to find the post-fault b_{PLL}, as derived in (22).

$$\varepsilon = \left| \frac{U_{\mathrm{ac}} - u_d}{U_{\mathrm{ac}}} \right| \quad 0 \le \varepsilon \le 1 \tag{21}$$

$$b'_{\mathrm{PLL}} = b_{\mathrm{PLL}} + \varepsilon \left| 1 - \frac{U_{\mathrm{ac,min}}}{U_{\mathrm{ac,ref}}} \right| \tag{22}$$

B. Improved Control System at DC Side with LADRC

For the control system, there are two PI controls in the CCC at the rectifier side and the CEA at the inverter side to be replaced with the LADRC. The transient equation of the HVDC [20] is given by (23).

$$\begin{cases} L_{\mathrm{r}} \dfrac{\mathrm{d}I_{\mathrm{dc,r}}}{\mathrm{d}t} = -R_{\mathrm{dl}} I_{\mathrm{dc,r}} + \dfrac{3\sqrt{2}\,U_{\mathrm{ac,r}} \cos\alpha_{\mathrm{r}}}{\pi k_{\mathrm{ct,r}}} - \dfrac{3}{\pi} X_{\mathrm{ct,r}} I_{\mathrm{dc,r}} - U_{\mathrm{c}} \\ L_{\mathrm{i}} \dfrac{\mathrm{d}I_{\mathrm{dc,i}}}{\mathrm{d}t} = -R_{\mathrm{dl}} I_{\mathrm{dc,i}} - \dfrac{3\sqrt{2}\,U_{\mathrm{ac,i}} \cos\alpha_{\mathrm{i}}}{\pi k_{\mathrm{ct,i}}} - \dfrac{3}{\pi} X_{\mathrm{ct,i}} I_{\mathrm{dc,i}} + U_{\mathrm{c}} \\ C_{\mathrm{dc}} \dfrac{\mathrm{d}U_{\mathrm{c}}}{\mathrm{d}t} = I_{\mathrm{dc,r}} - I_{\mathrm{dc,i}} \end{cases} \tag{23}$$

where C_{dc} is the DC capacitance; L is the inductance including the smoothing reactor and the DC line; R is the resistance; k is the tape ratio; X is the reactance; and the subscripts dl and ct denote the DC line and the converter transformer, respectively.

Since the regulation of the converter by the control system is approximated by the 1st-order lag link, the state equation for the control of the rectifier side α_{r} and inverter side α_{i} is derived by (24).

$$\begin{cases} \dot{\alpha}_{\mathrm{r}} = \left(-\alpha_{\mathrm{r}} + \alpha_{\mathrm{r,ref}} + x_{\alpha_{\mathrm{r}}}\right) \big/ T_{\alpha_{\mathrm{r}}} \\ \dot{\alpha}_{\mathrm{i}} = \left(\alpha_{\mathrm{i}} - \alpha_{\mathrm{i,ref}} + x_{\alpha_{\mathrm{i}}}\right) \big/ T_{\alpha_{\mathrm{i}}} \end{cases} \tag{24}$$

For the rectifier side, the CCC is used to keep the current constant, thus we can obtain:

$$y_{\mathrm{r}}(t) = I_{\mathrm{dc,r}}(t) - I_{\mathrm{dc,ref}}(t) = 0 \tag{25}$$

With (23) and (24), the 2nd-order derivative of $I_{\mathrm{dc,r}}$ with respect to t is derived by (26).

$$\ddot{I}_{\mathrm{dc,r}} = \frac{1}{L_{\mathrm{r}}} \left[-\left(R_{\mathrm{dl}} + \frac{3X_{\mathrm{ct,r}}}{\pi} \right) \dot{I}_{\mathrm{dc,r}} - \dot{U}_{\mathrm{c}} + \frac{3\sqrt{2}\,B}{\pi k_{\mathrm{ct,r}}} \left(\dot{U}_{\mathrm{ac,r}} \cos\alpha_{\mathrm{r}} - U_{\mathrm{ac,r}} \dot{\alpha}_{\mathrm{r}} \sin\alpha_{\mathrm{r}} \right) \right] \tag{26}$$

By substituting (24) into (26), the state space of (26) is derived by (27), where $d_{\mathrm{tol,r}}$ is given in (28).

$$\begin{cases} \begin{bmatrix} \dot{I}_{\mathrm{dc,r}} \\ \ddot{I}_{\mathrm{dc,r}} \\ \dot{d}_{\mathrm{tol,r}} \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{\mathrm{dc,r}} - I_{\mathrm{dc,ref}} \\ \dot{I}_{\mathrm{dc,r}} \\ d_{\mathrm{tol}} \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ b_{\mathrm{CCC}} & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} x_{\alpha_{\mathrm{r}}} \\ \dot{d}_{\mathrm{tol,r}} \end{bmatrix} \\ y_{\mathrm{r}} = I_{\mathrm{dc,r}} - I_{\mathrm{dc,ref}} \end{cases} \tag{27}$$

$$\begin{cases} d_{\mathrm{tol,r}} = \dfrac{1}{L_{\mathrm{r}}} \left[-\left(R_{\mathrm{dl}} + \dfrac{3X_{\mathrm{r}}}{\pi} \right) \dot{I}_{\mathrm{dc,r}} - \dot{U}_{\mathrm{c}} + \dfrac{3\sqrt{2}}{\pi k_{\mathrm{r}}} \left(\dot{U}_{\mathrm{ac,r}} \cos\alpha_{\mathrm{r}} - \dfrac{U_{\mathrm{ac,r}} \sin\alpha_{\mathrm{r}} \left(-\alpha_{\mathrm{r}} + \alpha_{\mathrm{r,ref}}\right)}{T_{\alpha_{\mathrm{r}}}} \right) \right] \\ b_{\mathrm{CCC}}(t) = -\dfrac{3\sqrt{2}\,U_{\mathrm{ac,r}} \sin\alpha_{\mathrm{r}}}{\pi T_{\alpha_{\mathrm{r}}} L_{\mathrm{r}} k_{\mathrm{ct,r}}} \end{cases} \tag{28}$$

Similar to (18), the 3rd-order LESO of the improved CCC with the LADRC is derived by (29).

Next, by compensating the disturbances observed by the

LESO to x, the LSEF is derived by (30), and there are five parameters to be tuned, i.e., $h_{1,\mathrm{CCC}}$, $h_{2,\mathrm{CCC}}$, $h_{3,\mathrm{CCC}}$, $K_{1,\mathrm{CCC}}$, and $K_{2,\mathrm{CCC}}$. Similar to the parameter tuning method of the improved PLL, h_1 and h_2 are tuned in (31).

$$\begin{bmatrix}\dot{z}_{1,\mathrm{CCC}}\\ \dot{z}_{2,\mathrm{CCC}}\\ \dot{z}_{3,\mathrm{CCC}}\end{bmatrix}=\begin{bmatrix}-h_{1,\mathrm{CCC}} & 1 & 0\\ -h_{2,\mathrm{CCC}} & 0 & 1\\ -h_{3,\mathrm{CCC}} & 0 & 0\end{bmatrix}\begin{bmatrix}z_{1,\mathrm{CCC}}\\ z_{2,\mathrm{CCC}}\\ z_{3,\mathrm{CCC}}\end{bmatrix}+\begin{bmatrix}0 & h_{1,\mathrm{CCC}}\\ b_{\mathrm{CCC}} & h_{2,\mathrm{CCC}}\\ 0 & h_{3,\mathrm{CCC}}\end{bmatrix}\begin{bmatrix}x_{\alpha_\mathrm{r}}\\ y_\mathrm{r}\end{bmatrix} \tag{29}$$

$$x_{\alpha_\mathrm{r}}=\frac{K_{1,\mathrm{CCC}}\left(I_{\mathrm{dc,r}}-I_{\mathrm{dc,ref}}-z_{1,\mathrm{CCC}}\right)-K_{2,\mathrm{CCC}}z_{2,\mathrm{CCC}}-z_{3,\mathrm{CCC}}}{b_{\mathrm{CCC}}} \tag{30}$$

$$\begin{cases}h_{1,\mathrm{CCC}}=3w_{\mathrm{ESO,CCC}}\\ h_{2,\mathrm{CCC}}=3w_{\mathrm{ESO,CCC}}^2\\ h_{3,\mathrm{CCC}}=w_{\mathrm{ESO,CCC}}^3\\ K_{1,\mathrm{CCC}}=w_{\mathrm{LSEF,CCC}}^2\\ K_{2,\mathrm{CCC}}=2w_{\mathrm{LSEF,CCC}}\end{cases} \tag{31}$$

b_{CCC} after the fault is derived in (32) with the variation of I_{dc}, where the subscript max denotes the maximum value.

$$b'_{\mathrm{CCC}}=b_{\mathrm{CCC}}+\varepsilon\left|\frac{I_{\mathrm{dc,max}}}{I_{\mathrm{dc,ref}}}-1\right| \tag{32}$$

For the inverter side, the CEA is used to keep the extinction angle constant, thus we can obtain (33). With (33), the derivative of γ with respect to t is derived in (34).

$$y_\mathrm{i}(t)=\gamma(t)-\gamma_{\mathrm{ref}}(t)=\arccos\left(-\cos\alpha_\mathrm{i}+\frac{\sqrt{2}\,k_{\mathrm{ct,i}}X_{\mathrm{ct,i}}I_{\mathrm{dc,i}}}{U_{\mathrm{ac,i}}}\right)-\gamma_{\mathrm{ref}} \tag{33}$$

$$\dot{\gamma}=-\frac{\dot{\alpha}_\mathrm{i}\sin\alpha_\mathrm{i}+\sqrt{2}\,k_{\mathrm{ct,i}}X_{\mathrm{ct,i}}\dfrac{U_{\mathrm{ac,i}}\dot{I}_{\mathrm{dc,i}}-\dot{U}_{\mathrm{ac,i}}I_{\mathrm{dc,i}}}{U_{\mathrm{ac,i}}^2}}{\sqrt{1-\left(-\cos\alpha_\mathrm{i}+\dfrac{\sqrt{2}\,k_{\mathrm{ct,i}}X_{\mathrm{ct,i}}I_{\mathrm{dc,i}}}{U_{\mathrm{ac,i}}}\right)^2}} \tag{34}$$

The state space of (34) is derived in (35), where $d_{\mathrm{tol,i}}$ is given in (36). Next, the 2nd-order LESO of the improved CEA is derived by (37).

$$\begin{cases}\begin{bmatrix}\dot{\gamma}\\ \dot{d}_{\mathrm{tol,i}}\end{bmatrix}=\begin{bmatrix}0 & 1\\ 0 & 0\end{bmatrix}\begin{bmatrix}\gamma-\gamma_{\mathrm{ref}}\\ d_{\mathrm{tol,i}}\end{bmatrix}+\begin{bmatrix}b_{\mathrm{CEA}} & 0\\ 0 & 1\end{bmatrix}\begin{bmatrix}x_{\alpha_\mathrm{i}}\\ \dot{d}_{\mathrm{tol,i}}\end{bmatrix}\\ y_\mathrm{i}=\gamma-\gamma_{\mathrm{ref}}\end{cases} \tag{35}$$

where b_{CEA} is the system gain of the improved CEA control based on LADRC.

$$\begin{cases}d_{\mathrm{tol,i}}=-\dfrac{-\dfrac{\sin\alpha_\mathrm{i}\left(\alpha_\mathrm{i}-\alpha_{\mathrm{i,ref}}\right)}{T_{\alpha_\mathrm{i}}}+\dfrac{\sqrt{2}\,k_{\mathrm{ct,i}}X_{\mathrm{ct,i}}\left(U_{\mathrm{ac,i}}\dot{I}_{\mathrm{dc,i}}-I_{\mathrm{dc,i}}\dot{U}_{\mathrm{ac,i}}\right)}{U_{\mathrm{ac,i}}^2}}{\sqrt{1-\left(-\cos\alpha+\dfrac{\sqrt{2}\,k_{\mathrm{ct,i}}X_{\mathrm{ct,i}}I_{\mathrm{dc,i}}}{U_{\mathrm{ac,i}}}\right)^2}}\\ b_{\mathrm{CEA}}(t)=-\dfrac{\sin\alpha_\mathrm{i}}{T_{\alpha_\mathrm{i}}\sqrt{1-\left(-\cos\alpha+\dfrac{\sqrt{2}\,k_{\mathrm{ct,i}}X_{\mathrm{ct,i}}I_{\mathrm{dc,i}}}{U_{\mathrm{ac,i}}}\right)^2}}\end{cases} \tag{36}$$

$$\begin{bmatrix}\dot{z}_{1,\mathrm{CEA}}\\ \dot{z}_{2,\mathrm{CEA}}\end{bmatrix}=\begin{bmatrix}-h_{1,\mathrm{CEA}} & 1\\ -h_{2,\mathrm{CEA}} & 0\end{bmatrix}\begin{bmatrix}z_{1,\mathrm{CEA}}\\ z_{2,\mathrm{CEA}}\end{bmatrix}+\begin{bmatrix}b_{\mathrm{CEA}} & h_{1,\mathrm{CEA}}\\ 0 & h_{2,\mathrm{CEA}}\end{bmatrix}\begin{bmatrix}x_{\alpha_\mathrm{i}}\\ y_\mathrm{i}\end{bmatrix} \tag{37}$$

By compensating for the disturbances observed by the LESO to x, the LSEF is derived by (38). The parameter tuning is similar to (20). b_{CEA} is derived in (39) with the change of γ.

$$x_{\alpha_\mathrm{i}}=\frac{K_{\mathrm{CEA}}\left(\gamma-\gamma_{\mathrm{ref}}-z_{1,\mathrm{CEA}}\right)-z_{2,\mathrm{CEA}}}{b_{\mathrm{CEA}}} \tag{38}$$

$$b'_{\mathrm{CEA}}=b_{\mathrm{CEA}}+\varepsilon\left|1-\frac{\gamma_{\min}}{\gamma_{\mathrm{ref}}}\right| \tag{39}$$

C. Proposed Control to Suppress SCF

The proposed control against SCF with LADRC is given in Fig. 7. Compared with the control in the CIGRE model, the PI controls in the PLL, CCC at the rectifier side, and CEA at the inverter side are replaced by the LADRC. The negative-sequence voltage and the other disturbances are considered as the total disturbance, observed and compensated by the LESO and the LSEF, respectively. The imbalance degree of the negative-sequence voltage with respect to the commutation voltage is defined to adjust the output of the LADRC with different fault levels. The fault detection applies the method of the CFPREV [4].

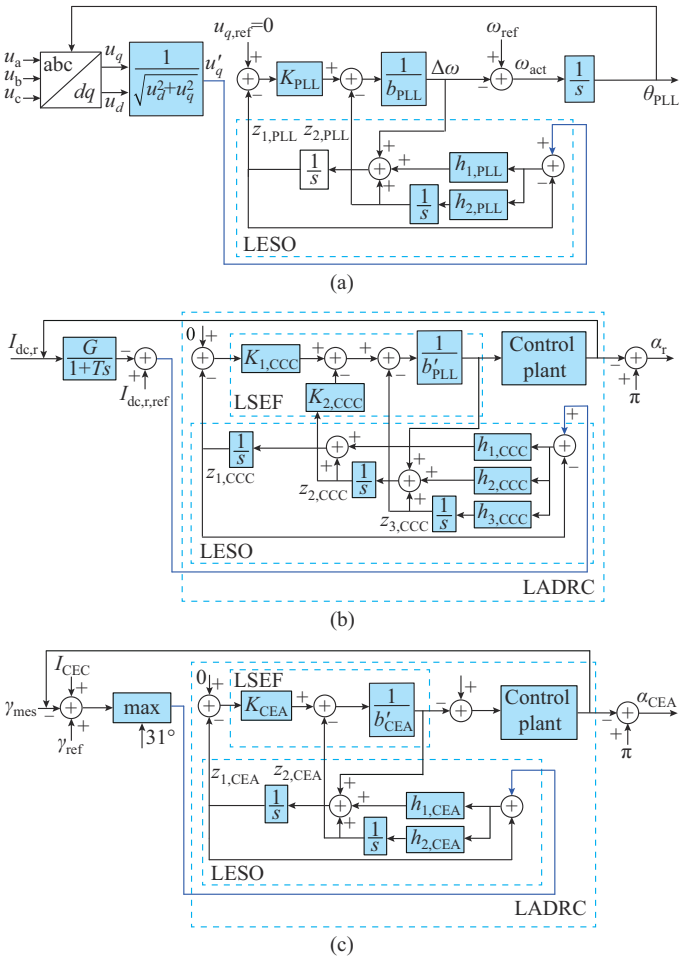

Fig. 7. Proposed control against SCF with LADRC. (a) Improved PLL. (b) Improved CCC at rectifier side. (c) Improved CEA at inverter side.

The improved PLL, CCC, and CEA controls based on the LADRC have three kinds of parameters to be tuned, i.e., the gain of the system b, the gain of the LESO h, and the gain of the LSEF K. With the mathematical model of the LCC-HVDC, b is easy to tune, as shown in (28) and (36). With the bandwidth-tuning method, tuning h and K is transformed to tuning the bandwidth of the LESO w_{LESO} and the bandwidth of the LSEF w_{LSEF}, as shown in (20) and (31), respectively. The parameters to be tuned are similar to those of the PI control.

With minor changes, the proposed control is suitable to the actual HVDC projects. In the CIGRE system, the DC current control is applied at both sides, where the DC voltage control is applied at neither the rectifier side nor the inverter side. For the actual HVDC projects, the constant voltage control at the rectifier side is to prevent overvoltage, and that at the inverter side is to keep the DC voltage constant. To maintain the DC voltage after the fault, the output of the constant voltage control of the inverter keeps at the maximum value, which does not affect the performance of the CEA during the recovery.

V. Simulations and Discussions

The HVDC system and an actual HVDC project are implemented with the PSCAD/EMTDC to verify the proposed control. The parameters of CIGRE HVDC are given in [20], [27]. The PLL in Fig. 4 and the firing pulse module are newly introduced to the CIGRE model. The firing mode is changed to the external pulse firing mode [5]. The simulation step is 20 μs and the sampling step is 50 μs, which helps collect more information about the transient process.

Considering that the AC fault near the inverter may not be cleared in time, its duration is set to be 0.2 s or 0.4 s to simulate serious fault and show the impact of the continuous fluctuation of the commutation voltage on the SCF.

A. Negative-sequence Voltage Under Asymmetrical and Symmetrical Faults

To compare the negative-sequence voltage of commutation bus and the harmonics under different fault types, the faults with the transition inductance of 0.45 H are applied at the inverter side, starting from 2.0 s and lasting for 0.2 s. The commutation voltage, harmonic distribution, and current at the valve side connected to the Y/Y transformer are presented, as shown in Fig. 8. The harmonic distributions of the positive-sequence voltage are shown in Fig. SA1 of Supplementary Material A.

The negative-sequence voltage is observed under the asymmetrical faults, and its amplitude during the CF is larger than that during the CF recovery, since the former has more harmonics of the positive-sequence voltage. In the steady state, the amplitudes of the positive and negative half-wave current of the valve connected to the Y/Y transformer, i.e., I_{YY}, are equal. After the first CF, I_{YY} is no longer symmetrical, but biased to one side due to the unidirectional conductivity of the valve group, yielding the harmonic component of the AC current and contributing to the negative-sequence voltage at the inverter bus. The negative-sequence voltage under the symmetrical fault is comparable to that under asymmetrical faults, but the former is close to 0 during the CF recovery.

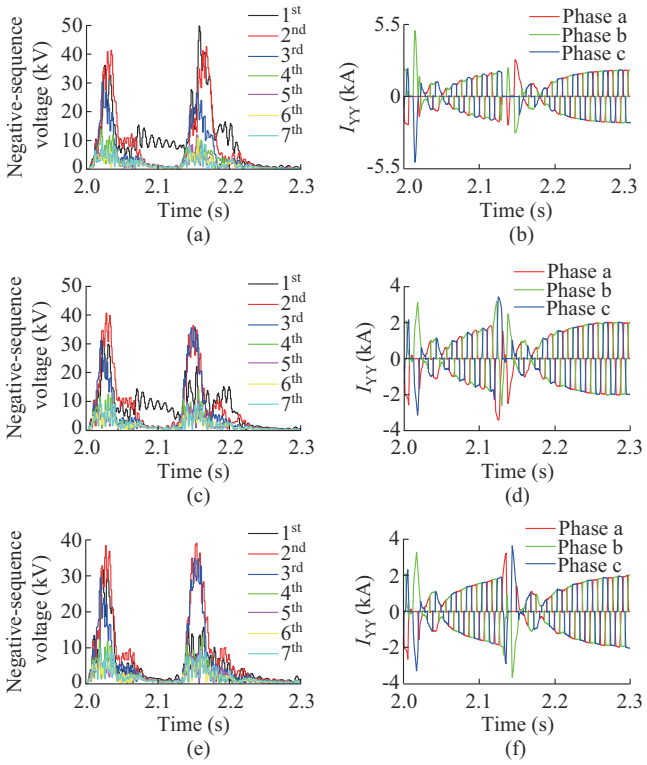

Fig. 8. Harmonic distribution of commutation voltage and current at valve side under different faults. (a) Negative-sequence voltage under SPG fault. (b) I_{YY} under SPG fault. (c) Negative-sequence voltage under double-phase-to-ground fault. (d) I_{YY} under double-phase-to-ground fault. (e) Negative-sequence voltage under symmetrical fault. (f) I_{YY} under symmetrical fault.

To show the impact of the negative-sequence voltage on the CF under the SPG and three-phase-to-ground (TPG) faults, the comparisons of the negative-sequence voltages of the fundamental frequency are presented, as shown in Fig. 9, and I_{YY} with different transition inductances is shown in Fig. SA2 of Supplementary Material A. Smaller transition inductance shows more severe fault.

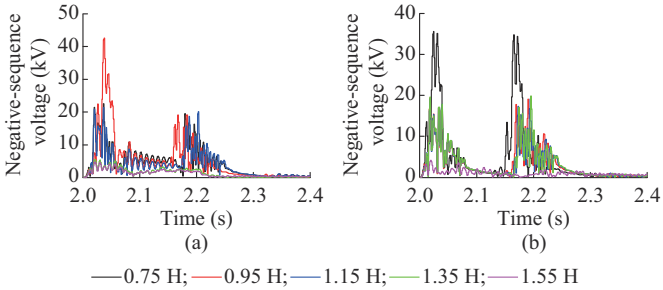

Fig. 9. Impact of fault levels on CF. (a) Negative-sequence voltage under SPG fault. (c) Negative-sequence voltage under TPG fault.

When the transition inductance increases to 1.35 H, the CF does not occur, showing that the critical inductance is between 1.15 H and 1.35 H. Similar results are found under the TPG fault. The negative-sequence voltage is comparable to that under the SPG fault with the same fault level. The

critical inductance is between 1.35 H and 1.55 H.

B. Contribution of Negative-sequence Voltage to SCF Under TPG Fault

Taking the TPG fault with a transition inductance of 0.45 H and a duration of 0.2 s as an example, the impact of the negative-sequence voltage at the AC side under the TPG fault is given in Fig. 10. Since the output of the PLL is essentially unchanged at the initial stage of fault, the actual phase of the PLL deviates from its reference value, yielding the derivation of firing phase $\Delta\theta_{\mathrm{PLL}}$ during fault. $\Delta\theta_{\mathrm{PLL}}$ is less than 0 after the first CF, then $\Delta\theta_{\mathrm{PLL}}$ gradually increases to the positive value with the system recovery, which causes α_{act} larger than α_{ref}. The difference between α_{act} and α_{ref} increases followed by $\Delta\theta_{\mathrm{PLL}}$, which reduces the extinction margin.

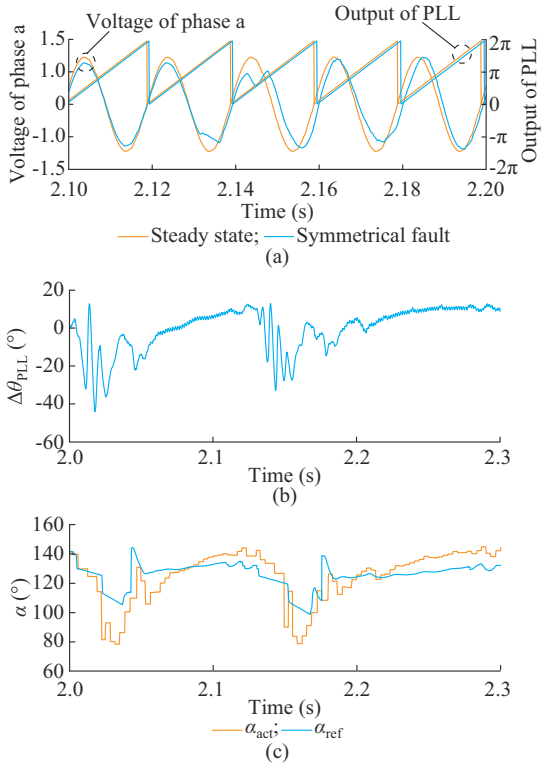

Fig. 10. Impact of negative-sequence voltage at AC side under TPG fault. (a) Voltage and ouput of PLL. (b) $\Delta\theta_{\mathrm{PLL}}$. (c) α.

Figure 11 shows the impact of the negative-sequence voltage at the DC side. With the increase of the negative-sequence voltage, I_{dc} increases and α decreases at the initial fault stage to cause the first CF, which means that the system enters stage 1. The inverter is controlled by the CEA, as shown in Fig. 11(a). Then, I_{dc} decreases, as shown in Fig. 11(b), indicating that the inverter will resume the commutation. Due to the activation of the CEC, the CCC begins to act and drives the system into the stage 2. γ decreases from the high level to the low level, but is still larger than the critical value, thus the SCF does not occur at stage 2. With the decrease of γ, the output of the CEA decreases and CCC is replaced by CEA to control the inverter, showing that the system enters stage 3. When the negative-sequence voltage increases again, as shown in Fig. 11(c), the fluctuation of the output of the CEC causes the fluctuation of the output of the CEA α_{ref}, yielding the SCF. The above findings are consistent with the conclusions in Section III. To further verify the contributions of the negative-sequence voltage to the SCF, its impacts on the AC and DC sides under the SPG fault are shown in Figs. SA3 of Supplementary Material A.

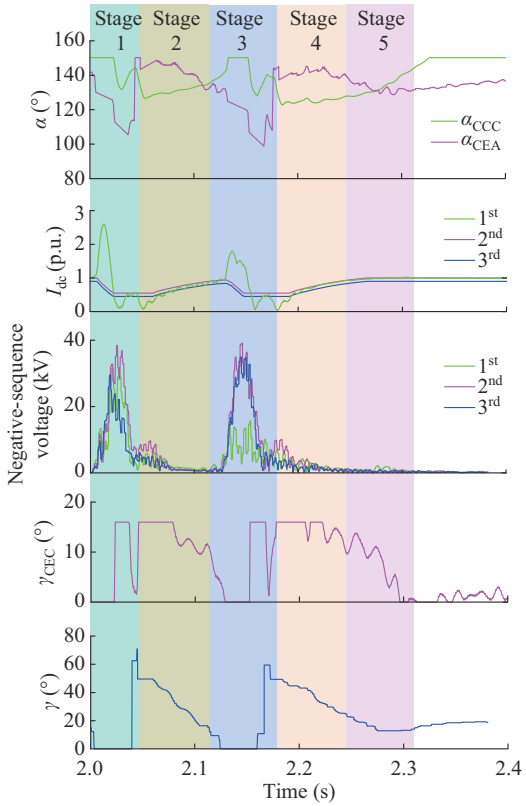

Fig. 11. Impact of negative-sequence voltage at DC side.

C. Effectiveness of Proposed Control

To illustrate the suppression effect of the proposed control on the SCF, the transient responses in control I-control III methods are compared under the symmetrical fault.

1) Control I: CIGRE control as shown in Fig. 1.

2) Control II: the control in [20].

3) Control III: the control proposed in this paper. Parameters of the proposed control in CIGRE HVDC system are listed in Table I.

With the transition inductance of 0.45 H, a TPG fault within 2-2.4 s occurs at the inverter side. Figure 12 compares the control effects under control I-control III. The transient responses of the inverter side under the TPG and SPG faults are shown in Figs. SA4 and SA5 of Supplementary Material A, respectively.

The negative-sequence voltage and its harmonics have three obvious increases by using control I, which indicates that there are two SCFs. There is no adjustment to the PLL and the control system, which causes the fluctuations of $\Delta\theta_{\mathrm{PLL}}$, α_{act}, and γ_{CEC}. Compared with control I, the negative-sequence voltage and its harmonics are reduced by one rise behavior by using control II, hence the fluctuations of $\Delta\theta_{\mathrm{PLL}}$, α_{act}, and γ_{CEC} are suppressed. Compared with control II, control III better suppresses the negative-sequence voltage in-

crease and the fluctuations of $\Delta\theta_{PLL}$, α_{act}, and γ_{CEC}. The above findings show that control III alleviates the adverse effect of negative-sequence voltage on suppressing the SCF, and is better than those of control I and control II.

TABLE I
PARAMETERS OF PROPOSED CONTROL IN CIGRE HVDC SYSTEM

Control type	b	w_{LESO}	w_{LSEF}
PLL based on LADRC	1	15.0	3.4
CCC based on LADRC	−38	37.5	11.8
CEA based on LADRC	−30	34.0	6.6

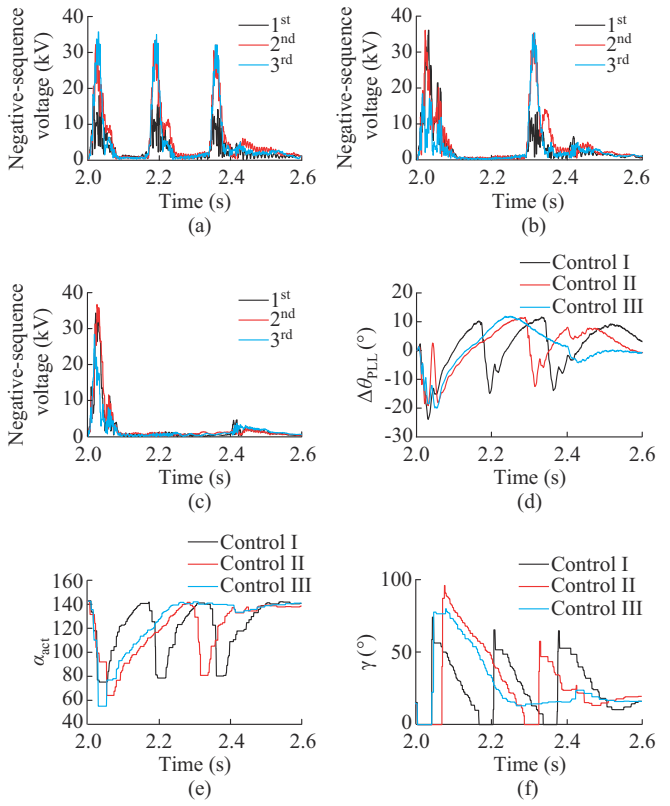

Fig. 12. Comparisons of control I, control II, and control III under TPG fault. (a) Negative-sequence voltage with control I. (b) Negative-sequence voltage with control II. (c) Negative-sequence voltage with control III. (d) $\Delta\theta_{PLL}$. (e) α_{act}. (f) γ.

D. Control Effect Validation Under TPG Faults

To further test the robustness and the ability against the SCF of the proposed control, it is necessary to compare the suppression effect in different SCF scenarios. The transition inductance varies from 0.20 H to 0.95 H with a step size of 0.05 H under the TPG fault, and the SCR varies from 2 to 3 with a step size of 0.5. A larger short-circuit ratio (SCR) means a strong AC system. The moment of fault varies from 2.000 s to 2.010 s with a step size of 0.001 s and a fault duration of 0.4 s. The results are shown in Fig. 13, and those under the SPG fault are shown in Fig. SA6 of Supplementary Material A. By using control I, there are lots of red and yellow areas with different faults, showing that the inverter is vulnerable to the SCF. By using control II, some yellow areas turn to blue at most of the fault levels. By using control III, there are more blue areas than those using control II, and some blue areas turn to green. As shown in Fig. 13(d), the control effect of the proposed control is better than the other two controls, especially with the obvious suppression effect to the SCF under weak AC systems. Above results show that the SCF risk is reduced notably by using the proposed control.

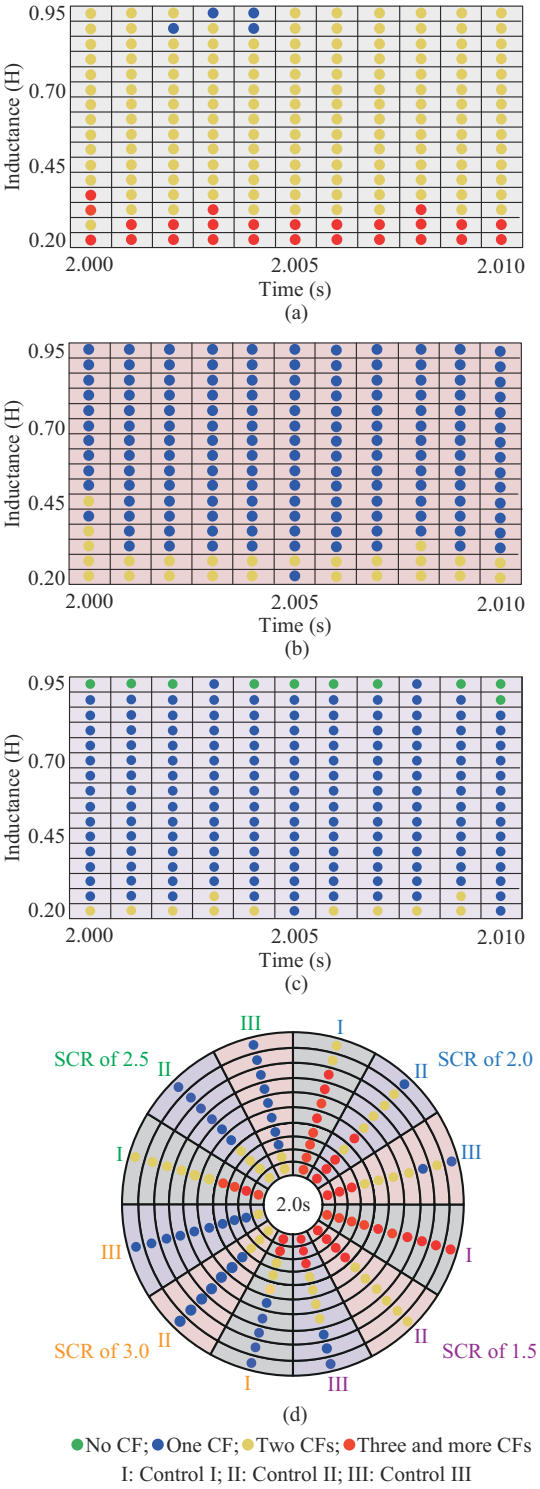

Fig. 13. Control effect with different fault conditions under TPG fault. (a) Control I. (b) Control II. (c) Control III. (d) Different SCRs.

E. Control Effect on SCF of Actual HVDC Project

To verify the control effect of the proposed control, an actual ±1100 kV Changji-Guquan project (1/2 bipolar operation modes) is applied [4], [6] and compared with that using the SIEMENS control. With the fault duration of 0.2 s, the TPG and SPG faults are applied at the inverter side. The responses of γ and U_{ac} with the proposed control and SIEMENS control are shown in Fig. SA7 of Supplementary Material A. Parameters of the proposed control in Changji-Guquan project are listed in Table II.

TABLE II
PARAMETERS OF PROPOSED CONTROL IN CHANGJI-GUQUAN PROJECT

Control type	b	w_{LESO}	w_{LSEF}
PLL based on LADRC	1	22	6
CCC based on LADRC	–27	41	16
CEA based on LADRC	–21	36	9

Figure 14 shows the suppression effect on SCF under different faults, where Cases 1-4 represent the control IV under TPG fault, control III under TPG fault, control IV under SDG fault, and control III under SPG fault, respectively. Although under serious faults, the suppression effect is limited, the proposed control does not increase the number of the CF, which shows its adaptability to the fault conditions, and SCF could be avoided in the actual HVDC project.

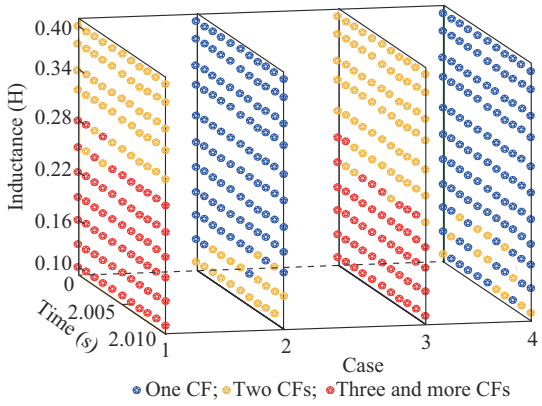

Fig. 14. Suppression effect to SCF under different faults.

VI. CONCLUSION

In this paper, the SCF suppression considering the negative-sequence voltage after the fault at the inverter side is studied. With the harmonics of the positive-sequence voltage, the analytical expression of the negative-sequence voltage with the commutation voltage is derived. The contribution of the negative-sequence voltage to the SCF is found by deriving the analytical expressions of the outputs of the PLL and the inverter control with respect to the time. The improved control based on the LADRC to replace the PI control against the negative-sequence voltage is proposed to suppress the SCF. Some conclusions are found as follows.

1) Since the modulation to the AC voltage and the DC current by the inverter is nonlinear, the AC voltage has the negative-sequence components due to harmonics after the symmetrical fault. During the CF process, the amplitude of the negative-sequence voltage under the symmetrical fault is comparable to that under the asymmetrical fault.

2) At the AC side, the negative-sequence voltage causes the phase shift of the PLL, which yields the deviation between the actual value and the reference value of the firing angle. At the DC side, the actual value of the firing angle is larger than the reference value of the firing angle when the CCC is switched to the CEA. These behaviors reduce the extinction margin and finally cause the SCF.

3) Compared with the traditional PI control and ADRC, the proposed control alleviates the adverse effect of the negative-sequence voltage on the commutation process, reduces the risk of the SCF, and improves the recovery speed of the system.

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