An Improved Submodule Capacitor Condition Monitoring Method for Modular Multilevel Converters Considering Switching States

Zan Jia, Yongjie Luo, Qianggang Wang, Niancheng Zhou, Yonghui Song, and Dachuan Yu

Abstract—The capacitor is one of the most important components in a modular multilevel converter (MMC). Due to the chemical process and the aging effect, the capacitor is subject to deterioration over time which is usually manifested by a drop in capacitance. To identify the abnormal capacitors and enhance the reliability of MMCs, an improved submodule (SM) capacitor condition monitoring method is proposed in this paper. The proposed method estimates the capacitance during each control cycle based on the switching states of SMs, offering advantages such as high accuracy and no adverse influence on the operation of MMCs. Firstly, the aging differences of capacitors in different SMs per arm of MMC are analyzed. Then, the capacitances of SMs that switch on the state are calculated based on the relationship between the capacitor voltage and current during each control cycle. A data processing algorithm is proposed to improve the accuracy of capacitance estimation. Finally, the simulation and the real-time control hardware-in-the-loop test results based on real-time digital simulator (RTDS) show the effectiveness of the proposed method.

Index Terms—Modular multilevel converter (MMC), capacitor condition monitoring, data processing, submodule switching state.

I. Introduction

MODULAR multilevel converter (MMC) has been widely utilized in the fields of offshore wind farms and high-voltage direct current (DC) transmission, for its excellent features such as compact design, low harmonic performance, and high efficiency [1]-[3]. As the voltage level and transmission capacity of the MMC increase, the number of series-connected submodules (SMs) in the arm becomes significantly high. Consequently, the reliability of an MMC may degrade over time due to the large number of SMs [4].

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The SM topology of MMC generally adopts a half-bridge or full-bridge circuit. The capacitor is the core component of the SM, accounting for nearly 60% of the size and over 50% of the weight [5]. According to data statistics, capacitors are one of the most fragile components in power electronic devices [6]. The capacitor in the MMC is subject to deterioration over time because of chemical processes and aging effects, which is usually manifested by a decreasing capacitance [7]. The decreasing capacitance can impact the normal operation of MMCs adversely, or even result in explosions [8]. Thus, monitoring the capacitances and detecting the abnormal capacitors in time are essential for the reliable operation of MMC.

In recent years, many research results of capacitance estimation of SM capacitors for MMC have been published, aiming to improve the reliability of MMC systems. The research results can be broadly classified into two categories: ① estimate the capacitance based on the capacitor impedance model, and ② evaluate the condition of capacitor by considering the impact of capacitance drop on the operation characteristics of MMC.

According to the type of needed electrical signals, the first category includes two subtypes: periodic small-signal ripples and nonperiodic large-signal charging/discharging profiles [9]. In [10], the capacitance is estimated by processing with the recursive least squares (RLS) method. However, the complex algorithms are often prohibitively resource-consuming. Similarly, the second harmonic impedance is extracted from the inherent second-harmonic voltage/current ripple that circulates in the SM capacitors to evaluate capacitance [11], [12]. The above methods require high requirements on the filter and are computationally costly. The concept of reference SM is first introduced in [13], where voltage magnitude of an SM capacitor within the arm is selected as the value of a reference for comparison with others. The switching pulses of the reference SM and the monitored SM are synchronized, and the capacitance is estimated by comparing the voltage ripple of two SMs. Based on this, the monitoring accuracy is improved by increasing the voltage ripple of the monitored SM and the reference SM [14]. The main disadvantages of such methods are that they have to be estimated in advance using another capacitor condition monitoring method, and the monitoring accuracy is limited by reference

SM. For the second subtype, the discharging curve of SM ca-
pacitors in connection with the parallel bleeding resistors is
leveraged to estimate capacitance [15]. One shortcoming of
the method is that at least six SMs are turned off during the
discharging process due to the symmetrical operation of the
SMs. A capacitor condition monitoring method based on the
DC-side start-up procedure of MMC is proposed in [16].
The SM capacitance is estimated by investigating its relation-
ship with the time constant of charging and electric parame-
ters. One distinctive disadvantage is that, in electrical engi-
neering practice, continuous operation of MMCs is one of
the top priorities and shutdown is only acceptable during ma-
jor failure and scheduled maintenance [17].

The second category focuses on the changing characteris-
tics of MMC in response to the capacitance decrease. In
[18], a capacitance estimation method of MMC considering
the relationship between the capacitor voltage variation and
the switching angle of driving signals is proposed. The RLS
method is used to reduce the uncertainties related to mea-
surements. A capacitor condition monitoring method is pro-
posed in [19], which uses the back propagation neural net-
work to map the relationship between switching frequencies
of SM and capacitance. Based on the influence of capaci-
tance drop on the average capacitance in one arm for MMC,
a capacitor condition monitoring method is proposed to ana-
lyze the variation of equivalent switching function in [20].
In [21], the capacitance is estimated by calculating the differ-
ence between the actual conduction time and the rated con-
duction time. The compensation for dead time is added to en-
hance the monitoring accuracy. The main focus of this kind
of method is to investigate the impact of capacitance drop
on the switching signals of SM in MMC. It evaluates the ca-
pacitance by analyzing the relationship between theoretical
values and actual sampled values. However, the switching
status of SM is significantly influenced by the modulation
strategy and capacitor voltage balance method. Furthermore,
the extra control effort and processor burden are required for
accuracy improvement and data filtering.

In this paper, an improved SM capacitor condition moni-
toring method for MMCs considering hundred-microsecond
switching states of SMs is proposed. The effect of structure
and operation characteristics of MMC on the aging of capaci-
tors among SMs is analyzed. Based on the capacitor voltage
increment during the adjacent control cycle (usually 100 μs)
and the arm current, capacitances of the SMs with the ON
state during the current control cycle are calculated. The da-
ta processing is used to filter valid capacitance calculation re-
sult. A more accurate capacitor condition monitoring result
can be obtained by averaging the effective data calculated
during the monitoring period. The performance of the pro-
posed method is validated through the simulation by MAT-
LAB/Simulink and the hardware-in-the-loop (HIL) test based
on real-time digital simulator (RTDS).

The rest of this paper is organized as follows. Section II
analyzes the SM capacitor aging of MMC. The capacitance
estimation method of MMC is proposed in Section III. This
is followed by simulation and HIL test results in Section IV

and Section V. Section VI concludes this paper.

II. SM CAPACITOR AGING OF MMC

A. Structure of MMCs

A three-phase MMC consists of six arms. The topology of
SM circuit is illustrated in Fig. 1. Each arm is equipped with
N SMs and an arm inductor L. For clarity, phase a is high-
lighted in this paper due to the symmetrical nature of the
three-phase legs. In Fig. 1, u_{dc} and i_{dc} are the DC-link volt-
age and current, respectively; u_a and i_a are the voltage and
current on alternating current (AC) side, respectively; u_{au}
and u_{al} are the total voltages across the SMs in the upper
and lower arms, respectively; and i_{au} and i_{al} are the currents
flowing through the upper and lower arms, respectively.
Each SM contains a DC storage capacitor C_{au} with a corre-
sponding voltage u_{cau} and a half-bridge configuration consist-
ing of two power switch devices (T_1 and T_2) with freewheel-
ing diodes (D_1 and D_2). Taking the upper arm as an exam-
ple, the switching function of the SM S_{au} can be defined in
(1). u_{sau} and i_{cau} can are given by (2) and (3), respectively.

$$S_{au} = \begin{cases} 1 & T_1 \text{ is ON and } T_2 \text{ is OFF} \\ 0 & T_1 \text{ is OFF and } T_2 \text{ is ON} \end{cases} \quad (1)$$
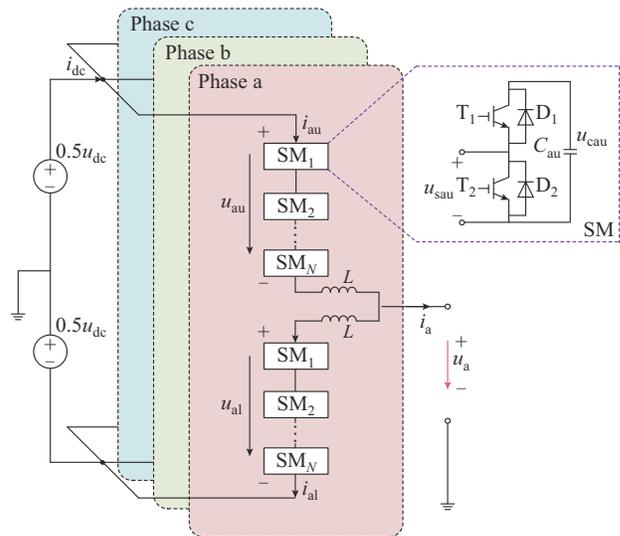

Fig. 1.   Topology of SM circuit.

$$u_{sau} = S_{au} u_{cau} \quad (2)$$

$$i_{cau} = S_{au} i_{au} \quad (3)$$

where u_{sau} is the output voltage of SM on AC side; and i_{cau}
is the current flowing through the capacitor. If i_{au} is positive,
the capacitor in the ON-state SM ($S_{au} = 1$) gets charged, in-
creasing u_{cau}. Meanwhile, the SM in the OFF state ($S_{au} = 0$)
functions as a bypass, keeping u_{cau} unchanged. Conversely, if
i_{au} is negative, the capacitor in the ON-state SM discharges,
causing a decrease in u_{cau}. Similarly, u_{cau} remains unchanged
in the OFF state of the SM. Detailed information regarding
the current paths and switching states in an SM is presented,
as shown in Table I.

TABLE I
TWO SWITCHING STATES OF AN SM

SM state	S_{au}	u_{sau}	i_{au}	C_{au}	Device
ON	1	u_{cau}	>0	Charge	D_1
			<0	Discharge	T_1
OFF	0	0	>0	Bypass	T_2
			<0	Bypass	D_2

B. Differences Among SM Capacitor Aging

The SM capacitors in the MMC are subject to deterioration over time, which is typically manifested by a drop in capacitance. Even though the SM capacitors in the MMC have the same rated values, the aging process of capacitors in different SMs per arm may vary due to diversified operation environments and control strategies. Indeed, these differences in aging rates can be analyzed from two perspectives: structure and operation characteristics of MMC.

1) Impact of Structure Characteristic on MMC

The primary influencing factors of SM capacitor aging include humidity, environmental temperature, hot-spot temperature of the capacitor as well as the voltage and current stress endured by the capacitors [9]. The prevalent empirical lifetime model for capacitors is shown in (4) [22].

$$L = L_0 \left(\frac{V}{V_0} \right)^{-n} \exp \left[\frac{E_a}{K_B} \left(\frac{1}{T} - \frac{1}{T_0} \right) \right] \qquad (4)$$

where L and L_0 are the lifetime under the operation and test conditions, respectively; V and V_0 are the voltages under operation and test conditions, respectively; T and T_0 are the temperatures in Kelvin under the operation and test conditions, respectively; E_a is the activation energy; K_B is Boltzmann's constant (8.62×10^{-5} eV/K); and n is the voltage stress exponent.

In the field of high-voltage DC transmission, MMCs are usually characterized by high transmission capacities and large footprint areas. Both the geometrical structure and the heat transfer (including conduction, convection, and radiation) of the SM are complex. For the MMC with many SMs, the local ambient temperature of an SM is inevitably affected by the temperature variation of the neighboring subsystems. Thus, the SM and arm inductors are regarded as a unit. A thermal matrix method is applied to consider the system-level thermal cross-coupling (TCC) [23].

$$T_{la} = Z_a P_{SM} + T_{ga} \qquad (5)$$

where T_{la} is the local ambient temperature vector of each SM; Z_a is the local ambient to global ambient thermal impedance, characterizing the TCC effects between SMs and the impact of the cabinet; P_{SM} is the total loss of SMs; and T_{ga} is the ambient temperature. Studies have shown that the hot-spot temperature divergence between different SMs is up to 17 °C [23]. Based on (4), the different temperatures due to the characteristic of MMC can lead to varying aging and lifetime of the capacitors among SMs.

2) Impact of Operation Characteristic of MMC

The rate of voltage and current change significantly im-

pacts the lifetime of capacitors, as shown in (4). In order to reduce operation losses, MMC usually adopts a voltage balance method with a low switching frequency [24]. Due to the differences in switching instants, the voltage balance method can affect the rate of voltage and current changes among capacitors in different SMs. As shown in Fig. 2, two SMs are randomly selected in one arm. There are different rates of voltage and current changes for the two SMs. And the difference will be more significant as the switching frequency decreases, which could impact the aging process of different capacitors.
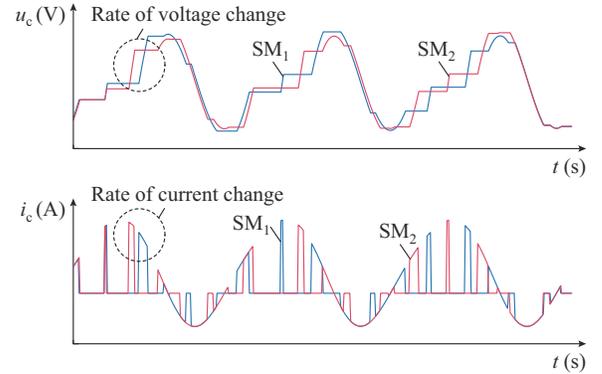

Fig. 2. Voltage and current for different SMs.

Besides, the differences in aging also contribute to the varying degrees of capacitance degradation of the capacitors. As a consequence, before replacing the deteriorated capacitor, the MMC needs to operate with varying capacitances among SMs on a single arm, which can further increase the difference in voltage stress among SMs and affect the operation characteristics of MMC [8]. Therefore, the unbalanced aging of capacitors in various SMs in one arm might be exacerbated.

In summary, the structure and operation characteristics of MMC result in significant differences in SM capacitor aging among different SMs per arm. The failure to replace aged capacitors may promptly lead to SM failures and even capacitor explosions in extreme cases. Therefore, it is crucial to monitor and ensure that the capacitance of SM does not drop below the threshold value, in order to maintain a safe and reliable operation of the MMC system.

III. CAPACITANCE ESTIMATION METHOD

A. Principle of Capacitance Estimation

The SM capacitor of MMC often operates under low-frequency conditions. The relationship among voltage u_{caui}, current i_{caui}, and capacitance C_{aui} of the ith SM is described as:

$$u_{caui} = u_{caui0} + \frac{1}{C_{aui}} \int_0^t i_{caui} \, dt \qquad (6)$$

where u_{caui0} is the DC component of the capacitor voltage; and C_{aui} and i_{caui} are the capacitance and current in the ith SM, respectively.

Based on (1), (3), and (6), it can be observed that the charging or discharging state of the SM capacitor is deter-

mined by the switching function and arm current. The value of the first derivative of a discrete signal such as i_{au} remains approximately equal for two consecutive control cycles. In the context of high-voltage and large-capacity MMCs, the arm current increment between adjacent control cycles can reach the magnitude of several tens of amperes. Several references endorse the application of linear interpolation for calculating voltage and current across adjacent control cycles in fault detection and condition monitoring [25], [26].

In order to prove the accuracy of linear interpolation, current errors of calculation using linear interpolation are analyzed through MMC simulation. Taking the upper arm of phase a as an example, i_{au} is illustrated in Fig. 3. The control frequency of MMC in practical engineering is usually set to be 10 kHz [27]. Three areas spanning two control cycles are magnified in the figure, marked as Area 1, Area 2, and Area 3, respectively. The variation of arm current across adjacent control cycles exhibits a linear trend. Therefore, as an illustration with arm current $i_{au} > 0$, if the ith SM is switched ON during the kth control cycle, the charging current of the capacitor can be expressed as:

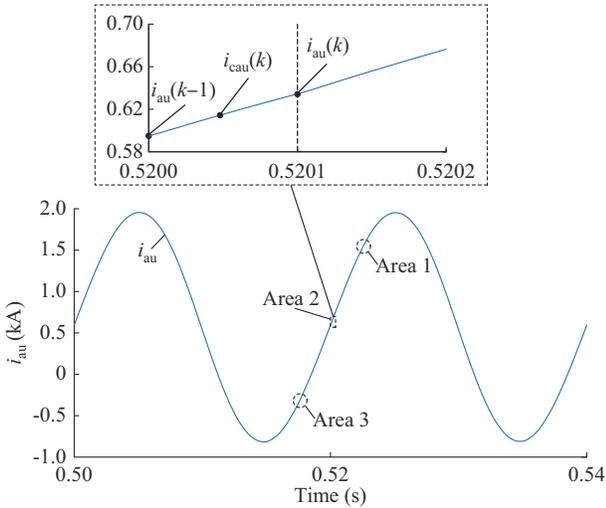$$i_{caui}(k) = \frac{i_{au}(k) + i_{au}(k-1)}{2} \tag{7}$$

Fig. 3.　Upper arm current of phase a.

According to (6) and (7), the capacitance of the ith SM during the kth control C_{aui} cycle can be computed by:

$$C_{aui} = \frac{i_{caui}(k)\Delta t}{u_{caui}(k) - u_{caui}(k-1)} \tag{8}$$

$$\Delta t = \frac{1}{f_{control}} \tag{9}$$

where $u_{caui}(k-1)$ is the capacitor voltage during the last control cycle; $u_{caui}(k)$ is the capacitor voltage during the current control cycle; $f_{control}$ is the control frequency; and Δt is the charging time. The random errors in the measured data (such as arm current and capacitor voltage) make the capacitance calculated by (8) inevitably inaccurate to some extent. We aim to enhance estimation accuracy by conducting multiple calculations and averaging the results. Under normal operation, N capacitor voltages in one arm are balanced, the ca-

pacitor voltages meet the relation in (10).

$$u_{cau1} = u_{cau2} = \ldots = u_{cauN} \tag{10}$$

Substituting (3) and (6) into (10), (11) is obtained as:

$$\int_{t_1}^{t_2} \frac{S_{au1}i_{au}}{C_{au1}} dt = \int_{t_1}^{t_2} \frac{S_{au2}i_{au}}{C_{au2}} dt = \cdots = \int_{t_1}^{t_2} \frac{S_{auN}i_{au}}{C_{auN}} dt \tag{11}$$

In [8] and [21], S_{aui} represents equivalent reference as:

$$S_{aui} = \frac{1 + x_{aui}}{2} \tag{12}$$

It is important to note that x_{aui} is related to S_{aui} and the mathematic expression for x_{aui} is difficult to deduce.

Based on (12), (11) can be simplified and the relationship among the capacitance of SMs per arm can be obtained as:

$$\frac{1 + x_{au1}}{C_{au1}} = \frac{1 + x_{au2}}{C_{au2}} = \cdots = \frac{1 + x_{auN}}{C_{auN}} \tag{13}$$

The continuous addition operation is implemented to (13), and (14) is obtained as:

$$\frac{1}{C_{au1}} \sum_{k=1}^{N_x} S_{au1k} = \frac{1}{C_{au2}} \sum_{k=1}^{N_x} S_{au2k} = \cdots = \frac{1}{C_{auN}} \sum_{k=1}^{N_x} S_{auNk} \tag{14}$$

where N_x is the number of control cycles during a monitoring period $T_{monitor}$, which is defined in (15). In this paper, the control frequency is set to be 10 kHz, and based on (9), it can be obtained that $\Delta t = 0.0001$ s.

$$N_x = \frac{T_{monitor}}{\Delta t} \tag{15}$$

Based on (10)-(14), different SMs per arm undergo nearly equal charging and discharging time to maintain voltage balance during one fundamental frequency cycle. Therefore, selecting an integer multiple of the fundamental frequency cycle as the capacitor condition monitoring period ensures that all the SM capacitors per arm can be monitored.

It should be noted that the capacitance of an SM can only be estimated when the SM is in the ON state during the previous control cycle. According to the switching state of the ith SM, the number of calculations $N_{monitori}$ within the monitoring period can be expressed as:

$$N_{monitori} = \sum_{k=1}^{N_x} S_{auik} \tag{16}$$

Combining with (6)-(14), C_{aui} is calculated as:

$$C_{aui} = \frac{1}{N_{monitori}} \sum_{k=1}^{N_x} \frac{i_{au}(k)S_{auik}\Delta t}{u_{caui}(k) - u_{caui}(k-1)} \tag{17}$$

For different SMs, the capacitor current can be expressed as $i_{caui} = i_{au}S_{aui}$, as shown in (17). The capacitor current is equal to the arm current when the SM is in the ON state. In (17), the capacitor current of each SM is multiplied. The calculation in (17) neglects the increment of arm current during the control cycle, which may result in errors in the estimation of capacitance. The circulating current in MMC is eliminated [28], and the axial symmetry of the arm current can partially compensate for the error (i.e., $error$), as shown in Fig. 4, where G denotes the switching signal.

Taking $i_{au} > 0$ as an example, if the current is increasing, the calculated capacitance result is underestimated. Conversely, the results of the capacitance calculation may be overestimated when the current decreases. Within one fundamental

frequency cycle, the capacitor undergoes multiple charging and discharging cycles. Therefore, employing an averaging method to the calculation results facilitates the mitigation of the errors. During normal operation of the converter, (17) can be repeated to identify any changes in the capacitance of every SM. Since capacitor degradation is a slow process, it is not necessary to store all estimated capacitance values, nor is it mandatory to store the calculated values at a high rate. Periodic estimation of SM capacitors can significantly enhance the reliability of the MMC.
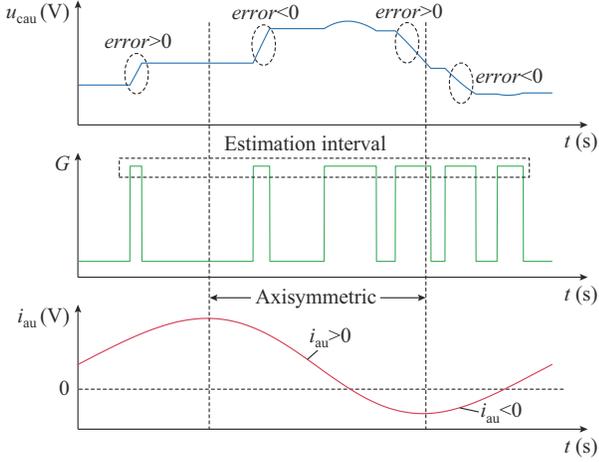

Fig. 4. Charging and discharging process of SM capacitor.

B. Capacitance Estimation Method

Based on the analysis in Section III‑A, a capacitance estimation method for SM capacitors is proposed. The flowchart of the capacitance estimation method is illustrated in Fig. 5, where $t(k)$ represents the kth control cycle; $u_{ci}(k)$ is the capacitor voltage of the ith SM during the kth control cycle; and N represents the number of SMs per arm. The data required for capacitance estimation can all be obtained from the valve control system of MMC, without requiring any additional hardware.
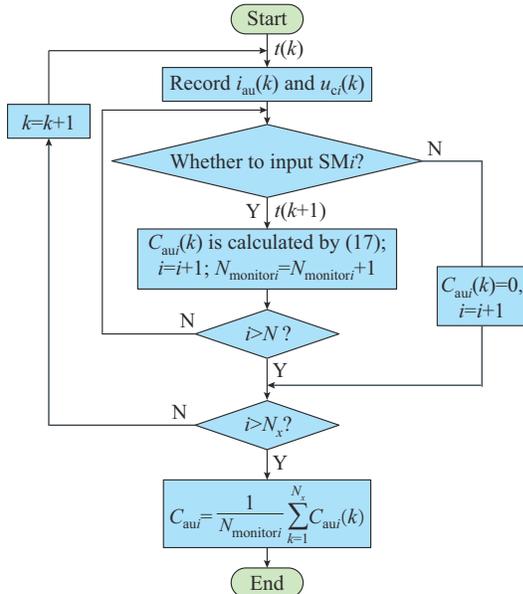

Fig. 5. Flowchart of capacitance estimation method.

In addition, considering the influence of voltage and current sensor precision as well as sampling errors in actual MMC systems, it is imperative to enhance the accuracy of capacitance estimation. The flowchart of data processing is shown in Fig. 6, where n_{numi} is the number of valid capacitance estimations for the ith SM; C_{min} and C_{max} are boundaries for data processing; and C_{sumi} is the sum of the effective capacitance calculation results of the ith SM during the monitoring period. Figure 5 entails the calculation of the average value for all capacitance estimation results of the same SM within the monitoring period, serving as the reference value for Fig. 6. The reference value of capacitance for different SMs are independently calculated, taking into account the aging condition of each capacitor.
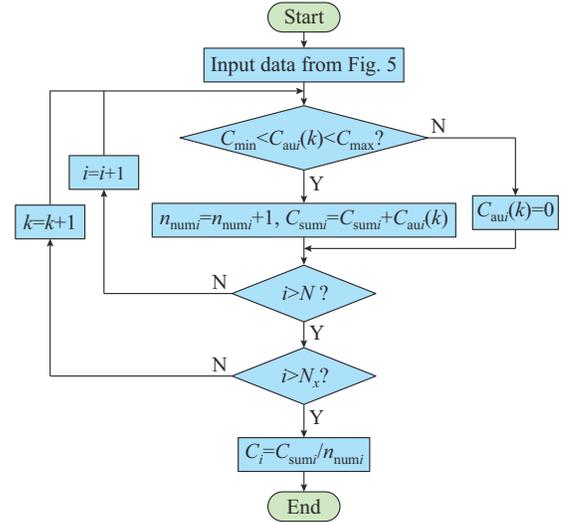

Fig. 6. Flowchart of data processing.

IV. SIMULATION VALIDATION

A. Simulation Results

In order to validate the efficacy of the proposed capacitance estimation method, a simulation is constructed in MATLAB/Simulink. The detailed parameters of MMC are listed in Table II. The MMC operates under a unity power factor inverter condition with effective circulating current suppression.

TABLE II
PARAMETERS OF MMC

Parameter	Value
Power rating (MW)	500
AC voltage (kV)	150
DC bus voltage (kV)	300
Number of SMs per arm	150
SM capacitance (mF)	10
Arm inductance (mH)	72
Control frequency (kHz)	10

Figure 7 shows the steady-state waveform of the MMC in the inverter mode, which includes the AC voltage u_{abc}, current i_{abc}, as well as the arm voltage u_{arm} and arm current i_{arm}

of phase a. The proposed method is started at 0.5 s. The simulation results indicate that the proposed method does not affect the stable operation of the MMC.
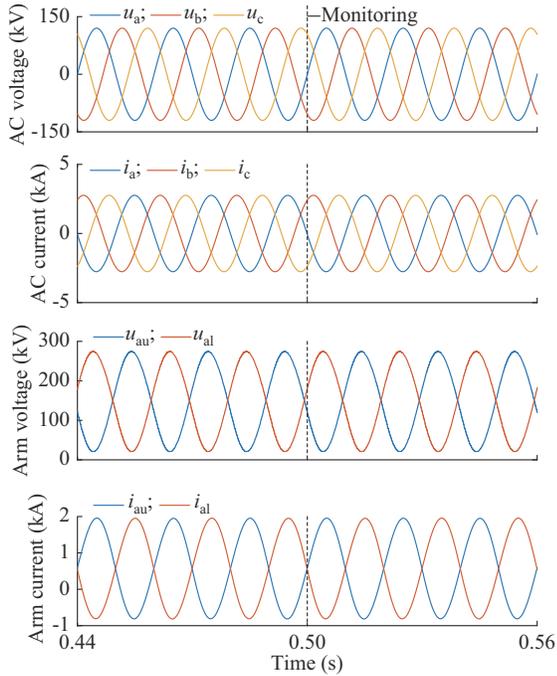

Fig. 7.   Steady-state waveform of MMC in inverter mode.

The capacitances for the SMs per arm are specified as follows: $C_1 = 11$ mF, $C_2 = 9.5$ mF, $C_3 = 9$ mF, $C_4 = 8.5$ mF, $C_5 = 8$ mF, $C_6, C_7, ..., C_{150} = 10$ mF. The capacitance estimation duration is set to be three fundamental frequency cycles. The capacitor condition monitoring results of the first 10 SMs on the upper arm of phase a are depicted in Fig. 8. The estimation errors for C_1, C_2, C_3, C_4, C_5, and $C_6, C_7, ..., C_{10}$ are 0.84%, 1.2%, 1.42%, 1.42%, 1.64%, and 1.17%, respectively. In an actual project, the monitoring accuracy of capacitors used in MMC is typically required to be within 1% [9]. In addition, it should be noted that the simulation does not consider the potential accuracy interference caused by the sampling equipment. Hence, it is essential to enhance the accuracy of the capacitance estimation.

Based on the proposed method, the error analysis are presented, as illustrated in Fig. 9, where C is the monitored capacitance. Taking SM_1 as an example, a detailed analysis of its monitoring process is conducted. The simulation results reveal that most errors occur during the transitions of SM switching states and at the zero-crossing points of arm current. In the simulation, the simulation step is set to be 1×10^{-5} s, meaning that for the capacitor voltage, the actual updating frequency is 100 kHz. For the monitoring system, its calculation frequency is synchronized with the control frequency, resulting in a data updating frequency of 10 kHz. Given that the calculation time interval of the capacitor condition monitoring should be less than 1×10^{-4} s, the observed simulation results reveal a delay of one simulation step in the voltage sampled by the monitoring module compared with the voltage of the MMC simulation system, as shown in Fig. 10.
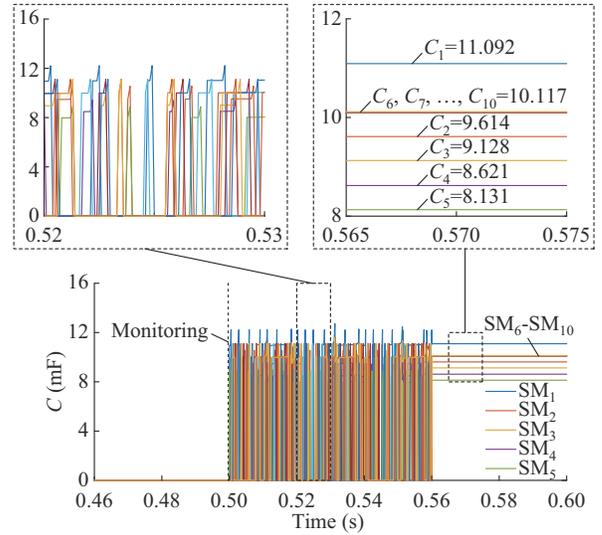

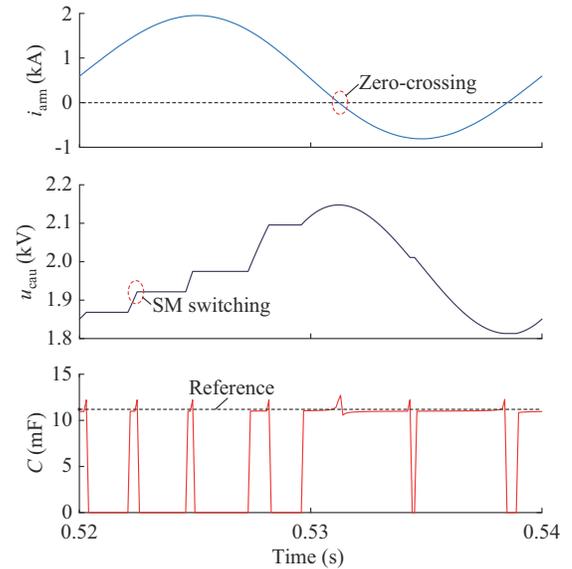Fig. 8.   Capacitor condition monitoring results of the first 10 SMs.

Fig. 9.   Error analysis of capacitance estimation.

Each time, the SM switches from the ON to OFF state, the capacitor voltage increment Δu_1 sampled by the monitoring system is smaller compared with the actual capacitor voltage increment Δu_2 of the simulation. Based on (8), the decrease in capacitor voltage increment leads to larger capacitance calculation results. Therefore, there is a "spike" with each switching in the SM state from ON to OFF state.

At the zero-crossing point of the arm current, there is an inherent error in the charging and discharging currents of the capacitor. At this time, there might be errors in the calculated capacitance, as shown in Fig. 9. Hence, additional data processing based on Fig. 6 is essential to enhance the precision of the capacitance estimation.

From the simulation results in Fig. 8, it is evident that the capacitance obtained exhibits a noteworthy level of accuracy. Therefore, C_{min} and C_{max} can be determined based on the capacitance estimation results in Fig. 8, as shown in (18).
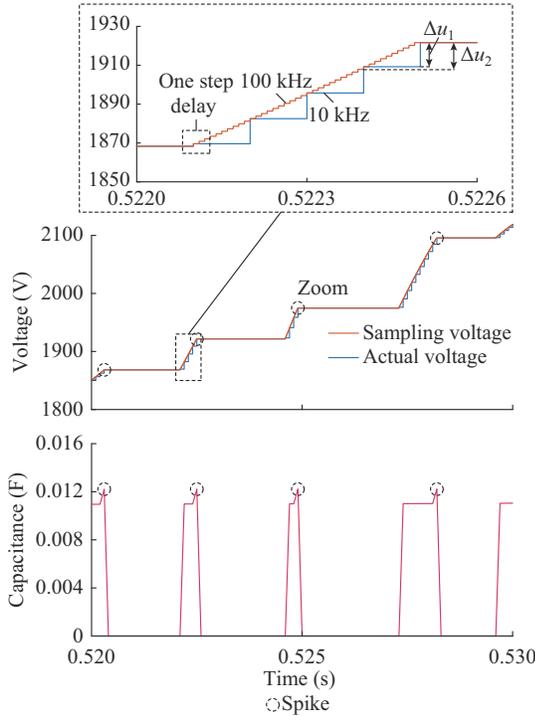
Fig. 10.   Process analysis of capacitance estimation.

excellent parallel computing capability of FPGA, all SMs requiring capacitance estimation are divided into 10 groups. Thus, the proposed method requires only a small amount of software resources to achieve capacitor condition monitoring. Its advantages can be demonstrated below by comparison with existing capacitance estimation methods.

Previous studies conducted on DC capacitance estimation for MMC applications are summarized, as shown in Table IV. State-of-the-art methods utilize the capacitor impedance model or switching signals to estimate the capacitance of the SM. The method in [10] employs the recursive weighted least square method, which imposes high computation burden. Similarly, [12] requires the calculation of second-harmonic impedance. The reference SM is introduced in [13]. This method has to change the state of SM under test and influence the normal operation of MMC. The capacitance estimation based on the DC-side start-up procedure of MMC is proposed in [16]. However, several MMC applications require continuous operation. Considering the characteristics of the above methods, the most suitable state-of-the-art solution to DC capacitance estimation is the one proposed in [21]. Hence this method is chosen for more detailed comparison.

$$
\begin{cases}
C_{\min} = 0.95 C_{\mathrm{mon}} \\
C_{\max} = 1.05 C_{\mathrm{mon}}
\end{cases} \tag{18}
$$

where C_{mon} is the calculated capacitance for the SM based on Fig. 5. The accurate capacitance estimation results obtained by filtering out the data with significant errors using (18) can be observed in Fig. 6. The simulation results of the proposed method and the existing method [21] are shown in Table III, where C_{act} is the actual capacitance; C_{exi} is the monitoring results of the existing method; and C_{pro} is the monitoring results of the proposed method. $\mathrm{SM}_{6\text{-}10,\max}$ denote the estimation results in SM_6-SM_{10} with the maximum errors.

TABLE III
CAPACITANCE ESTIMATION RESULTS OF TWO METHODS

SM	C_{act} (mF)	C_{exi} (mF)	C_{pro} (mF)
SM_1	11.0	11.12	11.01
SM_2	9.5	9.54	9.49
SM_3	9.0	9.04	9.01
SM_4	8.5	8.62	8.51
SM_5	8.0	7.88	7.99
$\mathrm{SM}_{6\text{-}10,\max}$	10.0	9.96	9.99

TABLE IV
COMPARISON OF STATE-OF-THE-ART CAPACITANCE ESTIMATION METHODS FOR MMC

Method	Software	Performance effect	Special operation
[10]	+++	No	No
[12]	++	No	No
[13]	+	Yes	No
[16]	+	No	Yes
[21]	+	No	No
Proposed method	+	No	No

Note: +, ++, and +++ indicate the increasing computation burden.

To highlight the advantages of the proposed method, a comparison is conducted with existing capacitance estimation method of MMC. Reference [21] estimates the capacitance of SMs by calculating the sum of switch signals of one SM within the monitoring period. It offers advantages such as computational simplicity and absence of adverse effects on MMC.

In [21], the capacitance of the SM is calculated by (19).

$$
C_{\mathrm{au}i} = \frac{C_{\mathrm{rated}}}{500} \sum_{k=1}^{N_t} S_{\mathrm{au}ik} \tag{19}
$$

where C_{rated} is the reference value of SM capacitor ($C_{\mathrm{rated}} = 1$ p.u.); and N_t is the number of control cycles during a monitoring period, which has the same meaning as N_x. The two methods are compared under the same simulation conditions and the detailed simulation parameters are shown in Table II. The sum of $S_{\mathrm{au}i}$ for the first 10 SMs on the upper arm of phase a during five fundamental cycles are shown in Fig. 11, where $S_{\mathrm{au}5\text{-}10,\max}$ represents the largest error resulting in the sum of switching function in SM_5-SM_{10}, and $C_{\mathrm{rated}} = 10$ mF. Based on [21], in accordance with the reduction of $C_{\mathrm{au}i}$, the sum of $S_{\mathrm{au}i}$ decreases.

B. Comparison with State-of-the-art Methods

The proposed method can be embedded into the MMC valve control layer to estimate the capacitance of SM. The control core within the valve control layer generally employs high-performance field-programmable gate array (FPGA) chips. For one SM, each evaluation of capacitance requires two addition and two multiplication operations. In the simulation, the number of SMs per phase is 300. Considering the

According to the data from Fig. 11, the capacitance for different SMs can be calculated by (19). Based on the data of Table III, the capacitance estimation errors of the two methods are shown in Fig. 12. The simulation results show that the maximum estimation error of the existing method is 1.5%, whereas for the proposed method, the maximum estimation error is only 0.13%. In the context of high-voltage and large-capacity MMCs, metallized polypropylene film capacitors have extensive applicability which is highly required for accuracy [9]. The proposed method has a significant advantage for engineering applications.
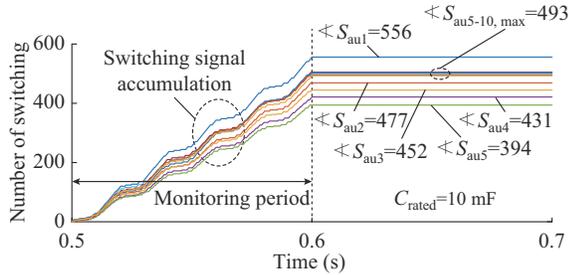

Fig. 11.   Sum of S_{aui} for the first 10 SMs.
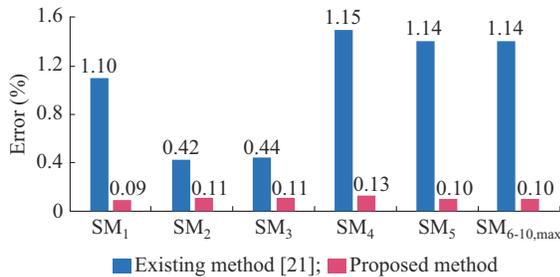

Fig. 12.   Capacitance estimation errors of two methods.

V. EXPERIMENTAL VERIFICATION

To further prove the effectiveness of the proposed method, the HIL test is also carried out based on RTDS. The control system is realized using the main control and valve control cabinets commonly utilized in the MMC project, enabling dual-loop control, modulation, and capacitor voltage balance. Considering the limitation of the processor, the maximum number of nodes allowed is 30, which imposes restrictions on the available channels for both digital and analog signals. Therefore, the HIL test system with 11-level MMC is constructed, and detailed parameters are shown in Table V.

TABLE V
PARAMETERS OF HIL TEST SYSTEM

Parameter	Value
Power rating (MW)	20
AC voltage (kV)	10
DC bus voltage (kV)	20
Number of SMs per arm	10
SM capacitance (mF)	7
Arm inductance (mH)	8
Control frequency (kHz)	10

The steady-state waveforms of the HIL test system is illustrated in Fig. 13, where the variables u_{abc}, i_{abc}, and i_{arm} maintain the same meanings as in the simulation. The HIL test results demonstrate the stable operation of the MMC system. The step of the HIL test system is 50 μs. Capacitances for SMs per arm are configured as: $C_1 = 5.6$ mF, $C_2 = 6.3$ mF, $C_3, C_4, ..., C_{10} = 7$ mF. To achieve a more accurate representation of actual project conditions, the sampling accuracy for the capacitor voltage and arm current is carefully configured to be ±0.5%. The capacitance estimation duration is set as two fundamental frequency cycles. The capacitor condition monitoring is started at 0.33 s. Due to the identical capacitance values of SM_3-SM_{10}, the analysis is limited to the monitoring results of the first five SMs.
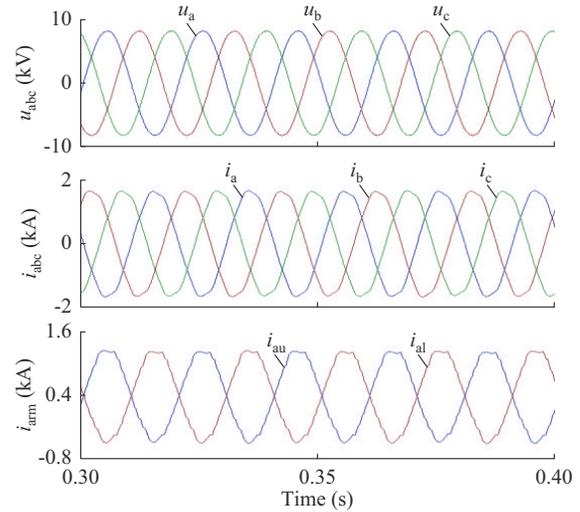

Fig. 13.   Steady-state waveforms of HIL test system.

The capacitance estimation results of the first 5 SMs on the upper arm of phase a are shown in Fig. 14, where C_3 is the data with the maximum errors in the capacitor condition monitoring results in SM_3-SM_5. The estimation errors for C_1, C_2, and C_3 are 1.7%, −1.3%, and 1.8%, respectively. The estimation errors exceed the requirements of the actual project.
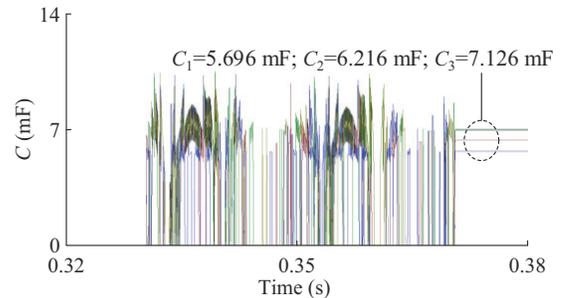

Fig. 14.   HIL test results of capacitance estimation.

As an example, the capacitance estimation process for SM_1 is illustrated in Fig. 15, revealing the relationship among the calculated result, the capacitor voltage, and the arm current. The error analysis in HIL test results shows some differences from the simulation results. In the HIL test system, the main circuit and control system of the MMC are

independent and simulated by different hardware units (i.e., RTDS). The communication speed between hardware units is uniform, indicating that the capacitor voltage, arm current, and switching states of SMs are synchronized. Thus, there are no spikes in experimental results. The main source of the errors in the HIL test system is associated with the measurement values at the zero-crossing points of the arm current and the accuracy of capacitor voltage and arm current sampling. Based on Fig. 6 and Fig. 14, the new capacitance estimation results are obtained, as shown in Table VI with the inverter under rated power of 1.0 p.u.. The errors of C_1, C_2, C_3 are 0.36%, −0.32%, −0.29%, respectively.

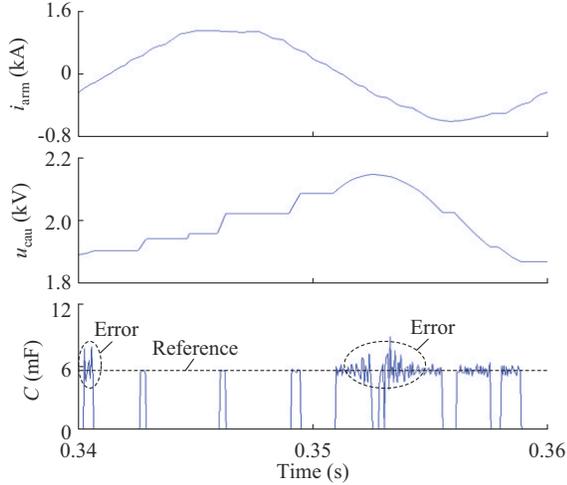
Fig. 15.   Error analysis of capacitance estimation in HIL test system.

TABLE VI
CAPACITANCE ESTIMATION RESULTS UNDER DIFFERENT OPERATION MODES

Mode	Estimated capacitance (mF)			Error (%)		
	SM$_1$	SM$_2$	SM$_3$	SM$_1$	SM$_2$	SM$_3$
Inverter (1.0 p.u.)	5.62	6.28	6.98	0.36	−0.32	−0.29
Inverter (0.8 p.u.)	5.62	6.33	6.99	0.36	0.47	−0.14
Inverter (0.6 p.u.)	5.61	6.32	6.99	0.18	0.32	−0.14
Rectifier (1.0 p.u.)	5.63	6.33	6.97	0.53	0.47	−0.43

To analyze the influence of different operation conditions on the capacitance estimation method, the MMC system is configured with new operation parameters and conditions in the HIL test system. To modify the power transmission of the MMC system, the transmission power is adjusted to 80% and 60% of the rated power, respectively. Besides, the operation mode is changed from inversion to rectification under the rated power of the MMC. The capacitance estimation results and errors under different operation conditions are presented in Table VI. The references for the capacitance of SM$_1$, SM$_2$, and SM$_3$ are 5.60 mF, 6.30 mF, and 7.00 mF, respectively. The results indicate that the estimation errors under different operation conditions are below 1%, validating the robustness of the proposed capacitor condition monitoring method when subjected to varying working conditions.

In summary, the proposed SM capacitor condition monitoring method offers several notable advantages in the context of hardware implementation and data acquisition. Based on the MMC valve control system, all variables required for the capacitance estimation can be acquired without additional hardware. Furthermore, the method demonstrates a low computation burden, rendering it an efficient and practical solution to online SM capacitor condition monitoring in MMC systems.

VI. CONCLUSION

In this paper, an improved SM capacitor condition monitoring method for MMCs considering switching states is proposed. The main conclusions of the proposed method can be summarized as follows.

1) The SM capacitor aging of MMC has been investigated, which shows that the structure and operation characteristics of MMC are the reasons behind the significant differences in the aging of capacitors among SMs per arm. It is also important to monitor capacitors in a timely manner for a highly reliable MMC.

2) An improved SM capacitor condition monitoring method based on the hundred-microsecond switching state is proposed. Compared with the existing methods, the advantages of the proposed method include higher calculation accuracy, and no effect on the operation performance of MMC.

3) The simulation results indicate that, compared with the existing method, the proposed method achieves a significant reduction in the maximum estimation error, which is from 1.5% to 0.13%. The HIL test results show that the estimation errors of the proposed method under different operation modes are below 1%, validating the robustness of the proposed method.

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