An Improved Modulation Strategy for Single-phase Three-level Neutral-point-clamped Converter in Critical Conduction Mode

Ning Li, Yujie Cao, Xiaokang Liu, Yan Zhang, Ruotong Wang, Lin Jiang, and Xiao-Ping Zhang

***Abstract*—Two-level totem-pole power factor correction (PFC) converters in critical conduction mode (CRM) suffer from the wide regulation range of switching frequency. Besides, in high-frequency applications, the number of switching times increases, resulting in significant switching losses. To solve these issues, this paper proposes an improved modulation strategy for the single-phase three-level neutral-point-clamped (NPC) converter in CRM with PFC. By optimizing the discharging strategy and switching state sequence, the switching frequency and its variation range have been efficiently reduced. The detailed performance analysis is also presented regarding the switching frequency, the average switching times, and the effect of voltage gain. A 2 kW prototype is built to verify the effectiveness of the proposed modulation strategy and analysis results. Compared with the totem-pole PFC converter, the switching frequency regulation range of the three-level PFC converter is reduced by 36%, and the average switching times is reduced by 45%. The experimental result also shows a 1.2% higher efficiency for the three-level PFC converter in the full load range.**

***Index Terms*—Critical conduction mode (CRM), on-board charger, switching frequency range, switching times, power factor correction (PFC), three-level converter.**

I. Introduction

With the great depletion crisis of fossil fuel energy sources in the world, electric vehicles (EVs) play an increasingly crucial role in sustainable transportation systems. With the rapid expansion of the global EV market, more stringent requirements for the efficiency, power density, and reliability of the high-voltage (200-450 V) battery storage and its pertinent on-board charger (OBC) system have been put forward [1], [2]. The OBC system commonly includes a front-end AC-DC converter with power factor correction (PFC) and an isolated DC-DC converter with current regulation that provides the DC voltage required by the battery. The proper topology selection and optimal control strategy design of the front-end PFC converter have attracted significant research attention [3]-[7].

The front-end PFC converter has several operating modes according to the inductor current waveform on the AC side, encompassing the continuous conduction mode (CCM), the discontinuous conduction mode (DCM), and the critical conduction mode (CRM) [8]-[14]. Converters operating in CRM have the advantages of high power factor (PF) and simple control strategy design. Besides, the constant on-time (COT) scheme commonly used in CRM enables the easy realization of unity PF for the converter. However, this scheme has a widely varied switching frequency that affects the system efficiency [9], [15]-[17].

In high-power EV applications, the switching losses are commonly reduced by using bridgeless and totem-pole PFC converters. For the totem-pole PFC converter in CRM, two power switches in one-phase bridge commutate at the line frequency to minimize the switching losses, and the other two switches operate under COT control. However, this also causes a wide-band switching frequency.

To reduce the switching frequency range, the improvements have been made in terms of converter topology and/or control strategy. In [18], a boost PFC converter operating in CRM with a constant switching frequency is implemented based on a variable on-time control, but the unity PF is not obtained. In [19], a hybrid conduction mode (HCM) with fixed frequency is proposed. But for the two aforementioned methods, the unity PF was not obtained. In [20], an improved modulation strategy with variable on-time was proposed for a three-phase single-switch boost rectifier operating in CRM. The switching frequency is constant and a high PF is obtained, but the use of diode rectifier bridge increases the switching loss. Focusing on the interleaved totem-pole

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PFC converter in CRM, the control scheme in [21] improves the input current distortion and reduces the high switching frequency around the grid voltage zero-crossing. However, the reduction range of switching frequency is unclear. Besides, for a two-level totem-pole PFC converter with traditional COT control, the switching frequency variation per switch will not be changed in the line frequency cycle.

Compared with two-level topologies, the multi-level topologies with increased number of switches and passive devices can effectively reduce the total harmonic distortion (THD) of input current [22], [23]. Among them, three-level PFC converters are commonly used in medium- and high-power OBC systems operating in CCM. However, in CCM, power switches cannot naturally achieve zero-current switching, hence increasing system losses. Conversely, the PFC converters in CRM can naturally realize soft switching. Therefore, it is necessary to investigate suitable CRM alternatives for controlling three-level PFC converters. In [24]-[26], the improved three-level topologies and control strategies are proposed to reduce the THD and improve the efficiency. However, some improved topologies based on the boost converter are not simple enough. For the EV application, the simplicity and reliability are necessary. Meanwhile, in [27], a CRM for the three-level boost PFC converter is proposed to reduce the switching frequency and peak input current, yet the unity PF is not achieved.

To solve the aforementioned issues, this paper proposes an improved modulation strategy for the single-phase three-level NPC converter in CRM with PFC to reduce the switching frequency and its variation range as well as the average switching times of each power switch. To this end, first, the COT control is used to maintain the unity PF of the three-level PFC converter, overcoming the high THD issue of [18]. Then, the wide variation range of switching frequency caused by the COT control is reduced by optimizing the discharging strategy and switching state sequence. The advantages of the proposed modulation strategy are summarized as follows.

1) When the input voltage is close to the peak value of two capacitors connected in series during discharging, the frequency of inductor current ripple and the average switching frequency per switch are consistent with the conventional two-level topology. When the input voltage is less than half the output voltage, one output capacitor is connected to the circuit. Compared with the two-level topology, the inductor has a longer discharging time interval, thereby reducing the average switching frequency.

2) The calculation complexity of space vector pulse width modulation (SVPWM) strategy can be further simplified [25] when the converter is working in CRM, owing to the COT interval. By optimizing the switching state sequence, the average switching times of each switch can be further reduced, which lowers the switching losses and improves the system efficiency. Besides, using proper balance control strategies for the three-level PFC converter [28], [29], the voltage imbalance of cascaded capacitors can be avoided.

The rest of this paper is organized as follows. In Section II, the principle and issue of wideband switching frequency range for totem-pole PFC converters with COT control are discussed. In Section III, the operation principle and modulation strategy are proposed for the three-level PFC converter, with the aim to reduce the average switching frequency per switch and narrow its regulation range. Section IV comprehensively compares the performances of the totem-pole PFC converter with COT control and three-level PFC converter with the proposed modulation strategy, based on the theoretical analysis. In Section V, experiment results are used to verify the advantages of the proposed modulation strategy and effectiveness of the theoretical analysis. Finally, Section VI draws conclusion remarks.

II. Totem-pole PFC Converter with COT Control

The totem-pole PFC converter is widely used in the OBC system due to its simple structure, low switching loss, and high efficiency. With the COT control, the on-time interval of a switch is constant in a switching cycle, and the off-time interval is determined by the falling slope of inductor current i_L. With reference to Fig. 1 [30]-[32], when i_L decreases to zero, the RS flip-flop sets Q to be 1. The output voltage V_o is detected and compared versus the reference V_{ref}. The error V_{ea} and the sawtooth wave V_{ramp} are compared to reset the RS flip-flop.

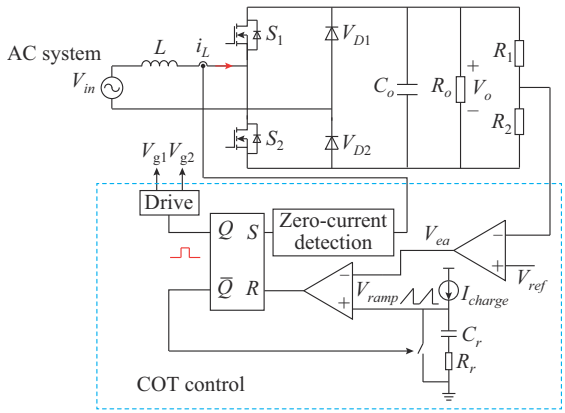

Fig. 1. Simplified COT control diagram for a totem-pole PFC converter.

With the traditional COT control, the peak inductor current is related to the on-time value of each switching cycle T_{on} as:

$$I_{L,pk}(\theta)=\frac{\sqrt{2}\,V_{in,rms}\sin\theta}{L}T_{on} \tag{1}$$

where $I_{L,pk}(\theta)$ is the instantaneous value of peak inductor current in the half line frequency; $\theta=\omega t$, and ω is the angular frequency; $V_{in,rms}$ is the root-mean-square value of input voltage V_{in}; and L is the inductance.

The average input current $I_{in,av}(\theta)$ can be derived from (1) as:

$$I_{in,av}(\theta)=\frac{1}{2}I_{L,pk}(\theta) \tag{2}$$

Assume $t_{off}(\theta)$ to be the instantaneous off-time value of the switching cycle, and then T_{on} and $t_{off}(\theta)$ are related as:

$$\frac{\sqrt{2}\,V_{in,rms}\sin\theta}{L}T_{on}=\frac{V_o-\sqrt{2}\,V_{in,rms}\sin\theta}{L}t_{off}(\theta) \tag{3}$$

The input power of the totem-pole PFC converter P_{in} can be expressed as:

$$P_{in}=\frac{2}{\pi}\int_0^{\frac{\pi}{2}}\sqrt{2}\,V_{in,rms}I_{in,av}(\theta)\sin\theta\mathrm{d}\theta \tag{4}$$

Combining (2)-(4), T_{on} can be derived as [33]:

$$T_{on}=\frac{2LP_o}{\eta V_{in,rms}^2} \tag{5}$$

where P_o is the output power of the totem-pole PFC converter; and η is the converter efficiency.

The instantaneous switching frequency is reflected by the frequency of inductor ripple current $f_{ripple}(\theta)$, which yields:

$$f_{ripple}(\theta)=\frac{1}{T_{on}+t_{off}(\theta)} \tag{6}$$

$t_{off}(\theta)$ can be expressed by T_{on} based on volt-second balance. Substituting (3) and (5) into (6), $f_{ripple}(\theta)$ can be expressed as:

$$f_{ripple}(\theta)=\frac{(V_o-\sqrt{2}\,V_{in,rms}\sin\theta)\eta V_{in,rms}^2}{2LP_oV_o} \tag{7}$$

From (7), $f_{ripple}(\theta)$ is determined by $V_{in,rms}$, V_o, L, and P_o. In the practical OBC application, L is constant, $V_{in,rms}$ is 110 V or 220 V, and V_o and P_o are independent variables. Define the voltage gain G as:

$$G=\frac{V_o}{\sqrt{2}\,V_{in,rms}} \tag{8}$$

$f_{ripple}(\theta)$ can be rewritten as:

$$f_{ripple}(\theta)=\frac{\eta V_{in,rms}^2}{2LP_oV_o}\left(1-\frac{\sin\theta}{G}\right) \tag{9}$$

It is observed that $f_{ripple}(\theta)$ is only dependent on G given the operation condition of $V_{in,rms}$, L, and P_o. These parameters define the base value of $f_{ripple}(\theta)$ as:

$$f_{ripple,base}=\frac{\eta V_{in,rms}^2}{2LP_oV_o} \tag{10}$$

Accordingly, $f_{ripple}(\theta)$ can be normalized as:

$$f_{ripple}^*(\theta)=\frac{f_{ripple}(\theta)}{f_{ripple,base}}=1-\frac{\sin\theta}{G} \tag{11}$$

Figure 2 shows the variation curves of $f_{ripple}^*(\theta)$ with different voltage gains G, where $f_{ripple,\min}^*$ is the minimum value of f_{ripple}^*. When G increases, the variation range of $f_{ripple}^*(\theta)$ becomes smaller, and vice versa. For instance, when $G=1.5$, $f_{ripple}^*(\theta)$ ranges from 0.33 to 1. In the OBC application with the input voltage of 110 V or 220 V and the output voltage determined by the battery type (usually 400 V), G is small, and the traditional COT control will cause a wide range of $f_{ripple}(\theta)$, which is unacceptable.

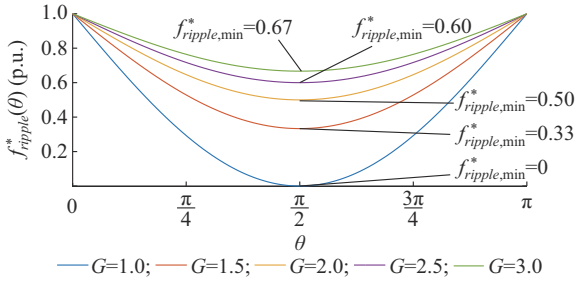

Fig. 2. Variation curves of $f_{ripple}^*(\theta)$ with different G.

III. Three-level PFC Converter with Proposed Modulation Strategy

To lower the switching frequency and minimize the variation range of the switch, the three-level PFC converter is implemented for the OBC system, and its modulation strategy is developed in this section.

A. Operation Principle

With reference to Fig. 3, the implemented three-level PFC converter has four power switches in each bridge arm. Switches S_{11}, S_{12}, S_{13}, and S_{14} form the bridge arm S_1, and S_{21}, S_{22}, S_{23}, and S_{24} form the bridge arm S_2. C_1 and C_2 are DC-side voltage stabilizing capacitors, and o is the midpoint. For simplicity, C_1 and C_2 are assumed to have the same capacitance and voltage values.

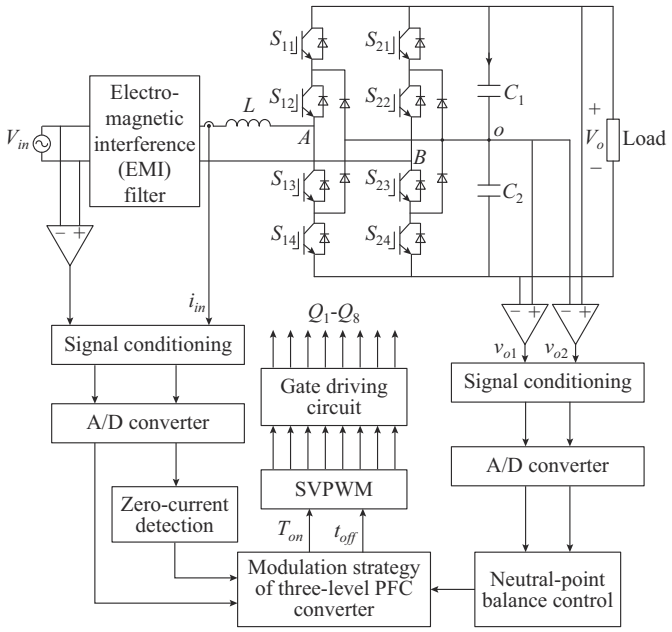

Fig. 3. Block diagram of implemented three-level PFC converter.

There are three switching states, i. e., P, O, and N, for each bridge arm. For the bridge arm S_1, when S_{11} and S_{12} are ON, and S_{13} and S_{14} are OFF, the switching state is P; when S_{12} and S_{13} are ON, and S_{11} and S_{14} are OFF, the state is O; when S_{13} and S_{14} are ON, and S_{11} and S_{12} are OFF, the state is N. Considering the two bridge arms, there are nine combinations of switching states [34], [35]. Accordingly, six current flow modes 1-6 can be identified in a half line frequency cycle (see Fig. 4 for the example when $V_{in}>0$).

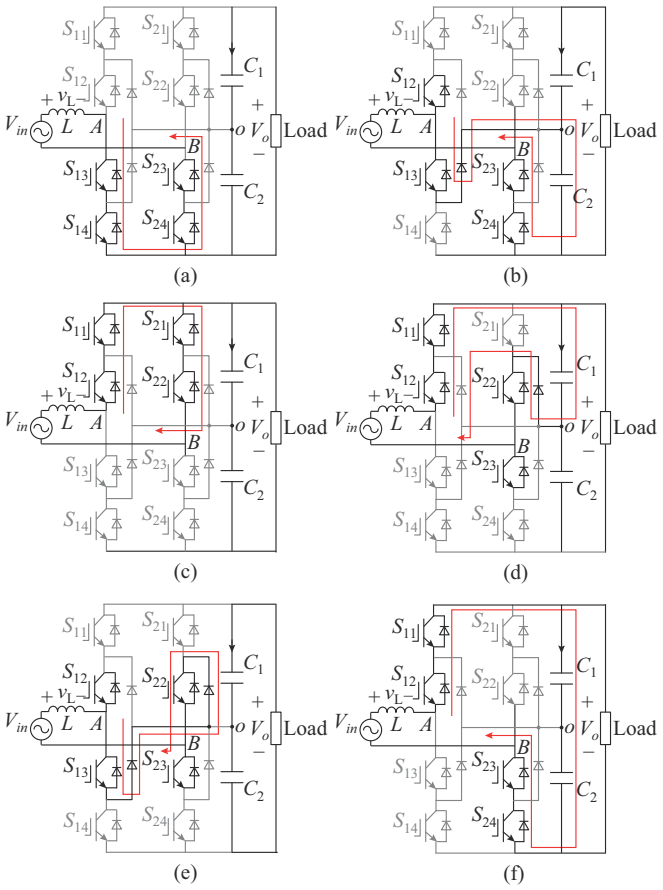

Fig. 4. Six current flow modes when $V_{in}>0$. (a) Mode 1: $U_{AB}=0$, $S_1=N$, and $S_2=N$. (b) Mode 2: $U_{AB}=V_o/2$, $S_1=O$, and $S_1=N$. (c) Mode 3: $U_{AB}=0$, $S_1=P$, and $S_2=P$. (d) Mode 4: $U_{AB}=V_o/2$, $S_1=P$, and $S_2=O$. (e) Mode 5: $U_{AB}=0$, $S_1=O$, and $S_2=O$. (f) Mode 6: $U_{AB}=V_o$, $S_1=P$, and $S_2=N$.

As observed in Fig. 4, in modes 1, 3, and 5, the inductor L is charged, which is consistent with the totem-pole PFC converter, and the charging time T_{on} is constant. In modes 2, 4, and 6, L is discharged with different discharging time t_{off}. In modes 2 and 4, C_1 or C_2 is used to discharge L. The neutral point potential is clamped by control strategy of the three-level PFC converter, and voltages of C_1 and C_2 are considered identical to $V_o/2$. Accordingly, modes 2 and 4 can only operate when $V_{in}<V_o/2$. However, in mode 6, C_1 and C_2 are used as series capacitors to discharge L with full range of V_{in}. Due to the transitions between modes, the switching frequency of each switch will change and the regulation range of the switching frequency will be affected.

In modes 1, 3, and 5, T_{on} is expressed by (1). In mode 6, the discharging time $t_{off,1}$ is determined by V_{in} and V_o; and in modes 2 and 4, the discharging time $t_{off,2}$ is determined by V_{in} and $V_o/2$.

$$t_{off,1}=\frac{2\sqrt{2}\,LP_o}{\eta V_{in,rms}(V_o-\sqrt{2}\,V_{in,rms})} \tag{12}$$

$$t_{off,2}=\frac{4\sqrt{2}\,LP_o}{\eta V_{in,rms}(V_o-2\sqrt{2}\,V_{in,rms})} \tag{13}$$

From (6), it can be observed that when t_{off} varies, the frequency of inductor ripple current will change. Hence, the switching frequency regulation range and average switching times of each switch can be reduced, if the switching sequence is optimized by properly combining the nine switching states of the three-level PFC converter.

The fundamental control principles of three-level PFC converter are as follows.

1) When $V_o/2<V_{in}<V_o$, C_1 and C_2 are used to discharge L. The inductor current I_L and pulse width modulation (PWM) pulses of S_{11}, S_{12}, S_{13}, and S_{14} are shown in Fig. 5(a) where the symbols such as PP and PN represent combinations of switching states in two bridge arm, and T_1 to T_5 represent a full cycle during which the inductor L undergoes charging and discharging phases. There are a total of 12 switching actions (marked by SW in Fig. 5(a)) during [t_0, t_6], and each switch commutates once in a cycle.

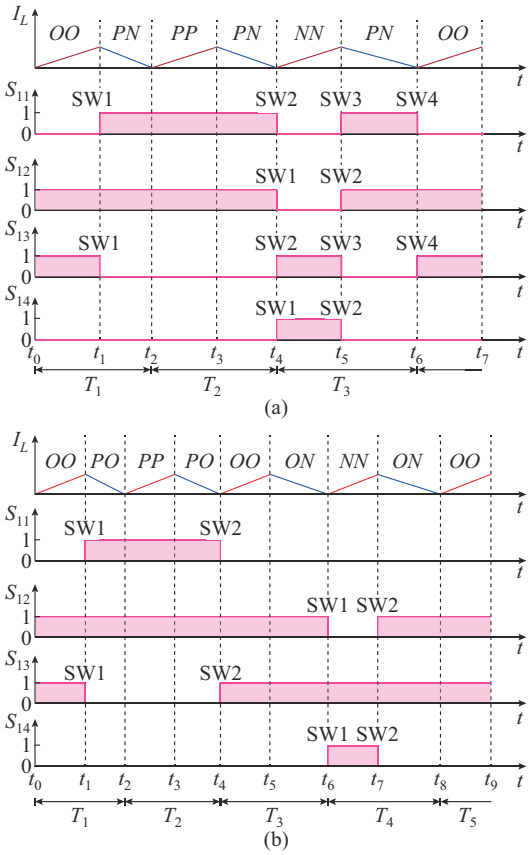

Fig. 5. Inductor current and PWM pulses of S_{11}, S_{12}, S_{13}, and S_{14}. (a) $V_o/2<V_{in}<V_o$. (b) $0<V_{in}<V_o/2$.

2) When $0<V_{in}<V_o/2$, C_1 or C_2 is used to discharge L. The inductor current I_L and PWM pulses of S_{11}, S_{12}, S_{13}, and S_{14} are shown in Fig. 5(b). At this time, there are a total of 8 switching actions during [t_0, t_8], and each switch commutates 0.5 times on average in a cycle.

It should be noted that OO, PP, and NN have the same effects as zero vectors. However, in order to reduce the number of switching actions and the issue of neutral point potential balance, three zero vectors are used alternately. Based on this, the average switching frequency of the converter can be analyzed. When $0<V_{in}<V_o/2$, for a boost PFC converter, a switch operates twice in one switching cycle, and its switching frequency is equal to the frequency of inductor ripple current; for the three-level PFC converter whose switches op-

erate 0.5 times on average in a cycle, the average switching frequency is 0.25 times the frequency of inductor ripple current. Similarly, when $V_o/2 < V_{in} < V_o$, the average switching frequency of the three-level PFC converter is 0.5 times the frequency of inductor ripple current.

B. Proposed SVPWM Strategy

The SVPWM strategy is usually used for three-phase three-level rectifiers due to its high utilization rate of DC-side voltage. In this paper, a single-phase SVPWM strategy, which reduces complexity of the modulation process, is proposed for the three-level PFC converter in CRM.

The space voltage vector diagram of the three-level PFC converter is shown in Fig. 6 [36]-[38]. The space is divided into four sections, which are separated by large vectors (*PN* and *NP*), small vectors (*PO*, *ON*, *NO*, and *OP*), and zero vectors (*PP*, *OO*, and *NN*). Two voltage vectors of a section are selected for synthesis of the reference voltage vector $\boldsymbol{V}$, which rotates counterclockwise at angular frequency ω, and the input voltage vector $\boldsymbol{V}_{in}$ is equal to the projection of $\boldsymbol{V}$ on the α-axis. When $\boldsymbol{V}$ is located on quadrants 1 and 2, $\mathrm{Re}(\boldsymbol{V}_{in}) > 0$; otherwise, $\mathrm{Re}(\boldsymbol{V}_{in}) < 0$.

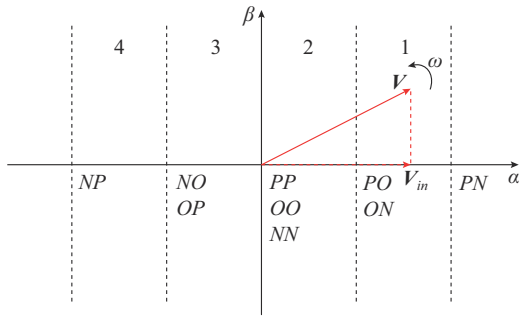

Fig. 6. Space vector diagram of three-level PFC converter.

Assume $\boldsymbol{V}$ is synthesized by vectors $\boldsymbol{V}_1$ and $\boldsymbol{V}_2$ (with operating time T_1 and T_2, respectively). Accordingly, their relationship in the entire vector space can be derived, as shown in Table I. In this strategy, the switching vector $\boldsymbol{V}_1$ has a constant operating time T_{on}; $\boldsymbol{V}_2$ has an operating time determined by voltage signals to simplify the modulation.

TABLE I
RELATIONSHIP IN ENTIRE VECTOR SPACE

Section	$\boldsymbol{V}_1$	T_1	$\boldsymbol{V}_2$	T_2
1	*PP*, *OO*, *NN*	T_{on}	*PN*	$\frac{V_{in}}{V_o - V_{in}} T_{on}$
2			*PO*, *ON*	$\frac{2\lvert V_{in}\rvert}{V_o - 2\lvert V_{in}\rvert} T_{on}$
3			*NO*, *OP*	$\frac{2\lvert V_{in}\rvert}{V_o - 2\lvert V_{in}\rvert} T_{on}$
4			*NP*	$\frac{V_{in}}{V_o - V_{in}} T_{on}$

When the converter works in CRM, the charging and discharging time of inductor current is predetermined, and thus, the operating time of the zero vector and other vectors in Fig. 6 is predetermined. In this case, the average switching times can be reduced by considering the sequence of vector actions.

IV. PERFORMANCE ANALYSIS AND COMPARISON

A. Average Switching Frequency and Variation Range

Based on the analysis in Section II, for the totem-pole PFC converter, only one switch operates in half line frequency cycle. Hence, the average switching frequency of each switch $f_{s,totem,pole}(\theta)$ is half the frequency of the inductor ripple current $f_{ripple}(\theta)$:

$$f_{s,totem,pole}(\theta) = \frac{\eta V_{in,rms}^2}{4LP_o}\left(1 - \frac{\sin\theta}{G}\right) \tag{14}$$

Let the reference value of the switching frequency be $f_{s,ref} = \eta V_{in,rms}^2/(4LP_o)$, then $f_{s,totem,pole}(\theta)$ is normalized as:

$$f_{s,toem,pole}^*(\theta) = 1 - \frac{\sin\theta}{G} \tag{15}$$

For the three-level PFC converter, when two output capacitors C_1 and C_2 are connected in series to the main circuit, the average switching frequency of each switch $f_{s,three,level}(\theta)$ is the same as that of the totem-pole PFC converter; when only one capacitor is connected, the average switching frequency reduces to half of the maximum switching frequency. Hence, by denoting the switching angle as α, we have:

$$f_{s,three,level}(\theta) = \begin{cases} \dfrac{\eta V_{in,rms}^2}{4LP_o}\left(1 - \dfrac{\sin\theta}{G}\right) & \alpha \le \theta \le \pi - \alpha \\ \dfrac{\eta V_{in,rms}^2}{8LP_o}\left(1 - \dfrac{2\sin\theta}{G}\right) & \text{otherwise} \end{cases} \tag{16}$$

$$f_{s,three,level}^*(\theta) = \begin{cases} 1 - \dfrac{\sin\theta}{G} & \alpha \le \theta \le \pi - \alpha \\ 0.5 - \dfrac{\sin\theta}{G} & \text{otherwise} \end{cases} \tag{17}$$

The variation values of the average switching frequency are compared between the two converters. For the totem-pole PFC converter, this value and its normalized value are:

$$\Delta f_{s,totem,pole} = \frac{\eta V_{in,rms}^2}{4LP_o}\frac{1}{G} \tag{18}$$

$$\Delta f_{s,totem,pole}^* = \frac{1}{G} \tag{19}$$

For the three-level PFC converter, the variation value of average switching frequency is affected by α. With reference to Fig. 7, when $\alpha_{\min} \le \alpha \le \alpha_{\max}$, its normalized variation value is 0.5 p.u. (in this case, $G = 1.5$, $\alpha_{\min} = 0.253$, and $\alpha_{\max} = 0.848$), where $f_{s,\min}^*$ and $f_{s,\max}^*$ are the minimum and the maximum values of $f_{s,three,level}^*(\theta)$, respectively. Here, $\alpha_{\max}$ is the grid angle when V_{in} is equal to $V_o/2$. However, when $\alpha < \alpha_{\min}$, the variation value will be larger. Thus, the variation value of average switching frequency can be minimized only when α is suitably chosen. Specifically, $\alpha_{\min}$ and $\alpha_{\max}$ should satisfy:

$$f_{s,three,level}^*(\alpha) = f_{s,three,level}^*(\pi/2) \tag{20}$$

$$f_{s,three,level}^*(\theta) = 0 \tag{21}$$

The solutions of (20) and (21) are:

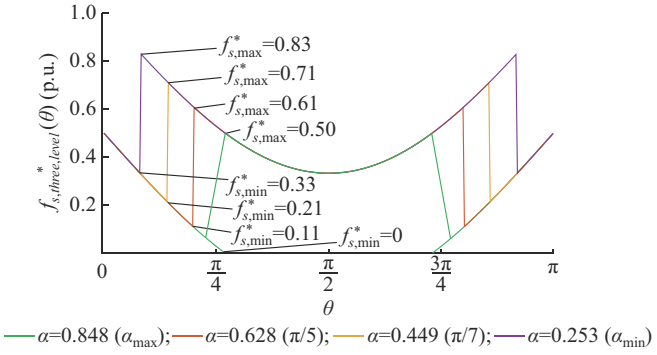

Fig. 7. Average switching frequency curves of three-level PFC converter with different α.

$$\begin{cases} \alpha_{\min} = \arcsin\left(\dfrac{2-G}{2}\right) \\ \alpha_{\max} = \arcsin\left(\dfrac{G}{2}\right) \end{cases} \tag{22}$$

When α is within the range specified by (22), the variation value and its normalized value of the average switching frequency can be expressed as:

$$\Delta f_{s,three,level} = \frac{\eta V_{in,rms}^2}{8LP_o} \tag{23}$$

$$\Delta f^*_{s,three,level} = 0.5 \tag{24}$$

From (19) and (24), when the three-level PFC converter is adopted instead of the totem-pole one, the variation value of average switching frequency ($\sqrt{2}V_{in,rms} > V_o/2$, and $1 < G < 2$) is reduced by:

$$\Delta f_s^* = \Delta f^*_{s,totem,pole} - \Delta f^*_{s,three,level} = \frac{2-G}{2G} \tag{25}$$

The reduction percentage can be expressed as:

$$\Delta f^*_{s,per} = \frac{\Delta f_s^*}{\Delta f^*_{s,totem,pole}} \times 100\% \tag{26}$$

B. Effect of Voltage Gain

The voltage gain G has a twofold effect on the performance of proposed modulation strategy. On one side, it affects the reduction in variation value of the average switching frequency (see (25) and (26)); on the other side, the available range of α is also changed according to (22).

With different G, though $f^*_{s,three,level}$ is kept constant (see (24)), Δf_s^* is changed due to the change in $\Delta f^*_{s,totem,pole}$ (see (19)). As shown in Fig. 8, when G increases from 1.2 to 1.8, a lower reduction in Δf_s^* is observed, comparing the three-level PFC converter with the totem-pole PFC converter. Accordingly, the proposed modulation strategy can achieve better performance for a smaller G.

When G increases, α_{max} increases and α_{min} decreases, indicating a larger difference between α_{max} and α_{min}, as shown in Fig. 9. This gives greater design space for the switching frequency of the power devices in practical industrial applications.

Therefore, a larger Δf_s^* can be obtained at the expense of the range selection of α, and vice versa.

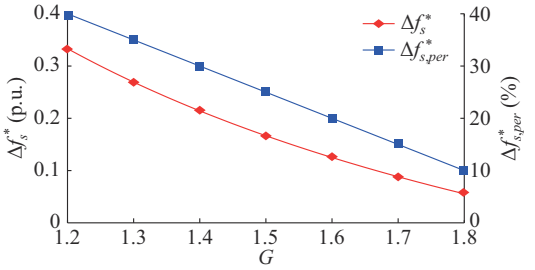

Fig. 8. Variation curves of Δf_s^* and $\Delta f^*_{s,per}$ with different G.

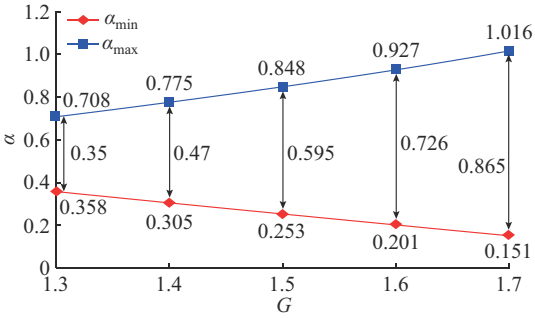

Fig. 9. Variation curves of α_{min} and α_{max} with different G.

C. Average Switching Times of Each Switch

The average switching times of each switch can be obtained by integrating the switching frequency in the pertinent interval. By combining (15) and (17), the average switching times of the three-level PFC converter is lower than that of the totem-pole one, i.e.,

$$\Delta N_t = \frac{\int_0^{\pi} f^*_{s,totem,pole}(\theta)\mathrm{d}\theta - \int_0^{\pi} f^*_{s,three,level}(\theta)\mathrm{d}\theta}{\int_0^{\pi} f^*_{s,totem,pole}(\theta)\mathrm{d}\theta} \tag{27}$$

With the variation of α, the average switching times of the three-level PFC converter change. The relationship between ΔN_t and α when $G = 1.5$ is shown in Table II. With lower α, ΔN_t also decreases. However, even in the worst case ($\alpha = \alpha_{min}$), it holds that $\Delta N_t > 0$. Hence, compared with the totem-pole PFC converter, the three-level PFC converter has a lower number of average switching times for each switch, which reduces the switching loss and improves the converter efficiency.

TABLE II
RELATIONSHIP BETWEEN ΔN_t AND α WHEN $G = 1.5$

α	ΔN_t (%)	α	ΔN_t (%)
0.848 (α_{max})	46.9	0.449 (π/7)	24.8
0.628 (π/5)	34.7	0.253 (α_{min})	14.0

V. EXPERIMENTAL VERIFICATION

In this work, a 2 kW experimental platform, as shown in Fig. 10, is used to verify the effectiveness of the proposed modulation strategy and analysis for the three-level PFC converter. For the totem-pole PFC converter, TI TMS320F28377 is used to control the circuit, and the N-channel MOSFETs IPW65R080CFD are chosen as the power switches. For the

three-level PFC converter, TI TMS320F28377 is used to control the circuit, and the *N*-channel MOSFETs Infineon IPP410N30N are used as the power switches. The key parameters of the main circuit for the three-level PFC converter are collected in Table III. The measurement results for the two converters are shown in Fig. 11. Based on the system parameters, $G=1.29$; then the optimal range of α can be obtained as $[\alpha_{\min}=0.365,\ \alpha_{\max}=0.698]$.

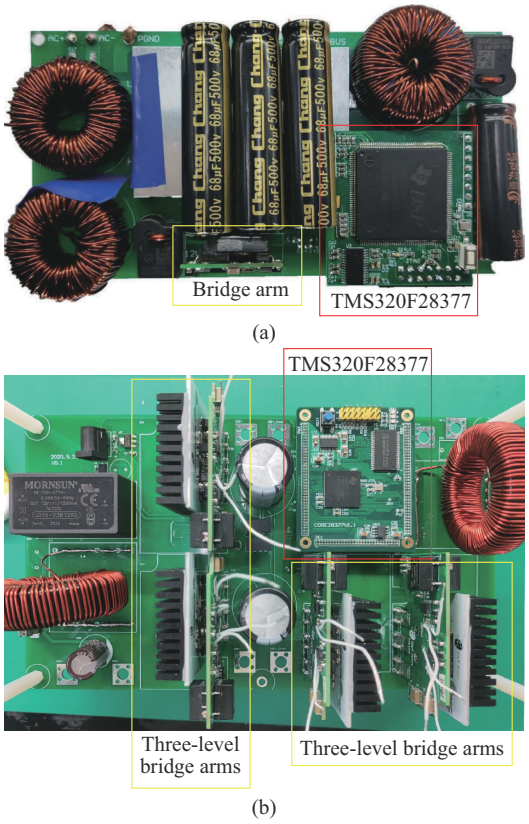

Fig. 10. Experimental platform. (a) Totem-pole PFC converter. (b) Three-level PFC converter.

TABLE III
KEY PARAMETERS OF MAIN CIRCUIT FOR THREE-LEVEL PFC CONVERTER

Parameter	Value	Parameter	Value
$V_{in,rms}$	220 V	P_o	2000 W
$\Delta f_{s,three,level}$	59.91 kHz	L	50 μH
V_o	400 V	C_1, C_2	2200 μF
I_o	5 A	R	80 Ω
Voltage of MOSFET V_{DS}	650 V	Current of MOSFET I_{DS}	30 A

As a first observation, when the three-level and the totem-pole PFC converters work in CRM, the unity PF is always obtained, as shown in the input voltage and current waveforms in Fig. 11(a) and (b). Here, a low-pass LC filter (with L of 230 μH and C of 220 nF) is used to obtain the average currents. Besides, the harmonic analysis has been used to measure the input current harmonics, as shown in Fig. 12. Despite a slightly increase in THD w.r.t. the totem-pole PFC converter, the proposed modulation strategy is proven to conform to IEC 61000-3-2 Class D, which is the harmonic standard for the EV charging device. The higher harmonic content can be ascribed to the hard switching in the switching process and can be mitigated by using switching frequency detection and comparison units, and achieving soft switching control.

To compute and compare the average switching frequency and the number of switching commutations for the two converters, the current waveforms of switches are observed. For simplicity, when $0<V_{in}<V_o/2$, the switching vectors *NN* and *ON* synthesize the voltage; when $V_o/2<V_{in}<V_o$, the switching vectors *NN* and *PN* synthesize the voltage. At this time, the relationship between the inductor current and the switch states can be found in Fig. 13. Currents flowing through switches are measured for two cases, i.e., $\theta=\pi/2$ and $\theta=\pi/6$, as shown in Fig.11(c)-(f). In both cases, $\alpha=0.698$.

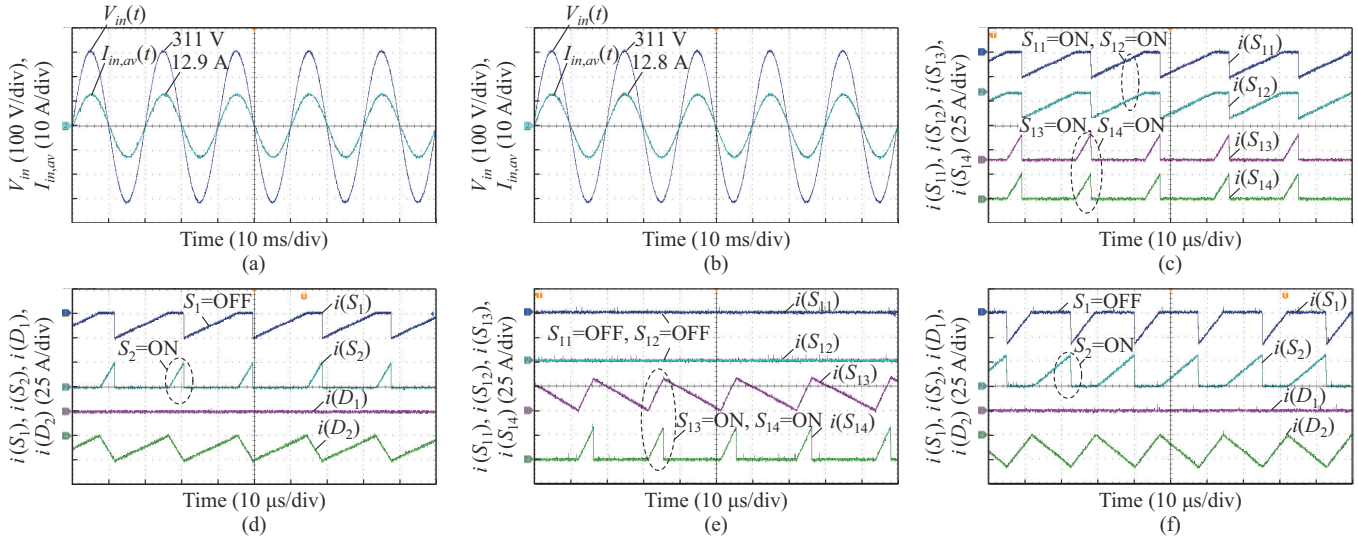

Fig. 11. Measurement results. (a) Input voltage and current of three-level PFC converters. (b) Input voltage and current of totem-pole PFC converters. (c) Currents flowing through S_{11}, S_{12}, S_{13}, and S_{14} in three-level PFC converter when $\theta=\pi/2$. (d) Currents flowing through S_1, S_2, D_1, and D_2 in totem-pole PFC converter when $\theta=\pi/2$. (e) Currents flowing through S_{11}, S_{12}, S_{13}, and S_{14} in three-level PFC converter when $\theta=\pi/6$. (f) Currents flowing through S_1, S_2, D_1, and D_2 in totem-pole PFC converter when $\theta=\pi/6$.

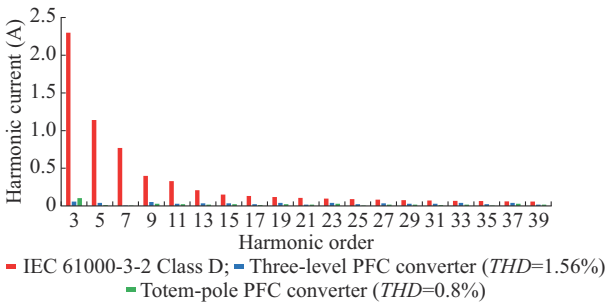

Fig. 12. Harmonic analysis of input current of three-level and totem-pole PFC converters.

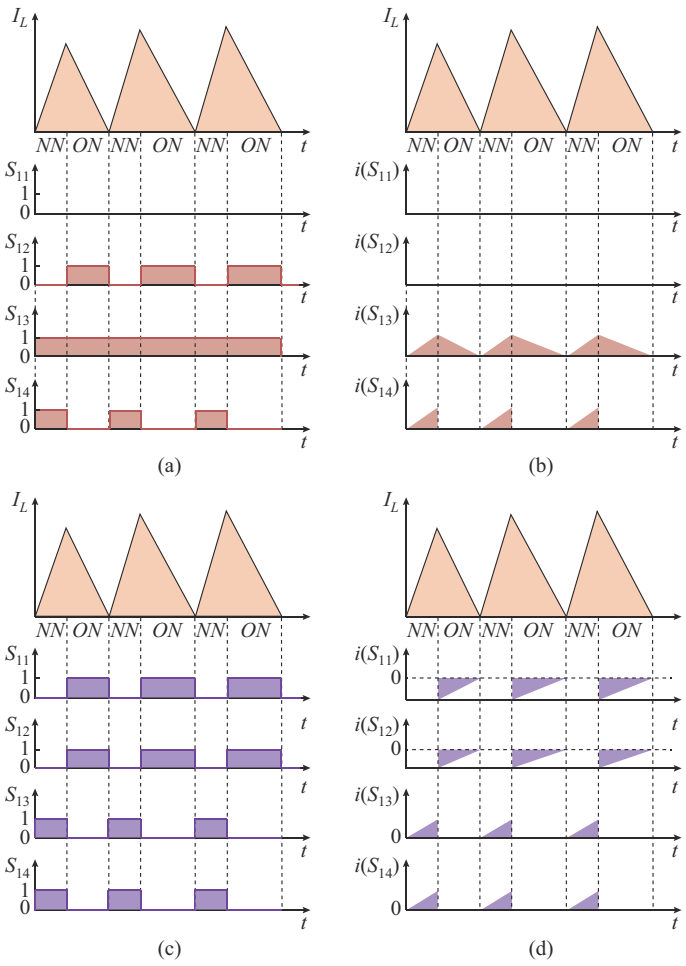

Fig. 13. Inductor current versus switch states. (a) Switch states when $0<V_{in}<V_o/2$. (b) Currents flowing through switches when $0<V_{in}<V_o/2$. (c) Switch states when $V_o/2<V_{in}<V_o$. (d) Currents flowing through switches when $V_o/2<V_{in}<V_o$.

When $\theta=\pi/2$, the switching frequencies of switches are 52.29 and 52.31 kHz for the three-level and the totem-pole PFC converters, respectively. Each switch commutates once on average in a cycle, both for the three-level topology with eight switches and the totem-pole topology with four switches. Hence, the average switching frequencies of each switch are 26.15 and 26.16 kHz for the three-level and the totem-pole PFC converters, respectively.

When $\theta=\pi/6$, the switching frequencies of switches are 53.44 and 141.68 kHz for the three-level and totem-pole PFC converters, respectively. For the three-level topology, each switch commutates 0.5 times on average in a cycle; for the totem-pole topology, each switch commutates once on average in a cycle. Hence, the average switching frequencies of each power switch are 13.36 and 70.84 kHz for the three-level and the totem-pole PFC converters, respectively.

Then, the average switching frequencies for the two converters are calculated and normalized with different θ values, as shown in Fig. 14. Theoretical values are taken for the three-level PFC converter when $\theta=\alpha$ and $\theta=\pi-\alpha$ ($\alpha=0.698$), due to the measurement difficulty in these cases. Based on the result, the variation ranges of average switching frequency can be obtained, and values of $\Delta f^*_{s,per}$ and ΔN_t are calculated by (26) and (27), respectively, as shown in Table IV. The three-level PFC converter is proven to have evident performance improvement, and the good agreement between the measurement and theoretical values validates the previous analysis.

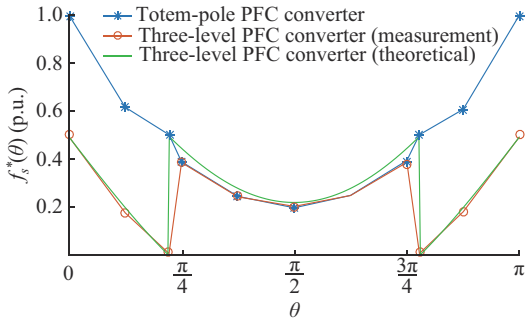

Fig. 14. Normalized values of average switching frequencies of totem-pole and three-level PFC converters.

TABLE IV
PERFORMANCE COMPARISON OF TWO CONVERTERS

Parameter	Theoretical value	Measurement value	Deviation (%)
$\Delta f^*_{s,totem,pole}$	0.778 p.u.	0.804 p.u.	3.29
$\Delta f^*_{s,three,level}$	0.5 p.u.	0.511 p.u.	2.15
$\Delta f^*_{s,pre}$	35.73%	36.48%	2.04
ΔN_t	44.00%	45.10%	2.44

Besides, different values of α are selected for the same voltage gain G to compare the switching losses of three-level PFC converter under the full load condition, as shown in Table V. The inductor current waveforms under different α when $G=1.29$ are shown in Fig. 15. In this case, the three-level PFC converter has a slightly higher switching loss when $\alpha=\pi/6$. Indeed, when α is smaller, the three-level PFC converter has increased switching times, and thus higher switching loss.

TABLE V
SWITCHING LOSSES OF THREE-LEVEL PFC CONVERTER

α	Switching loss (W)			
	On-state	Turn-on switching	Turn-off switching	Total
$\alpha=\pi/6$	17.5	8.3	0.8	26.6
$\alpha=\pi/5$	17.3	7.5	0.7	25.6

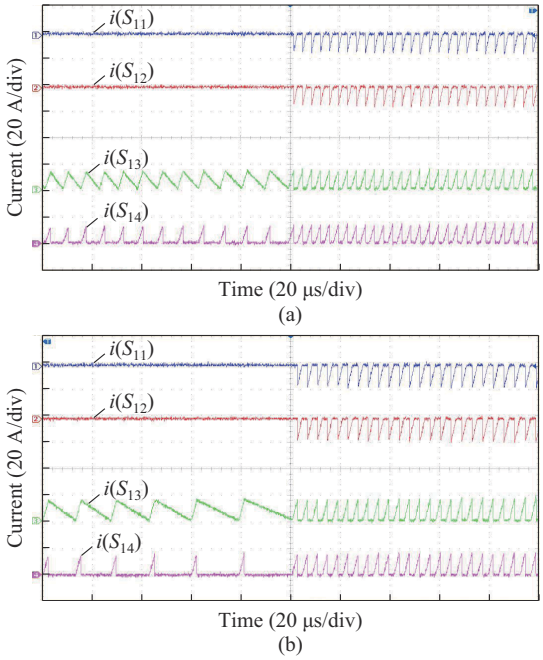

Fig. 15. Inductor current waveforms under different α when $G = 1.29$. (a) $\alpha = \pi/6$. (b) $\alpha = \pi/5$.

Finally, the conversion efficiencies of the two converters under different loads are studied, as shown in Fig. 16, and the proposed modulation strategy is proven more effective with a lighter load when the switching frequency is higher. In the studied load range, the three-level PFC converter has a 1.2% higher efficiency on average than the totem-pole PFC converter.

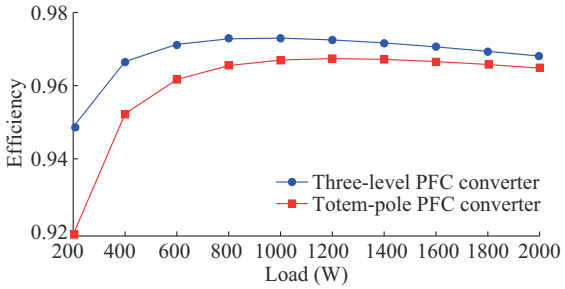

Fig. 16. Efficiency comparison of two converters.

It is noted that the converter exhibits additional losses, such as those incurred by the magnetic components (including inductor winding and core losses), which, though existed, have not been enumerated in Table V due to their comparatively minor impact in relation to switching losses. Nevertheless, it is imperative to conduct a comprehensive analysis of these diverse sources of losses and incorporate them in the ultimate calculation (e.g., as depicted in Fig. 16), to derive an accurate representation of efficiency.

VI. Conclusion

In this paper, an improved modulation strategy is designed for the three-level NPC converter in CRM with PFC. During operation, the proposed modulation strategy selects the appropriate switching state and discharging capacitor scheme, and achieves a unity PF. Compared with the totem-pole PFC converter, the proposed modulation strategy is proven to have a notably lower switching frequency regulation range, which is beneficial to the design of EMI filters. Also, the average switching times of each switch are reduced, thereby increasing the converter efficiency in the full load range. Experiment results also prove the effectiveness of the theoretical analysis in this paper.

Despite the successful use of the proposed modulation strategy, several issues remain to be investigated in the future, including the midpoint potential problem of the control strategy, the detailed implementation of the control strategy to achieve soft switching and reduce harmonic content, and finally, the design of an EMI filter for a wide switching frequency range.

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