

# Traveling Wave Characteristics Based Pilot Protection Scheme for Hybrid Cascaded HVDC Transmission Line

Dalin Mu, Sheng Lin, and Xiaopeng Li

**Abstract**—The hybrid cascaded high-voltage direct current (HVDC) transmission system has various operation modes, and some operation modes are having sharply increasing requirements for protection rapidity, while the traditional pilot differential protection (PDP) has poor rapidity, and even refuses to operate when faults occur on the DC line. Therefore, a novel pilot protection scheme based on traveling wave characteristics is proposed. First, the adaptability of the traditional PDP applied in engineering is analyzed for different operation modes. Then, the expressions of the forward traveling wave (FTW) and backward traveling wave (BTW) on the rectifier side and the inverter side are derived for different fault locations. From the theoretical derivation, the difference between the BTW and FTW on the rectifier side is less than zero, and the same is true on the inverter side. However, in the event of an external fault of DC line, the difference between the BTW and FTW at near-fault terminal protection installation point is greater than zero. Therefore, by summing over the product of the difference between BTW and FTW of the rectifier side and that of the inverter side, the fault identification criterion is constructed. The simulation results show that the proposed pilot protection scheme can quickly and reliably identify the short-circuit faults of DC line in different operation modes.

**Index Terms**—Hybrid cascaded high-voltage direct current (HVDC) transmission system, DC line, operation mode, pilot protection.

## I. INTRODUCTION

**H**YBRID cascaded high-voltage direct current (HVDC) systems, which combine the advantages of line commutated converter based HVDC (LCC-HVDC) and modular multilevel converter based HVDC (MMC-HVDC) technologies, have become a hot spot for academic research and engineering applications [1]–[3]. For example, the Baihetan-Jiangsu HVDC Project of China (referred to as the Bai-Jiang Proj-

ect) is a hybrid cascaded HVDC project, and has been put into operation in 2022. To ensure the safe and stable operation of the hybrid cascaded HVDC project, the traveling wave protection of the DC lines is equipped as the primary protection [4], [5], and the differential undervoltage protection and pilot protection are equipped as the backup protection [6]–[9]. Among them, the pilot protection configured in the project is generally pilot differential protection (PDP), which has absolute selectivity. However, in order to avoid the influence of the transient process of the ultra-long line capacitive current, a long time delay must be carried out, and the operation time of PDP is as long as 1.1 s [10]. The converter valve protection such as the maximum trigger angle monitoring protection will operate before the PDP operation [11], [12]. Unfortunately, the PDP loses the role of backup protection for the DC line.

To improve the rapidity of PDP, extensive studies have been carried out from the aspects of PDP optimization [10], [13]–[15] and new protection principles [16]–[27]. In terms of the PDP optimization, with regard to the problem of HVDC systems blocking caused by improper coordination of the PDP and the maximum trigger angle monitoring protection, the PDP blocking logic with a delay of 600 ms is removed, and the time combination of PDP and converter valve protection is optimized in [10]. The AC voltage is used as an auxiliary criterion for PDP in [13], which can provide selectivity for the delay blocking logic, and the proposed optimization method considers the reliability and rapidity of PDP.

In terms of new principles of pilot protection, it mainly includes the protection schemes based on different feature quantities at both ends of the DC line, or the protection schemes using boundary characteristics of the DC line. For the former, a PDP principle based on the virtual impedance of the fault component is proposed in [16], which can achieve fault identification and high sensitivity for different kinds of faults. In addition, the boundary characteristics are also used. Electrical similarity and cosine distance are also used to identify DC line faults in [17]–[19]. For example, the correlation between the forward traveling wave (FTW) of line-mode fault voltage on the rectifier side and the backward traveling wave (BTW) of line-mode fault voltage on the inverter side are calculated to formulate the detection criterion of DC line fault in [17], but the selection of the

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threshold value for fault identification cannot be founded. Directional pilot protection method is also used in [20], [21]. However, this method not only requires to send the local protection information to the remote end, but also needs to send the information back from the remote end, resulting in long delay and complex time sequence.

For the latter, the DC line fault of LCC-HVDC is identified by using surge impedance at tuning frequency and transient energy ratio based on the DC filter (DCF) boundaries at both ends of the DC line in [22], [23]. The proposed method may be affected by the operation state of the DCF. Regarding the smoothing reactor boundary of MMC-HVDC, the voltage polarity and power characteristics of the reactor are used to construct the protection criterion in [25], and the proposed method is simple but has high sensitivity. In addition, a protection method that does not depend on the line boundary is proposed in [27]. The above methods improve the protection performance for the DC line to a certain extent, and shorten the pilot protection operation time from the second level to the 100-ms level.

However, for the hybrid cascaded HVDC systems with a structure similar to the Bai-Jiang Project, the three MMCs on the inverter side adopt a half-bridge submodule, with as many as 621 operation modes [28]. The boundaries at both ends of the DC line are not symmetrical. There are significant differences in the fault characteristics for DC lines in different operation modes. For example, when the inverter side of the hybrid cascaded HVDC systems operates in half-voltage mode only with MMC, the MMC submodule will discharge after the DC line fault, and the fault development process is rapid due to the small dampness of the system. If the traditional PDP is not applicable to different operation modes of hybrid cascaded HVDC systems, it is necessary to study an accurate and fast pilot protection method for DC lines that takes into account the operation mode.

Based on this, the difference in the rapidity requirements of PDP in different operation modes of hybrid cascaded HVDC systems is considered, and a novel pilot protection scheme, which is suitable for multiple operation modes, is proposed. The principle of PDP adopted in the existing engineering is introduced in detail, which requires long delays to eliminate the effect of line distribution capacitance. The characteristics of line-mode voltage after fault at different positions are analyzed, and the FTW and BTW expressions are derived. Through analysis, it is found that only when the DC line fault occurs, both the difference values between BTW and FTW on the rectifier side and the inverter side are less than zero, but the external fault of DC line does not have such a feature. Therefore, this paper identifies the short-circuit faults of DC lines based on this characteristic. The proposed pilot protection scheme does not need to consider the transient process of faults in AC system, which improves the rapidity of the protection operation.

## II. ADAPTABILITY ANALYSIS OF PDP FOR DC LINES

### A. Hybrid Cascaded HVDC System and Operation Mode

This paper focuses on the Bai-Jiang Project in China, a

typical hybrid cascaded HVDC project. The rectifier of the hybrid cascaded HVDC systems is constructed with two 12-pulse LCCs, and the inverter is composed of a 12-pulse LCC in series with three parallel MMCs. Due to the symmetry of the bipolar structure for cascaded HVDC system, this paper only analyzes the unipolar structure, as shown in Fig. 1, where  $f_1$  represents the DC line fault,  $f_2$  represents the backward external fault of DC line, and  $f_3$  represents the forward external fault of DC line.

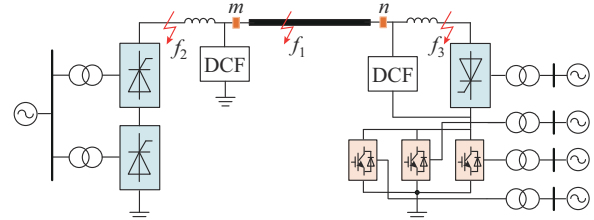


Fig. 1. Unipolar structure of full-voltage operation.

Hybrid cascaded HVDC systems have two operation modes: full-voltage and half-voltage [28]. At the same time, the number of MMCs in operation is considered. For the full-voltage operation mode, the inverter side has three operation modes, i.e., an MMC, two MMCs, and three MMCs are put into operation, respectively. For the half-voltage operation mode, the inverter side has four operation modes, i.e., a 12-pulse LCC, an MMC, two MMCs, and three MMCs are put into operation, respectively. The MMC submodule capacitor uncontrollably discharges to the fault point when a short-circuit fault occurs in the DC system. In order to consider the most serious fault conditions for the proposed pilot protection scheme, this paper takes the case where three MMCs are put into operation simultaneously as an example for analysis.

This paper takes the bipolar full-voltage operation (Mode a), the bipolar half-voltage operation of high-voltage valve (Mode b), and the bipolar half-voltage operation of low-voltage valve (Mode c) as examples for fault analysis. The unipolar structures of Mode b and Mode c are shown in Fig. 2.

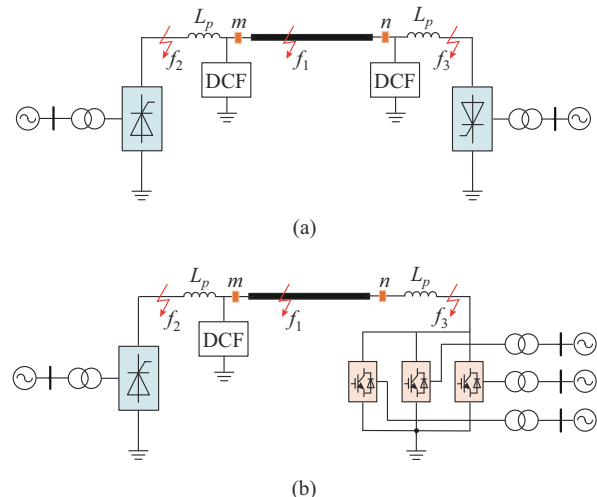


Fig. 2. Unipolar structures of half-voltage operation. (a) Mode b. (b) Mode c.

Combined with Fig. 1 and Fig. 2, different structures of the converter station will result in different boundary components at both ends of the DC line for Modes a-c. Mode a and Mode b are affected by the single-phase conductivity of the LCC, and the inverter side will not discharge to the fault point when a short-circuit fault occurs on the DC line. However, for Mode c, the MMC will definitely discharge to the fault point when a short-circuit fault occurs on the DC line, and its fault current will have a huge impact on the DC system.

### B. Adaptability Analysis of PDP

The difference of the DC line current between the rectifier station and the inverter station  $i_{dif}$  is calculated, and if it is greater than the setting value within a certain period of time, it will be determined that a short-circuit fault occurs on the DC line. The criteria can be expressed as:

$$\begin{cases} i_{dif} = |i_{DL} - i_{DLOST}| \\ i_{RES} = |i_{DL} + i_{DLOST}|/2 \\ i_{dif} > \max(i_{set}, k_{set} i_{RES}) \end{cases} \quad (1)$$

where  $i_{DL}$  is the DC line current of the rectifier station;  $i_{DLOST}$  is the contralateral current;  $i_{RES}$  is the restraint current;  $i_{set}$  is the setting value; and  $k_{set}$  is the ratio factor.

In the project, to prevent the PDP malfunction resulted from the transient influence of AC short-circuit fault, the following protection logic is formulated: the current differences before and after 65 ms on the rectifier side and the inverter side, i.e.,  $\Delta i_R$  and  $\Delta i_I$ , are calculated, respectively. If the current difference  $\Delta i_R$  or  $\Delta i_I$  is greater than the setting value (0.105 p.u.), a 600 ms lock-up delay will be carried out. And if  $\Delta i_R$  or  $\Delta i_I$  still exceeds the setting value during the lock-up period, the 600 ms lock-up delay will be repeated. This is called delay lock-up strategy (DLS). At the same time, after satisfying the PDP criterion, a 500 ms operation delay is required before the signal is issued. Therefore, the PDP requires a delay of 1.1 s.

According to the actual engineering parameters, this paper builds a simulation model based on PSCAD/EMTDC, and analyzes the PDP operation performance in different modes of hybrid cascaded HVDC systems. Figure 3 shows the simulation results of  $\Delta i_R$  and  $\Delta i_I$ , the state of DLS  $i_{dif}$ , and the DC line currents  $i_{MMC1}$ – $i_{MMC3}$  of MMC1–MMC3, when a 100  $\Omega$  grounding fault occurs at the midpoint of the DC line for Mode c. The operation results of the PDP  $L_{PDP}$  for inverter and rectifier stations are shown in Fig. 3(e). The control strategy of Mode c on the inverter side is that MMC1 adopts constant DC voltage control, and MMC2 and MMC3 adopt fixed active power control. The control characteristic curves of inverter station MMCs are shown in Fig. 4, where  $U_{dcref}$ ,  $P_{mmc1}$ ,  $P_{ref,mmc2}$ , and  $P_{ref,mmc3}$  are the reference voltage of MMC1, the active power of MMC1, the reference active power of MMC2, and the reference active power of MMC3, respectively. The fault time is 2 s, and the fault duration time is 1.5 s. The control strategy of MMCs is the same in the full-voltage operation mode and half-voltage operation of low-voltage valve mode.

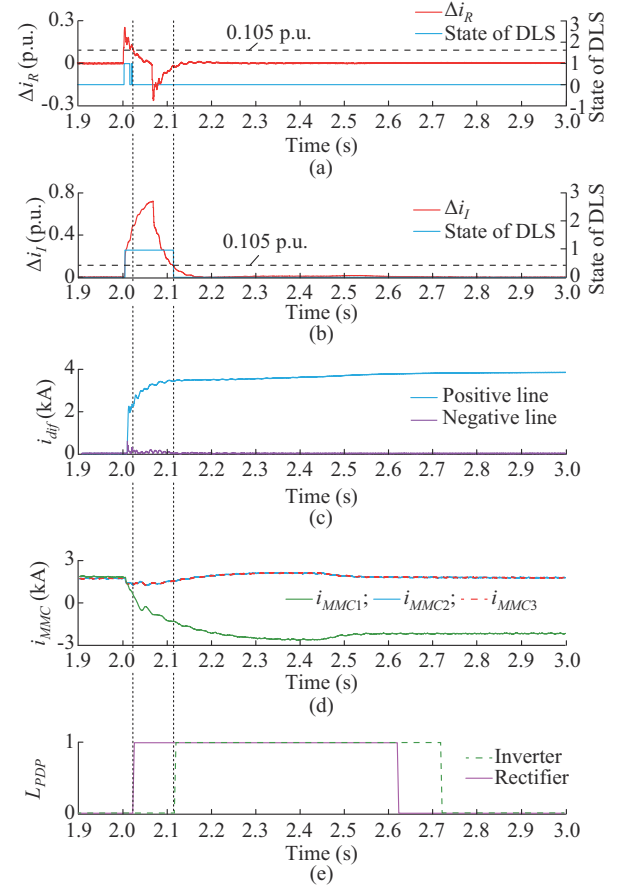


Fig. 3. PDP operation characteristics of DC line fault for Mode c. (a)  $\Delta i_R$  and state of DLS. (b)  $\Delta i_I$  and state of DLS. (c)  $i_{dif}$ . (d)  $i_{MMC1}$ . (e)  $L_{PDP}$ .

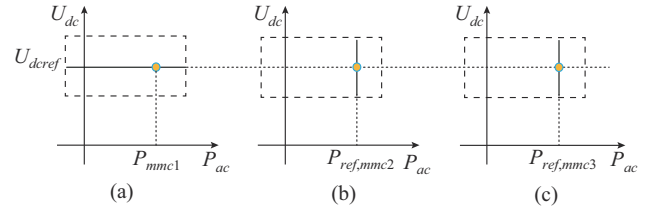


Fig. 4. Control characteristic curves of inverter station MMCs. (a) MMC1. (b) MMC2. (c) MMC3.

It can be observed from Fig. 3 that the last peak time when  $\Delta i_R$  is greater than the setting value 0.105 p.u. appears at 2.024 s, which is the moment that the last DLS is executed, and the PDP will block for 600 ms. The current difference between the rectifier side and the inverter side of the positive line  $\Delta i_{Pdif}$  increases rapidly and it is greater than the PDP threshold value. Coupled with the protection operation delay of 500 ms, the fastest operation time is 1.124 s after the fault. MMC1 discharges after the fault, and its discharging current  $i_{MMC1}$  can reach 2.86 kA, which is 1.713 times the rated current 1.67 kA, and can exceed 2.4 kA continuously for a long time. MMC1 operates at a high fault current state for a long time. Similarly,  $\Delta i_I$  is greater than the setting value at 2.142 s, and the fastest operation time is 1.242 s after the fault due to the operation of DLS. MMC1 also operates with a longer period for high fault current, which seriously threatens the reliable operation of the system. In addi-

tion, the PDP adaptability in the other two modes are also analyzed, and the MMC does not discharge to the fault point. That is, the requirement for the rapidity of pilot protection for Mode c is much more urgent compared with Mode a and Mode b. Therefore, it is urgent to propose a fast pilot protection scheme to reduce the harm of the huge inrush current to the HVDC system in Mode c.

### III. FAULT CHARACTERISTIC ANALYSIS

The electrical quantities between the bipolar DC line are decoupled by pole-mode conversion. In addition, considering the frequency variable characteristics of the DC line, this paper analyzes the fault characteristics with the line-mode component. The fault characteristics of Modes a-c are analyzed, but only the fault analytical expression of Mode c is given due to space limitations.

#### A. DC Line Fault

From Fig. 2(b), it can be observed that when a fault  $f_1$  occurs on the positive DC line at a distance of  $x$  km from the rectifier side, the Peterson equivalent diagram of the line-mode fault component on both sides of the DC line is shown in Fig. 5.

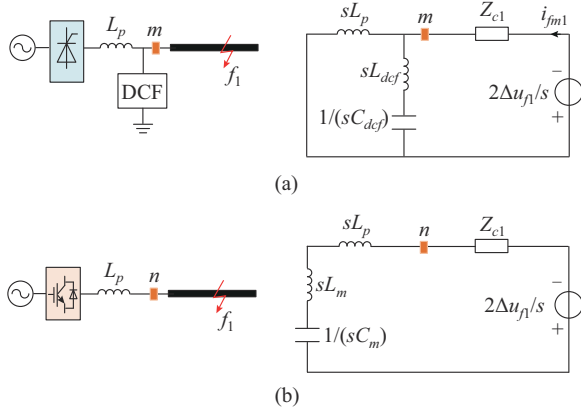


Fig. 5. Peterson equivalent diagram of fault  $f_1$ . (a) Rectifier side. (b) Inverter side.

From Fig. 5, the fault component propagates to points  $m$  and  $n$ , and the refraction and reflection occur at the impedance discontinuity position. As observed from Fig. 5(a), the circuit equation at point  $m$  is obtained as:

$$-2\Delta u_{f1} = Z_{c1} i_{fm1} + u_c + L_{def} C_{def} \frac{d^2 u_c}{dt^2} \quad (2)$$

where  $\Delta u_{f1}$  is the voltage amplitude at the fault point;  $L_{def}$  is the equivalent inductance of DCF;  $C_{def}$  is the equivalent capacitance of DCF;  $u_c$  is the terminal voltage of  $C_{def}$ ;  $i_{fm1}$  is the fault current of DC line;  $Z_{c1}$  is the line-mode wave impedance of the DC line; and the subscript 1 represents the fault  $f_1$ .

For  $f_1$ , the relationship of FTW, BTW, and refracted traveling wave at point  $m$ , i.e.,  $u_{Bm1}$ ,  $u_{Em1}$ , and  $u_{Fm1}$ , respectively, is expressed as:

$$u_{Em1} = u_{Fm1} - u_{Bm1} \quad (3)$$

$u_{Em1}$  can be expressed as:

$$u_{Em1} = -\Delta u_{f1} e^{-\gamma_1 x} \quad (4)$$

where  $\gamma_1$  is the the line-mode component of the propagation coefficient.

From Fig. 5(a), the BTW  $u_{Em1}$  propagated from the fault point to point  $m$  has the following relationship with the refracted wave  $u_{mb}$  as:

$$-2\Delta u_{f1} e^{-\gamma_1 x} = Z_{c1} i_{fm1} + u_{mb} \quad (5)$$

where  $u_{mb}$  is the refracted voltage at point  $m$ .

Therefore,  $u_{Bm1}$  can be expressed as:

$$u_{Bm1} = u_{mb} + \Delta u_{f1} e^{-\gamma_1 x} = -\Delta u_{f1} e^{-\gamma_1 x} - Z_{c1} i_{fm1} \quad (6)$$

$i_{fm1}$  can be calculated according to Fig. 4(a), and the calculation expression is given as:

$$i_{fm1}(s) = \frac{-2\Delta u_{f1} [sL_p + sL_{def} + 1/(sC_{def})]}{s(sL_p + Z_{c1})[sL_{def} + 1/(sC_{def})] + s^2 L_p Z_{c1}} \quad (7)$$

$i_{fm1}$  can be obtained by the first-order model approximation as:

$$i_{fm1}(s) = -2\Delta u_{f1} \frac{L_p}{s + \frac{Z_{c1}}{L_p}} \quad (8)$$

Then, the reverse Laplace transform is performed to obtain  $i_{fm1}(t)$  as:

$$i_{fm1}(t) = -2\Delta u_{f1} L_p e^{-\frac{Z_{c1}}{L_p} t} \quad (9)$$

From (4), (6), and (9),  $u_{Bm1}$  is expressed as:

$$u_{Bm1}(t) = 2Z_{c1} L_p \Delta u_{f1} e^{-\gamma_1 x - \frac{Z_{c1}}{L_p} t} - \Delta u_{f1} e^{-\gamma_1 x} \quad (10)$$

Similarly, for the inverter side, the BTW at point  $n$   $u_{En1}$  can be obtained as:

$$u_{En1} = -\Delta u_{f1} e^{-\gamma_1 (L-x)} \quad (11)$$

where  $L$  is the whole length of DC line.

The FTW at point  $n$   $u_{Bn1}$  is expressed as:

$$u_{Bn1}(t) = 2Z_{c1} L_p \Delta u_{f1} e^{-\gamma_1 (L-x) - \frac{Z_{c1}}{L_p} t} - \Delta u_{f1} e^{-\gamma_1 (L-x)} \quad (12)$$

The difference between  $u_{Em1}$  and  $u_{Bm1}$ , i.e.,  $\Delta u_{mf1}(t)$ , is expressed as:

$$\Delta u_{mf1}(t) = -2Z_{c1} L_p \Delta u_{f1} e^{-\gamma_1 x - \frac{Z_{c1}}{L_p} t} \quad (13)$$

The difference between  $u_{En1}$  and  $u_{Bn1}$ , i.e.,  $\Delta u_{nf1}(t)$ , is expressed as:

$$\Delta u_{nf1}(t) = -2Z_{c1} L_p \Delta u_{f1} e^{-\gamma_1 (L-x) - \frac{Z_{c1}}{L_p} t} \quad (14)$$

The product of (13) and (14)  $K_1$  is expressed as:

$$K_1 = 4Z_{c1}^2 L_p^2 \Delta u_{f1}^2 e^{-\gamma_1 L - \frac{2Z_{c1}}{L_p} t} \quad (15)$$

From (15),  $K_1$  is greater than zero. That is,  $\Delta u_{mf1}$  and  $\Delta u_{nf1}$  have the same sign.

#### B. Backward External Fault of DC Line

The Peterson equivalent diagram is shown in Fig. 6 when the short-circuit fault  $f_2$  occurs. From Fig. 6, the boundaries on both sides of the DC line are asymmetrical. The line boundary on the rectifier side consists of the DCF and smoothing reactor. While on the inverter side, the smoothing



reactor and MMC are used as the physical boundary. From Fig. 6(a), the FTW at point  $m$   $u_{Bm2}$  can be expressed as:

$$u_{Bm2}(s) = \frac{-2\Delta u_{f2}[sL_p + sL_{dcf} + 1/(sC_{dcf}) + Z_{c1}]}{sZ_{c1}(sL_p + Z_{c1}) + sQ[sL_{dcf} + 1/(sC_{dcf})]} \quad (16)$$

where  $Q = 2Z_{c1} + sL_p$ ;  $\Delta u_{f2}$  is the voltage amplitude for the short-circuit fault  $f_2$  at fault point; and the subscript 2 represents the fault  $f_2$ .

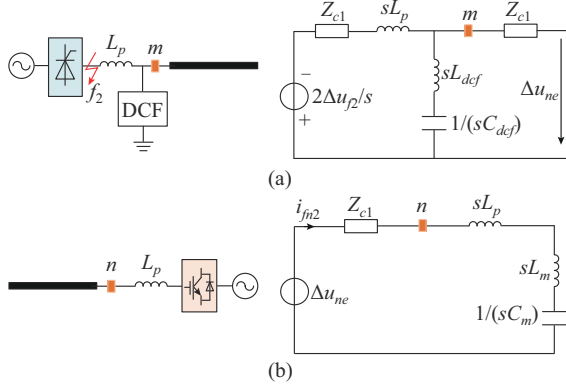


Fig. 6. Peterson equivalent diagram of fault  $f_2$ . (a) Rectifier side. (b) Inverter side.

$u_{Bm2}(t)$  is calculated by the first-order model approximation as:

$$u_{Bm2}(t) = \frac{-2\Delta u_{f2}Z_{c1}}{L_p + Z_{c1}^2 C_{dcf}} e^{-\frac{2Z_{c1}}{L_p + Z_{c1}^2 C_{dcf}} t} \quad (17)$$

The BTW at point  $m$   $u_{Em2}$  is zero within the time of  $2L/v$  ( $v$  is the line-mode wave velocity) after the FTW is detected. The FTW at point  $m$  propagates to point  $n$ , and the BTW at point  $n$   $u_{En2}$  is expressed as:

$$u_{En2} = u_{Bm2}(t) e^{-\gamma_1 L} \quad (18)$$

Referring to (5) and (6), the FTW at point  $n$   $u_{Bn2}$  can be obtained as:

$$u_{Bn2} = u_{En2} - i_{fn2} Z_{c1} \quad (19)$$

The DC line current  $i_{fn2}$  can be calculated as:

$$i_{fn2}(s) = \frac{u_{mf2}(t)}{sL_p + Z_{c1} + sL_m + 1/(sC_m)} \quad (20)$$

where  $L_m$  is the arm equivalent reactance; and  $C_m$  is the arm equivalent capacitance of the three parallel MMCs.

$i_{fn2}$  is calculated by the first-order model approximation as:

$$i_{fn2}(s) = -2\Delta u_{f2} \frac{Z_{c1} C_m / G}{s + 2Z_{c1} / G} \quad (21)$$

where  $G = L_p + 2Z_{c1}^2 C_m + Z_{c1} L_{dcf} (Z_{c1} + L_p)$ .

The reverse Laplace transform is performed for (21), and  $i_{fn2}(t)$  can be expressed as:

$$i_{fn2}(t) = -\frac{2\Delta u_{f2} Z_{c1} C_m}{G} e^{-\frac{2Z_{c1}}{G} t} \quad (22)$$

The expression of  $u_{Bn2}$  is given as:

$$u_{Bn2}(t) = \frac{2\Delta u_{f2} Z_{c1}^2 C_m}{G} e^{-\frac{2Z_{c1}}{G} t} + u_{mf2}(t) e^{-\gamma_1 L} \quad (23)$$

The difference between  $u_{Em2}$  and  $u_{Bm2}$ , i.e.,  $\Delta u_{mf2}(t)$ , is given as:

$$\Delta u_{mf2}(t) = \frac{2\Delta u_{f2} Z_{c1}}{L_p + Z_{c1}^2 C_{dcf}} e^{-\frac{2Z_{c1}}{L_p + Z_{c1}^2 C_{dcf}} t} \quad (24)$$

The difference between  $u_{En2}$  and  $u_{Bn2}$ , i.e.,  $\Delta u_{nf2}(t)$ , is given as:

$$\Delta u_{nf2}(t) = -\frac{2\Delta u_{f2} Z_{c1}^2 C_m}{G} e^{-\frac{2Z_{c1}}{G} t} \quad (25)$$

The product of (24) and (25)  $K_2$  is expressed as:

$$K_2 = -\frac{4\Delta u_{f2}^2 Z_{c1}^3 C_m}{G(L_p + Z_{c1}^2 C_{dcf})} e^{-\frac{2Z_{c1}}{L_p + Z_{c1}^2 C_{dcf}} t - \frac{2Z_{c1}}{G} t} \quad (26)$$

From (26),  $K_2$  is less than zero. That is,  $\Delta u_{mf2}(t)$  and  $\Delta u_{nf2}(t)$  have different signs.

### C. Forward External Fault of DC Line

For the fault  $f_3$ , the Peterson equivalent circuit diagram is shown in Fig. 7. According to Fig. 7(a), the FTW at point  $n$   $u_{Bn3}$  can be expressed as:

$$u_{Bn3}(s) = \frac{-2\Delta u_{f3} Z_{c1}}{s(2Z_{c1} + sL_p)} \quad (27)$$

where  $\Delta u_{f3}$  is the voltage amplitude for the short-circuit fault  $f_3$  at fault point; and the subscript 3 represents the fault  $f_3$ .

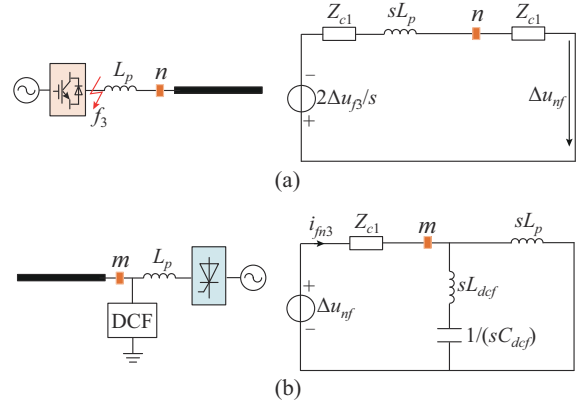


Fig. 7. Peterson equivalent diagram of fault  $f_3$ . (a) Rectifier side. (b) Inverter side.

$u_{Bn3}(t)$  is obtained by the reverse Laplace transform as:

$$u_{Bn3}(t) = -2\Delta u_{f3} e^{-\frac{2Z_{c1}}{L_p} t} \quad (28)$$

However, the BTW is zero within the time  $2L/v$  after the FTW being detected at point  $n$ . The FTW at point  $n$  propagates to  $m$  on the full line length of  $L$ , and the BTW at point  $m$   $u_{Em3}$  is expressed as:

$$u_{Em3} = -2\Delta u_{f3} e^{-\frac{2Z_{c1}}{L_p} t - \gamma_1 L} \quad (29)$$

The FTW at point  $m$   $u_{Bm3}$  can be obtained as:

$$u_{Bm3} = u_{Em3} - Z_{c1} i_{fm3} \quad (30)$$

The DC line current  $i_{fm3}$  can be calculated as:

$$i_{fm3}(s) = \frac{u_{Em3} [sL_p + sL_{dcf} + 1/(sC_{dcf})]}{[sL_{dcf} + 1/(sC_{dcf})](Z_{c1} + sL_p) + sL_p Z_{c1}} \quad (31)$$

$i_{fm3}$  is expressed by the first-order approximation model as:

$$i_{fm3}(s) = 2u_{Em3} \frac{1/L_p}{s + 2Z_{c1}/L_p} \quad (32)$$

The reverse Laplace transform is performed for the above equation, and  $i_{fm3}(t)$  is expressed as:

$$i_{fm3}(t) = \frac{2u_{Em3}}{L_p} e^{-\frac{2Z_{c1}}{L_p}t} \quad (33)$$

The expression of  $u_{Bm3}$  is given as:

$$u_{Bm3}(t) = 4\Delta u_{f3} \frac{Z_{c1}}{L_p} e^{-\gamma_1 L - \frac{4Z_{c1}}{L_p}t} - 2\Delta u_{f3} e^{-\gamma_1 L - \frac{2Z_{c1}}{L_p}t} \quad (34)$$

The difference between  $u_{Em3}(t)$  and  $u_{Bm3}(t)$ , i.e.,  $\Delta u_{mf3}(t)$ , is given as:

$$\Delta u_{mf3}(t) = -4\Delta u_{f3} \frac{Z_{c1}}{L_p} e^{-\gamma_1 L - \frac{4Z_{c1}}{L_p}t} \quad (35)$$

The difference between  $u_{En3}(t)$  and  $u_{Bn3}(t)$ , i.e.,  $\Delta u_{nf3}(t)$ , is given as:

$$\Delta u_{nf3}(t) = 2\Delta u_{f3} e^{-\frac{2Z_{c1}}{L_p}t} \quad (36)$$

The product of (35) and (36)  $K_3$  is expressed as:

$$K_3 = -8\Delta u_{f3}^2 \frac{Z_{c1}}{L_p} e^{-\gamma_1 L - \frac{6Z_{c1}}{L_p}t} \quad (37)$$

From (37),  $K_3$  is less than zero. That is,  $\Delta u_{mf3}(t)$  and  $\Delta u_{nf3}(t)$  have different signs.

Similarly, Mode a and Mode b are also analyzed, and the above regularities still hold true. That is, the products of the traveling wave difference for the rectifier side and the inverter side are all greater than 0 for all of the three kinds of operation modes when short-circuit faults occur on the DC line, and it is less than 0 in the cases of external faults. In addition, since Mode b operates in the same way as the traditional LCC-HVDC structure, it shows that the proposed pilot protection scheme is also suitable for the traditional LCC-HVDC system.

#### IV. PILOT PROTECTION SCHEME

##### A. Start-up Criterion

The start-up criterion is carried out by the change of the line-mode current. The improved current gradient algorithm is used, and the expression is shown as:

$$I_{start} = \sum_{N=i+1}^{i+3} i_1(N) - \sum_{N=i-3}^{i-1} i_1(N) > \Delta i_{set} \quad (38)$$

where  $i_1(N)$  is the line-mode current sampling value on the rectifier or inverter side of the DC line; and  $\Delta i_{set}$  is the setting value, and it is 0.01 p.u..

##### B. Fault Identification Criterion

From the analysis in Section III, it can be observed that when short-circuit faults occur on the DC line, both the difference between BTW and FTW on the rectifier side and that on the inverter side have the same sign. For the external fault, they have different signs. Therefore, based on the data of the FTW and BTW of the first detection of the traveling wave after the fault, the product of  $\Delta u_{mf}(n)$  and  $\Delta u_{nf}(n)$  is

calculated, and if it is greater than 0, the DC line fault is identified. The pilot protection criterion of DC line fault is set as:

$$K = \sum_{n=0}^P \Delta u_{mf}(n) \Delta u_{nf}(n) > 0 \quad (39)$$

where  $P$  is the number of sampling points, and the value of  $P$  is determined by the sampling data window. Theoretically, the shorter the length of the data window, the faster the fault detection, which satisfies the protection rapidity requirements, but the protection reliability may be reduced by the influence of system disturbance. The longer the data window, the longer the fault detection time, which meets the protection reliability requirements, but reduces the protection operation quickness. Based on this, the time window of the traveling wave difference is taken as 0.2 ms in this paper. Therefore,  $P$  is equal to 20.

The DC line fault is identified when  $K > 0$ . Otherwise, it indicates that the external fault of the DC line occurs.

##### C. Fault Pole Identification Criterion

For a short-circuit fault on the DC line, in order to further determine whether the fault is located on the positive line, negative line, or bipolar line, the zero-mode component of fault voltage  $u_0$  is used to construct the fault pole identification criterion, and the expression is given as:

$$\begin{cases} u_0 \geq u_{0set} & NP \\ u_0 \leq -u_{0set} & PP \\ -u_{0set} < u_0 < u_{0set} & DP \end{cases} \quad (40)$$

where  $u_{0set}$  is the protection threshold value, which is set to be greater than the maximum unbalance voltage of the bipolar fault, and it can be set to be 0.05 p.u.;  $NP$  represents that the short-circuit faults on the negative line;  $PP$  represents that the short-circuit faults on the positive line; and  $DP$  represents that the short-circuit faults on the bipolar line.

##### D. Flowchart of Pilot Protection Scheme

The flowchart of the proposed pilot protection scheme of the DC line for the hybrid cascaded HVDC system is shown in Fig. 8. The voltage and current on the rectifier side and the inverter side of the bipolar DC line are measured. The line-mode current and voltage and the zero-mode voltage are calculated using the measured data. The FTW and BTW can also be calculated. When the start-up criterion is met, the traveling wave difference on the rectifier side and the inverter side are calculated, respectively. The product  $K$  is calculated and used to determine whether the criterion is satisfied. If  $K > 0$ , it indicates that a short-circuit fault occurs on the DC line, and the fault pole is further identified. Otherwise, it is determined that no fault occurs on the DC line.

#### V. SIMULATION VALIDATIONS

##### A. Simulation Model and Control Strategy

Bipolar models in different operation modes of the hybrid cascaded HVDC systems are built on PSCAD/EMTDC as follows.

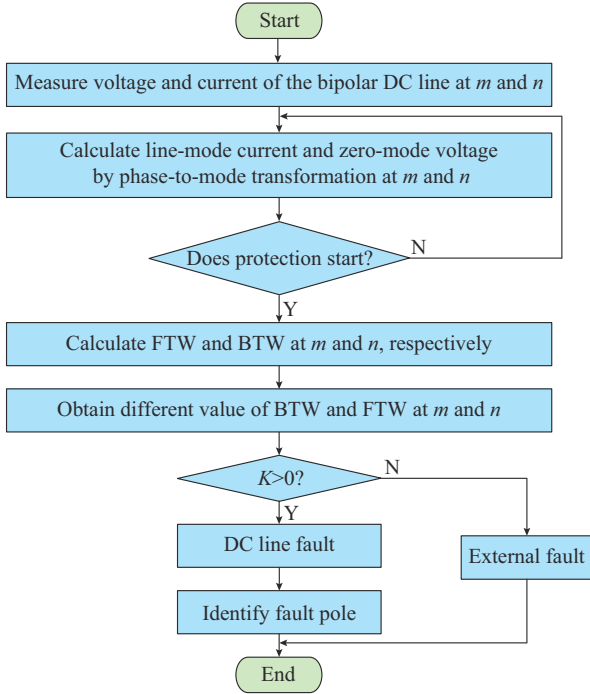


Fig. 8. Flowchart of proposed pilot protection scheme.

1) Model a. The rectifier station adopts two 12-pulse LCCs, the high-voltage side of the inverter station is a 12-pulse LCC, and the low-voltage side includes three parallel MMCs, of which the number of modules on MMC bridge arm is 200. The control strategy is that the rectifier side adopts fixed DC current control, the high-voltage side of the inverter side adopts fixed DC voltage control, the low-voltage side of inverter station adopts fixed DC voltage control and fixed reactive power control, and the remaining two MMCs adopt fixed active power control and fixed reactive power control.

2) Mode b. Rectifier side and inverter side both have a 12-pulse LCC in operation. The rectifier side adopts fixed DC current control, and the inverter side adopts fixed DC voltage control.

3) Mode c. Rectifier side has a 12-pulse LCC, and inverter side contains three parallel MMCs. The control strategy of the rectifier side is the same as that of Mode b, and the control strategy of the three MMCs is the same as that of Mode a. The DC line adopts the frequency variable parameter model and the line length  $L$  is 2086 km. The sampling frequency is 100 kHz.

### B. Performance Verification of Proposed Pilot Protection Scheme

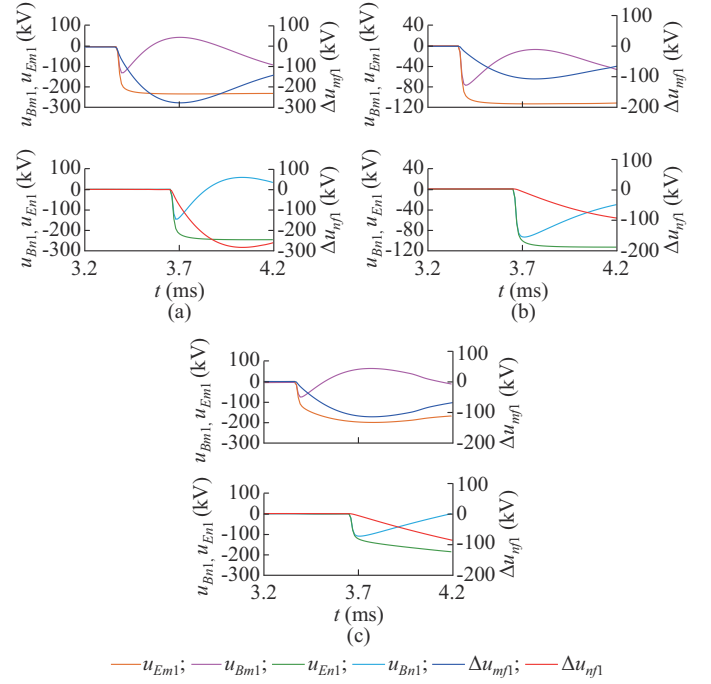
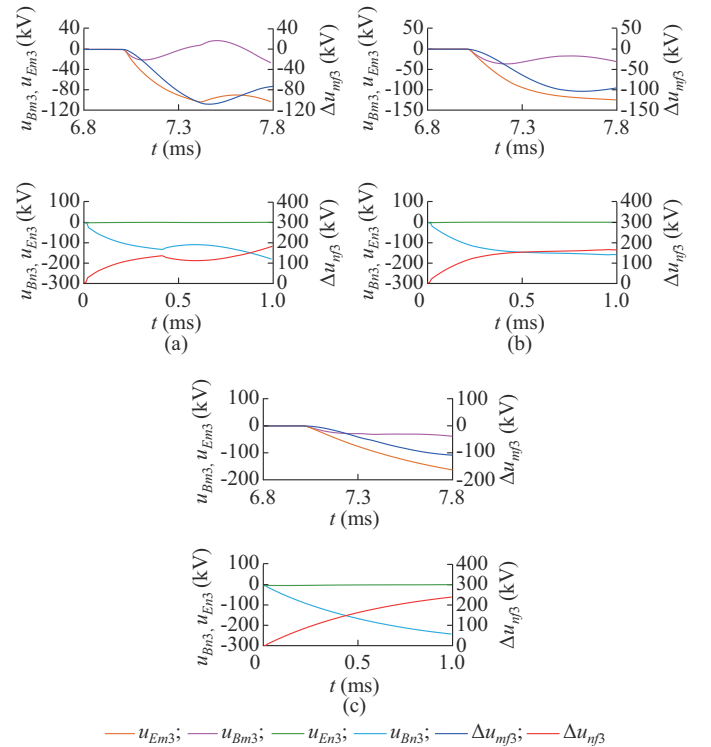
In the three operation modes, the following two cases are simulated.

Case 1: 100  $\Omega$  grounding short-circuit fault  $f_1$  occurs at  $x=1000$  km.

Case 2: metal grounding short-circuit fault  $f_3$  occurs on the positive DC line.

For the fault  $f_1$ , the simulation results of the FTWs and BTWs on the rectifier and inverter sides, i.e.,  $u_{Bm1}$ ,  $u_{Em1}$  and

$u_{Bn1}$ ,  $u_{En1}$ , respectively, and  $\Delta u_{mf1}$  and  $\Delta u_{nf1}$  are shown in Fig. 9. For the fault  $f_3$ , the simulation results are shown in Fig. 10.

Fig. 9. Simulation results of FTW and BTW at  $m$  and  $n$  for fault  $f_1$ . (a) Mode a. (b) Mode b. (c) Mode c.Fig. 10. Simulation results of FTW and BTW at  $m$  and  $n$  for fault  $f_3$ . (a) Mode a. (b) Mode b. (c) Mode c.

It can be observed from Fig. 9 that, after the short-circuit faults occur on the DC line, the FTWs and BTWs on the rectifier and inverter side completely overlap within a short pe-

riod when the fault traveling wave is detected. Subsequently, the FTWs on both sides begin to decrease and then increase, that is, the FTWs begin to change in the opposite direction. However, the BTWs still remain unchanged in the original direction, and the BTWs basically stabilize rapidly in Mode a and Mode b. For Mode c, the BTW on the rectifier side increases and decreases, while the BTW on the inverter side slowly increases, and the value of Mode c is closer to that of Mode a. The main reason for this difference is that the capacitors of three MMCs will discharge in Mode c. It can be observed from Fig. 10 that for fault  $f_3$ , the FTW on the inverter side is almost zero, and only the BTW can be detected within the time  $2L/v$  after the FTW is obtained. From Section III-C,  $\Delta u_{m\beta}$  is less than zero, and  $\Delta u_{m\beta}$  is greater than zero. According to (39),  $K < 0$ , which indicates that the DC line is not faulty.

As can be observed from Figs. 9 and 10, the identification of the fault location can be completed within 0.2 ms after the fault traveling wave is detected, respectively, on the rectifier side and inverter side. In addition, for DC line double terminal protection, the time of data calculation and transmission cannot be ignored. The time spent on data transmission and calculation is within 20 ms. Therefore, the fault detection time is only 20.2 ms, which is a significant improvement over the 100 ms of many improved pilot protection schemes.

### C. Adaptability of Pilot Protection to Diverse Fault Conditions

The working conditions of fault locations, transition resistors, and fault types are considered in three modes to verify the adaptability of the proposed pilot protection scheme. The identification results are shown in Table I, where “A” means an internal fault, “B” means an external fault, “P” means a positive line fault, “N” means a negative line fault, and “DP” means a bipolar line fault.

### D. Comparison with Existing Schemes

From the Table I,  $K$  is always greater than zero for different cases of  $f_1$ , and the DC line fault can be identified.  $K$  is less than zero for fault  $f_2$ . In the three modes, the proposed pilot protection scheme can accurately and reliably identify DC line faults.

### E. Influence of Noise

In actual engineering, the influence of noise is inevitable. It is necessary to study the performance of pilot protection under noise interference. In particular, the noise is mixed in the first step during the measurement of electrical quantities. Therefore, Gaussian white noise is added to the voltage and current signals with signal-to-noise ratios (SNRs) of 30 dB and 40 dB. The positive line fault at  $x=500$  km for three operation modes with  $1000 \Omega$  fault resistance is simulated to demonstrate the robustness performance. The results are shown in Table II. Obviously, the proposed pilot protection scheme can still detect faults with noise at 30 dB and 40 dB, and it has a high anti-noise ability.

TABLE I  
SIMULATION RESULTS OF PROPOSED PILOT PROTECTION SCHEME

Operation mode	Fault case	$R_f (\Omega)$	$K$	Result
Mode a	$f_1$ -P-500	300	$>0$	A/P
	$f_1$ -P-1500	300	$>0$	A/P
	$f_1$ -P-2000	300	$>0$	A/P
	$f_1$ -N-1500	300	$>0$	A/N
	$f_1$ -P-500	500	$>0$	A/P
	$f_1$ -P-1500	500	$>0$	A/P
	$f_1$ -P-2000	500	$>0$	A/P
	$f_1$ -D-1000	0	$>0$	A/DP
	$f_2$ -P	0	$<0$	B/P
Mode b	$f_1$ -P-500	300	$>0$	A/P
	$f_1$ -P-1500	300	$>0$	A/P
	$f_1$ -P-2000	300	$>0$	A/P
	$f_1$ -N-1500	300	$>0$	A/N
	$f_1$ -P-500	500	$>0$	A/P
	$f_1$ -P-1500	500	$>0$	A/P
	$f_1$ -P-2000	500	$>0$	A/P
	$f_1$ -D-1000	0	$>0$	A/DP
	$f_2$ -P	0	$<0$	B/P
Mode c	$f_1$ -P-500	300	$>0$	A/P
	$f_1$ -P-1500	300	$>0$	A/P
	$f_1$ -P-2000	300	$>0$	A/P
	$f_1$ -N-1500	300	$>0$	A/N
	$f_1$ -P-500	500	$>0$	A/P
	$f_1$ -P-1500	500	$>0$	A/P
	$f_1$ -P-2000	500	$>0$	A/P
	$f_1$ -D-1000	0	$>0$	A/DP
	$f_2$ -P	0	$<0$	B/P

Note: taking  $f_1$ -P-500 as an example, it indicates a positive line fault at  $x=500$  km for fault  $f_1$ .

TABLE II  
RESULTS OF PROPOSED PILOT PROTECTION SCHEME WITH DIFFERENT SNRS

SNR (dB)	Operation mode	$x$ (km)	$K$	Result
30	Mode a	500	$>0$	A/P
	Mode b	500	$>0$	A/P
	Mode c	500	$>0$	A/P
40	Mode a	500	$>0$	A/P
	Mode b	500	$>0$	A/P
	Mode c	500	$>0$	A/P

### F. Comparison with Existing Schemes

Some pilot protection schemes have been proposed using double terminal components [17], [22], [25], [26]. The comparative results of the proposed pilot protection scheme and the existing pilot protection schemes in terms of the maximum detected fault transition resistance and the maximum fault detection time are presented in Table III. As can be seen in Table III, compared with the existing pilot protection schemes, the proposed pilot protection scheme takes a shorter time in the fault detection of the DC line. At the same



time, it is also capable of detecting pole-to-ground faults with a high resistance of 1000  $\Omega$ .

TABLE III  
COMPARISON RESULTS OF PROPOSED PILOT PROTECTION SCHEME  
WITH EXISTING ONES

Pilot protection scheme	The maximum fault resistance ( $\Omega$ )	Sampling time window (ms)
[17]	Not declared	65.0
[22]	300	0.5
[25]	1000	5.0
[26]	400	10.0
Proposed	1000	0.2

## VI. CONCLUSION

The hybrid cascaded HVDC system has various operation modes, and there are significant differences in the characteristics of DC line faults in different operation modes. Affected by the diverse types of converters, the fault current in some operation modes increases rapidly, and the requirement for protection rapidity is very high. For example, the discharge current of MMC on the inverter side is up to 1.7 times as that during normal operation in some modes, which poses a great threat to the safe operation of the system. Therefore, it means that the traditional PDP with a time delay of 1.1 s is no longer applicable. Based on this, this paper proposes a fast pilot protection scheme applicable to multiple operation modes according to the product of the difference voltages between the BTW and FTW on the rectifier side and the difference voltages between the BTW and FTW on the inverter side. This scheme does not require long time delays to eliminate the effect of line distributed capacitance discharge, which meets the requirements of protection rapidity. The simulation results further verify the performance of the proposed pilot protection scheme.

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