FPGA-based Digital Implementation of Flexible Power Control for Three-phase to Single-phase MMC-based Advanced Co-phase Traction Power Supply System

Jiangpeng Yang, Hongjian Lin, *Senior Member*, *IEEE*, Haotian Zhu, Zeliang Shu, *Senior Member*, *IEEE*, Lan Ma, Changsong Cai, *Senior Member*, *IEEE*, Pengcheng Zhang, *Senior Member*, *IEEE*, Li He, Ruoyu Li, Shasha Song, and Josep M. Guerrero, *Fellow*, *IEEE*

***Abstract*—A three-phase to single-phase modular multilevel converter based advanced co-phase traction power supply (MMC-ACTPS) system is an effective structure to address the concerns of phase splitting and poor power quality of the conventional electrified railway. Due to the large number of MMC-ACTPS system modules, I/O resources and computing speed have high requirements on processors. Moreover, the module capacitor balance is challenging because the sorting time is too long when the traditional sorting algorithm for voltage balance is used. To solve the above issues, a digital implementation scheme of flexible power control strategy for three-phase to single-phase MMC-ACTPS system based on field programmable gate array (FPGA), which has sufficient I/O resources, has been proposed. Due to the parallel execution characteristics of the FPGA, the execution time of the controller and the modulator can be greatly reduced compared with a digital signal processor (DSP) + FPGA or DSpace. In addition, an improved sorting algorithm is proposed to reduce the sorting time and the implementation steps are analyzed. Finally, simulation and experimental results are presented to demonstrate the effectiveness and correctness of the proposed control strategy.**

***Index Terms*—Advanced co-phase power traction supply (ACTPS) system, modular multilevel converter (MMC), digital implementation, flexible power transmission, circulating current mitigation.**

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J. Yang, H. Zhu, Z. Shu (corresponding author), L. Ma, L. He, R. Li, and S. Song are with National Rail Transportation Electrification and Automation Engineering Technology Research Center, Chengdu 611756, China, and they are also with the School of Electrical Engineering, Southwest Jiaotong University, Chengdu 611756, China (e-mail: upqcyjp@163.com; zht2246178679@163.com; shuzeliang@swjtu. edu. cn; 397845217@qq. com; 1121770418@qq. com; crexyer@qq.com; 304980647@qq.com).

H. Lin is with the Department of Electrical Engineering, City University of Hong Kong, Hong Kong, China (e-mail: lhj41333696@163.com).

C. Cai is with the School of Electrical Engineering and Automation, Wuhan University, Wuhan 430072, China (e-mail: changsongcai@whu.edu.cn).

P. Zhang is with the Department of Electrical Engineering, Tsinghua University, Beijing 100084, China (e-mail: pczhang@tsinghua.edu.cn).

J. M. Guerrero is with the Department of Energy Technology, Aalborg University, Aalborg 9220, Denmark (e-mail: joz@energy.aau.dk).

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I. Introduction

MULTILEVEL converters are worthy assets in the area for the power transmission of electrified railway. Traditional traction power supply system usually works in the heterogeneous power supply mode with multiple neutral sections (NSs), with respect to the substation (SS), as shown in Fig. 1(a) [1]. Some critical issues are resulted, such as power interruption, voltage sag, distortion, unbalance, reactive power, and harmonic [2]-[4]. To address the aforementioned issue hereinbefore, an active power compensator (APC) [5], [6] is applied as shown in Fig. 1(b). However, the voltage frequency, phase, and amplitude of two SSs in this system are uncontrollable. Hence, NSs are not totally canceled and the terminals of two adjacent catenaries could not be connected directly.

In order to connect through all catenary wires in a single-phase traction catenary grid, an advanced co-phase traction power supply (ACTPS) system based on three-phase to single-phase converters is introduced [7], [8], as shown in Fig. 1 (c). In it, power electronics technology based SS No. 3 and SS No. 4 are used to replace the traditional traction transformers, then to flexibly control voltage and power flow. Any NS in the traction grid can be removed along with compensating reactive power and harmonics.

The voltage of a three-phase grid is 110 kV or 220 kV, and the voltage of a single-phase traction grid is 25 kV. The voltage levels are too high, which makes the two-level converter unsuitable. Several modular multilevel converter based ACTPS (MMC-ACTPS) systems are proposed [9]-[12]. This kind of system is famous for its superior performance, such as its simple structure, easy control, and lower switching loss. What's more, switching devices in each bridge arm can output more voltage levels under different switching combinations [13]-[15]. In the ACTPS system, the traction

loads need to obtain active power and reactive power from the three-phase grid. However, this will reduce the power factor of the three-phase grid. To address this issue, [16] and [17] propose a transient current control strategy to ensure the running of the converter in unit power factor mode. This strategy cannot provide reactive power to the traction load. Based on this strategy, in order to flexibly decouple the active and reactive power, a nonlinear control strategy is presented in [17]. But for the nonlinear control, it is hard to implement in the digital controller. Hence, exploring a flexible power transmission control strategy is crucial.

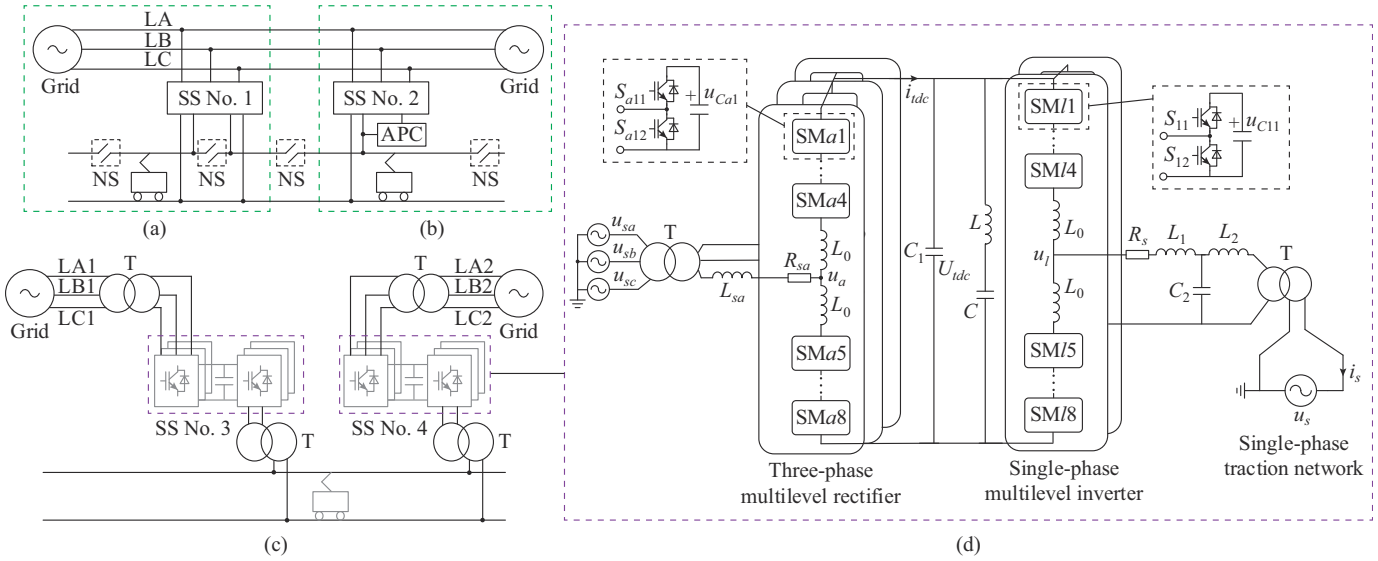


Fig. 1. Traction power supply systems. (a) Traditional traction power supply system. (b) Co-phase traction power supply system. (c) MMC-ACTPS system. (d) Circuit schematic of MMC-ACTPS system.

The existence of circulating current is an another problem in the MMC topology. The AC circulating current increases the switching device losses and the leg current of an MMC is distorted. Regarding the AC circulating current mitigation, a voltage balance model based strategy and a virtual impedance sliding mode based strategy [18]-[20] are proposed to mitigate AC circulating current for DC-DC MMC. Furthermore, a space vector modulation based strategy [21] is proposed to mitigate the circulating current and achieve the optimized power transmission as well. Strategies hereinbefore involve massive complex nonlinear calculations, which are difficult in digital implementation. In addition, [22] introduces a nearest level modulation based strategy to address this concern. But this strategy is only applicable for the application with large numbers of sub-modules (SMs). The quasi proportional-resonant (PR) controller can accurately suppress the circulation at a specific frequency, but it affects the stability of the system [23].

Although the MMC-ACTPS system can cancel all NSs, its application has been restricted. On the one hand, since the number of SMs is often dozens or even hundreds under high voltage [24], [25], the traditional sorting algorithm for capacitor voltage balance takes too long time to compute, resulting in poor control effect and even system instability. The traditional sorting algorithm for capacitor voltage balance is to compare the SM capacitor voltage of each bridge arm. This algorithm compares two capacitor voltages at a time until all capacitor voltages are compared [26], [27]. On the other hand, the control algorithm is digitally implemented with digital signal processor + field programmable gate array (DSP + FPGA) in most literature such as [10], [28]-[32]. DSPs have limitations regarding the concurrence of operations, i.e., computational simultaneity and parallelism of the calculations. The communication between DSP and FPGA is required, which increases the system complexity and decreases the reliability. DSPACE is adopted to implement control algorithms in [33]-[36]. This is a simulation system with high cost and poor practicability. Instead, in a full FPGA implementation, the parallelism of operations permits to perform the calculations of the control technique with faster processing speed. FPGA is used as the only processor in the MMC system [11], but the program design is not analyzed.

From the above discussions, the power control and circulating current suppression are two important issues for MMC systems. In addition, an algorithm to reduce the sorting time and a digital implementation scheme based on FPGA which can reduce the operation time are required. To address these issues, the main contributions of this paper are enumerated as follows.

1) A flexible power transmission control strategy and a negative sequence based AC frequency-double circulating current mitigation scheme are designed to effectively control power and circulating current.

2) A digital implementation scheme based on the FPGA of the above-mentioned control algorithm is proposed, which reduces the resource occupation and operation time. Wherein the folding structure is used to reduce the number of adders and multipliers.

3) An improved sorting algorithm is proposed, which can reduce the sorting time especially when there are many SMs and can be easily extended to N SMs.

The rest of this paper is organized as follows. The topolo-

gies and control strategy of three-phase and single-phase MMCs are analyzed in Section II. Then, the negative sequence based AC frequency-double circulating current mitigation scheme and SM capacitor voltage balancing are analyzed in Section III. A digital implementation scheme based on FPGA and an improved sorting algorithm is proposed in Section IV. Simulation and experimental results are exhibited in Section V. Finally, Section VI concludes this paper.

II. Topologies and Control Strategies of Three-phase and Single-phase MMCs

The circuit schematic of MMC-ACTPS system is shown in Fig. 1(d). It consists of a three-phase grid, a multilevel rectifier, a multilevel inverter, and a traction network, where $u_{s\varphi}$ ($\varphi = a, b, c$) denotes three-phase voltages; u_s is the single-phase voltage; i_s is the single-phase current; $L_{s\varphi}$ ($\varphi = a, b, c$) denotes the three-phase filtering inductors; $R_{s\varphi}$ ($\varphi = a, b, c$) denotes the three-phase line resistors; L_o is the arm filter inductor; R_s is the single-phase line resistor; L_1 and L_2 are the single-phase filtering inductors; C_2 is the single-phase filtering capacitor; U_{tdc} is the intermediate DC capacitor voltage; and i_{tdc} is the intermediate DC current. The LC filter which includes an inductor L and a capacitor C on the DC side is used to filter the secondary ripple of the intermediate DC capacitor C_1 to avoid the impact of the secondary ripple on the three-phase and single-phase power grids. To facilitate the analysis, four half-bridge SMs are installed in each arm of one phase leg. SMφ1 to SMφ4 ($\varphi = a, b, c$) are in the upper arm; and SMφ5 to SMφ8 are in the lower arm. Each SM is comprised of two switching devices $S_{\varphi x1}$, $S_{\varphi x2}$ ($x = 1, 2, \ldots, 8$) and one capacitor. $u_{C\varphi x}$ denotes the voltages of eight capacitors.

To each SM, there are two types of two-level voltage output.

1) $S_{\varphi x1} = 1$ and $S_{\varphi x2} = 0$, SM is on.

2) $S_{\varphi x1} = 0$ and $S_{\varphi x2} = 1$, SM is off.

To guarantee the basic operation of the three-phase MMC, the DC-side voltage should be controlled to be stable by providing the active power. In addition, the reactive power should be controlled to be zero in order to block any reactive power injected back into the three-phase grid and ensure that the ACTPS system can be operated under the unity power factor condition. The equivalent circuit and the control block diagram are shown in Fig. 2 [37]. This part of control is relatively mature and the specific derivation is shown in the Supplementary Materials. In addition, the definitions of variables in Fig. 2 are give in the Supplementary Materials. Hence, in this paper, the main characteristic of the ACTPS system focuses on its grid-connected single-phase MMC side. In order to remove NSs among all SSs and connect directly the electrical lines between two different SSs, the voltage outputs by different SSs should be controlled to be identical. What's more, for the sake of compensating reactive and harmonic power and feeding the locomotive traction loads, different kinds of power should be provided flexibly from the single-phase MMC to the locomotive traction loads.

As discussed hereinbefore, two tasks should be finished.

1) Obtain controlled amplitude, phase angle, and frequency of output voltage.

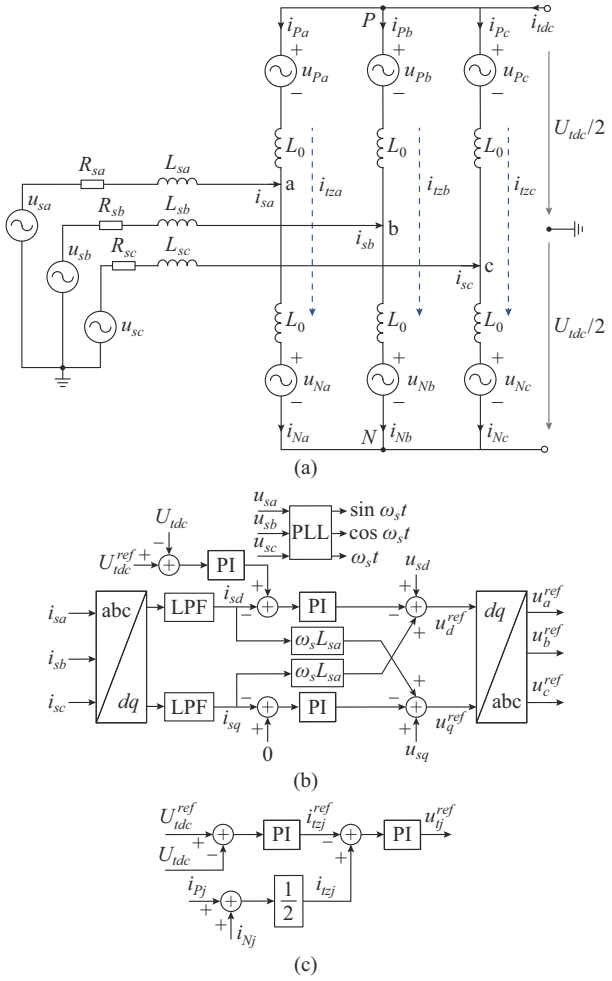


Fig. 2. Equivalent circuit and relevant control block of three-phase MMC. (a) Equivalent circuit. (b) Three-phase decoupling control strategy. (c) Voltage stabilization control strategy.

2) Provide the arbitrary amount of reactive and active power to traction locomotives.

Figure 3(a) shows the equivalent circuit of single-phase MMC connected to the traction network [15], where U_{sdc} and i_{sdc} are the single-phase DC-side voltage and DC-side current in single-phase MMC, respectively; i_{Pj} and i_{Nj} are the upper-arm and lower-arm currents in single-phase MMC, respectively; u_j is the leg voltage in single-phase MMC; i_{szj} is the single-phase circulating current; and $j = l, r$ is the index of leg. With respect to Fig. 3(a), four half-bridge SMs are installed in each arm of one phase leg either, where SMj1 to SMj4 are installed in the upper arm; and SMj5 to SMj8 are installed in the lower arm. With respect to Fig. 3(a), the single-phase voltage source, single-phase AC current, and leg port voltage are defined as:

$$\begin{cases} u_s(t) = U_s \sin \omega_s t \\ i_s(t) = I_d \sin \omega_s t + I_q \cos \omega_s t \\ u_{lr}(t) = U_d \sin \omega_s t + U_q \cos \omega_s t \end{cases} \tag{1}$$

where $u_{lr} = u_l - u_r$ is the port voltage in single-phase MMC, and U_d and U_q are its DC components in d and q axes, respectively; U_s is the amplitude of single-phase voltage; I_d and I_q are the amplitudes of the active and reactive instanta-

neous currents, respectively; and ω_s is the single-phase angular frequency. Furthermore, to make sure the normal operation of the single-phase inverter, the following two steps are included.

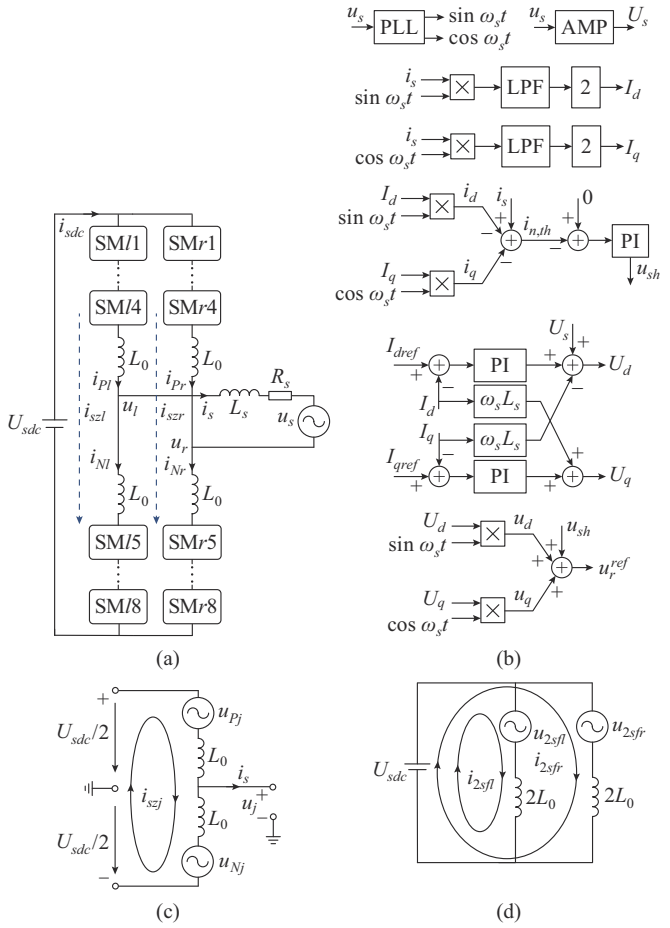


Fig. 3. Equivalent circuit and relevant control control strategy of single-phase MMC. (a) Equivalent circuit. (b) Single-phase decoupling control strategy. (c) Equivalent circuit of circulating currents flowing between upper arm and lower arm. (d) Equivalent circuit of circulating currents flowing between two legs.

1) Step 1: Establishing Optimized d-q Decoupled Mathematical Model

Applying Kirchhoff voltage law (KVL) to the topology in Fig. 3(a), it is obtained that

$$u_{lr}(t)=u_s(t)-R_s i_s(t)-L_s \mathrm{d}i_s(t)/\mathrm{d}t \tag{2}$$

where L_s is the equivalent filter inductance defined as L_1+L_2. The *d-q* mathematical mode of this topology is obtained by substituting (1) into (2).

$$\begin{cases} U_d=U_s-\omega_s L_s I_q-(R_s-L_s p)I_d \\ U_q=\omega_s L_s I_d-(R_s-L_s p)I_q \end{cases} \tag{3}$$

where p is the differential factor.

Based on (3), U_d and U_q consist of three components and two components, respectively. The feedforward decoupling method is adopted to enable I_d and I_q to be controlled independently [38]. Formula (3) is rewritten as:

$$\begin{cases} U_d=U_s-\omega_s L_s I_q+\left(k_p+\dfrac{k_i}{s}\right)(I_{dref}-I_d) \\ U_q=\omega_s L_s I_d+\left(k_p+\dfrac{k_i}{s}\right)(I_{qref}-I_q) \end{cases} \tag{4}$$

where k_p and k_i are the gains of proportional-integral (PI) controller; and I_{dref} and I_{qref} are the reference values of I_d and I_q, respectively. The design and stability analysis of the current controller are included in the Supplementary Materials.

2) Step 2: Detecting Different Types of Currents

Assuming that AC current is comprised of three components, i.e.,

$$i_s(t)=i_d(t)+i_q(t)+i_h(t)=I_d\sin\omega_s t+ I_q\cos\omega_s t+\sum_{n=2}^{\infty}I_h\sin(\omega_s t+\phi_n) \tag{5}$$

where $i_d(t)$ and $i_q(t)$ are the instantaneous active and reactive currents, respectively; $i_h(t)$ is the harmonic component of $i_s(t)$, and I_h and ϕ_n are its amplitude and initial angle, respectively; and n is the harmonic order. In order to obtain the active current, a new variable $i_\alpha(t)$ is defined as:

$$i_\alpha(t)=i_s(t)\sin\omega_s t=\frac{I_d}{2}(1-\cos 2\omega_s t)+\frac{I_q}{2}\sin 2\omega_s t+ \sum_{n=2}^{\infty}\frac{I_n}{2}(\cos((n-1)\omega_s t+\phi_n)-\cos((n+1)\omega_s t+\phi_n))=\frac{I_d}{2}+i_{pj} \tag{6}$$

where I_n and i_{pj} are the n^{th} harmonic current and the AC component of $i_\alpha(t)$, respectively.

Subsequently, $i_\alpha(t)$ is passed through a low-pass filter (LPF) with a cut-off frequency of $\omega_s/(2\pi)$ to obtain $I_d/2$. Hence, the active instantaneous current $i_d(t)$ can be generated by I_d multiplying by $\sin\omega_s t$.

Similar to the aforementioned condition, the reactive current can be obtained by introducing a new variable $i_\beta(t)$ defined as:

$$i_\beta(t)=i_s(t)\cos\omega_s t=\frac{I_q}{2}(1+\cos 2\omega_s t)+\frac{I_d}{2}\sin 2\omega_s t+ \sum_{n=2}^{\infty}\frac{I_n}{2}(\cos((n-1)\omega_s t+\phi_n)-\cos((n+1)\omega_s t+\phi_n))=\frac{I_q}{2}+i_{qj} \tag{7}$$

where i_{qj} is the AC component of $i_\beta(t)$.

Similarly, $i_\beta(t)$ is passed through an LPF with a cut-off frequency of $\omega_s/(2\pi)$ to obtain $I_q/2$. Therefore, the reactive instantaneous component $i_q(t)$ is obtained by I_q multiplying by $\cos\omega_s t$.

Finally, the n^{th} harmonic current component $i_{n,th}(t)$ can be derived by:

$$i_{n,th}(t)=i_s(t)-i_d(t)-i_q(t) \tag{8}$$

Based on (1) - (8), the overall control diagram of single-phase inverter is given in Fig. 3(b), where u_{sh} is the voltage reference for harmonic current suppression; u_r^{ref} is the total voltage reference for power control; and u_d and u_q are the active and reactive components of u_r^{ref}, respectively. To achieve the independent control of the active power and reactive power, an optimized control strategy including two control

loops, i.e., active and reactive power control loops, is proposed. Based on the proposed control strategy, the single-phase current i_s is multiplied by $\cos\omega_s t$ and $\sin\omega_s t$ from the phase-locked loop (PLL) to obtain active current and reactive current $i_d(t)$ and $i_q(t)$, respectively. Subsequently, two LPFs are utilized to filter high-frequency components. The DC active and reactive current components I_d and I_q remain. According to (4), U_d and U_q are derived from the output of PI controllers. The harmonic component $i_{n.th}$ is obtained from (8) and regulated to zero by PI controller. Obviously, an arbitrary amount of active power and reactive power can be provided by the proposed control strategy.

III. AC Frequency-double Circulating Current Minimization and SM Capacitor Voltage Balancing

A. AC Circulating Current Minimization

The three-phase circulating current minimization is mature and the derivation is shown in the Supplementary Materials. Similar to the three-phase system, there is also a frequency-doubled circulating current on the single-phase MMC. Assuming that the path and direction of the circulating current are shown in Fig. 3(a). According to KVL, we have

$$\begin{cases} \dfrac{U_{sdc}}{2} = u_{Pj} + L_0\dfrac{\mathrm{d}i_{Pj}}{\mathrm{d}t} + u_j \\ \dfrac{U_{sdc}}{2} = u_{Nj} + L_0\dfrac{\mathrm{d}i_{Nj}}{\mathrm{d}t} - u_j \end{cases} \tag{9}$$

where u_{Pj} and u_{Nj} are the upper-arm and lower-arm voltages in single-phase MMC, respectively.

The flowing direction of the common-mode current is shown in the equivalent circuit in Fig. 3(c). We assume that

$$\begin{cases} u_{szj} = L_0\dfrac{\mathrm{d}i_{szj}(t)}{\mathrm{d}t} \\ i_s(t) = I_s\sin(\omega_s t + \varphi_s) \end{cases} \tag{10}$$

where u_{szj} is the common-mode voltage in single-phase MMC; and I_s and φ_s are the amplitude and the initial angle of $i_s(t)$, respectively. Subsequently, in the single-phase MMC, $i_{szj}(t)$ can be expressed as:

$$i_{szj}(t) = \frac{I_{sdc}}{2} + i_{2sfj}(t) = \frac{I_{sdc}}{2} + I_{2sfj}\sin(2\omega_s t + \theta_{2sfj}) \tag{11}$$

where I_{sdc} is the DC component of i_{sdc}; and $i_{2sfj}(t)$ is the frequency-double circulating current of single-phase MMC, and I_{2sfj} and θ_{2sfj} are its amplitude and initial angle, respectively.

Based on Fig. 3, we have

$$\begin{cases} u_{Pl} = u_{Nr} \\ u_{Pr} = u_{Nl} \\ i_{Pl} = i_{Nr} \\ i_{Pr} = i_{Nl} \end{cases} \tag{12}$$

According to (10)-(12), the instantaneous upper- and lower-arm currents in single-phase MMC are obtained as:

$$\begin{cases} i_{Pl}(t) = i_{Nr}(t) = \dfrac{I_{sdc}}{2} - \dfrac{I_s}{2}\sin(\omega_s t + \varphi) + I_{2sfl}\sin(2\omega_s t + \theta_{2sfl}) \\ i_{Nl}(t) = i_{Pr}(t) = \dfrac{I_{sdc}}{2} + \dfrac{I_s}{2}\sin(\omega_s t + \varphi) + I_{2sfl}\sin(2\omega_s t + \theta_{2sfl}) \end{cases} \tag{13}$$

Hence, the DC-link instantaneous power $P_{sdc}(t)$ can be expressed as:

$$P_{sdc}(t) = U_{sdc}i_{sdc} = U_{sdc}I_{sdc} + 2U_{sdc}I_{2sfl}\sin(2\omega t + \theta_{2sfl}) \tag{14}$$

Based on (13) and (14), the characteristic of the single-phase MMC is concluded as follows.

1) AC frequency-double circulating current just flows through the DC-link voltage to form a loop, as shown in Fig. 3(d), where u_{2fsj} is the frequency-double component of two arm voltages.

2) The arm current and DC-link instantaneous power will be distorted by the instantaneous AC frequency-double circulating current.

Conducting static coordinate transform to (28) in [15] and taking leg l as an example, we have

$$\begin{cases} u_{sz\alpha} = L_0\dfrac{\mathrm{d}i_{2sfl\alpha}}{\mathrm{d}t} \\ u_{sz\beta} = L_0\dfrac{\mathrm{d}i_{2sfl\beta}}{\mathrm{d}t} \end{cases} \tag{15}$$

where u_{szk} and i_{2sflk} ($k=\alpha,\beta$) are the α- and β-axis values corresponding to u_{szl} and i_{2sfl}, respectively.

Furthermore, (15) can be transformed into d-q coordinate system to obtain the DC common-mode voltage components of frequency-double currents, which are expressed as:

$$\begin{cases} u_{szd} = L_0\dfrac{\mathrm{d}i_{2sfd}}{\mathrm{d}t} - 2\omega_s L_0 i_{2sfd} \\ u_{szq} = L_0\dfrac{\mathrm{d}i_{2sfq}}{\mathrm{d}t} + 2\omega_s L_0 i_{2sfq} \end{cases} \tag{16}$$

where u_{szv} and i_{2sfv} ($v=d,q$) are the d- and q-axis values corresponding to u_{szl} and i_{2sfl}, respectively.

As aforementioned, i_{2sfl} can be obtained from the common-mode current i_{szl} through the band-pass filter (BPF) as well. In order to finish the coordinate transformer, a virtual component $i_{sz\beta}$ lagging 90° with respect to $i_{sz\alpha}$ is introduced to achieve the following expression.

$$i_{2sfl\alpha} = I_{2sfl}\sin(2\omega_s t + \theta_{2sf}) i_{2sfl\beta} = i_{2sfl\alpha}\mathrm{e}^{-\mathrm{j}\pi/2} = I_{2sfl}\sin\left(2\omega_s t + \theta_{2sf} - \frac{\pi}{2}\right) \tag{17}$$

Similarly, $i_{2sfl\alpha}$ and $i_{2sfl\beta}$ will be transformed to be the DC variables, and i_{2sfd} and i_{2sfq} are regulated to approximate their reference values, i.e., i_{2sfdr} and i_{2sfqr}, by PI controllers.

The overall AC frequency-double circulating current mitigation control scheme of three-phase MMC and single-phase MMC is shown in Fig. 4, where $u_{tz\varphi}^{ref}$ ($\varphi=a,b,c$) and u_{szk}^{ref} ($k=\alpha,\beta$) are the voltage references of three-phase circulating current controller and single-phase circulating current controller, respectively. In addition, the definitions of variables in Fig. 4 (a) are shown in the Supplementary Materials. In Fig. 4, the three-phase AC frequency-double circulating currents i_{2tfa}, i_{2tfb}, and i_{2tfc} are measured and transformed by a negative-sequence matrix to derive the DC circulating current components, i.e., i_{2tfd} and i_{2tfq}. The obtained DC circulating current components are regulated by PI controllers to approximate the reference values. A similar conclusion holds for single-phase AC frequency-double circulating currents.

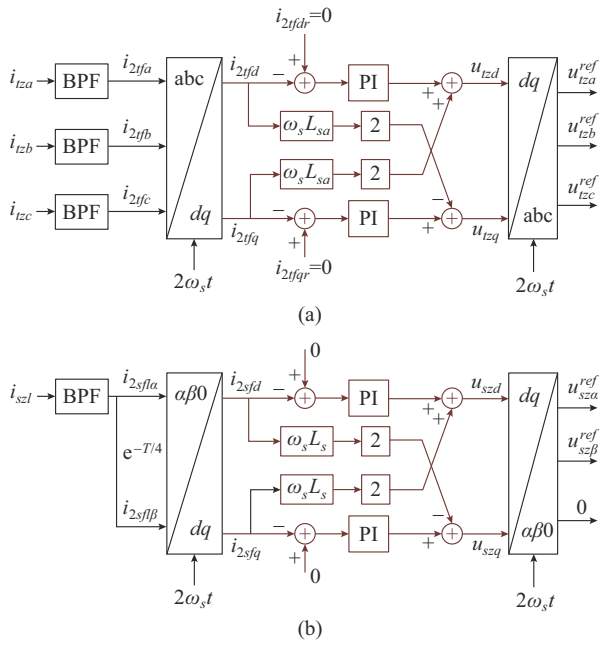


Fig. 4. AC frequency-double circulating current mitigation control scheme. (a) Three-phase MMC. (b) Single-phase MMC.

B. SM Capacitor Voltage Balancing Algorithm

The aspect of SM capacitor voltage balancing of MMC is not the focus of this paper. Hence, combined with the sine wave pulse width modulation (SPWM) method that determines the level number of the MMC, a strategy that sorts and selects SMs to be bypassed or inserted according to arm current direction is adopted in this paper [19], [37].

As aforementioned, the overall control strategy of the MMC-ACTPS system is comprised of three-phase closed-loop control, voltage stabilization, strategy for three-phase and single-phase AC frequency-double circulating current mitigation, SM voltage balance sorting algorithm, and single-phase optimized grid-connected control strategy.

IV. Digital Implementation of Control System

A. Overall Architecture of Control System

The overall architecture of the control system is depicted in Fig. 5, where the definition of the variables are attached in the Supplementary Materials.

The ADC SM collects voltage and current analog signals and converts them into 12-bit digital signals, ranging from –2048 to 2047. The digital signals of these voltages and currents enter the three-phase controller and the single-phase controller, and the output signals are modulated waves. When the amplitude is 2047, the corresponding modulation index is 1. The driving signal of the switch can be obtained through the modulation SM. In addition, an SysFSM SM is a state machine that can control the start and stop of the system. The implementation of the state machine is shown in the Supplementary Materials. The protection SM can block the driving signal in time in case of abnormal voltage or current to avoid system damage.

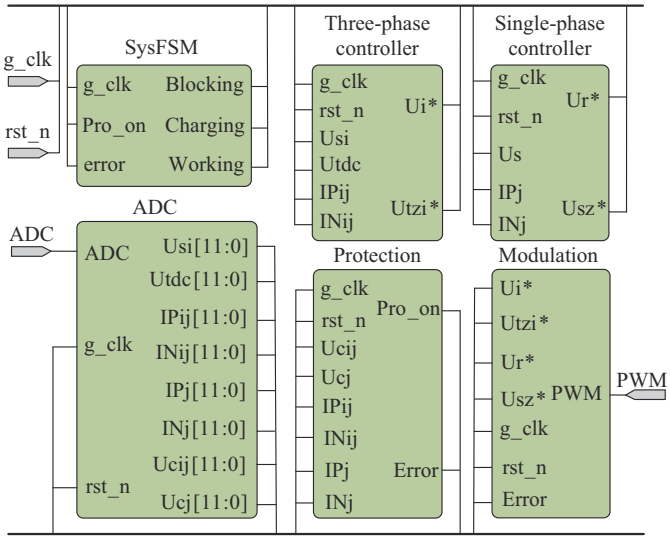


Fig. 5. Overall architecture of control system.

B. Three-phase Controller

The corresponding hardware architecture of three-phase controller in the register transfer level is designed, as shown in Fig. 6(a), where the definition of the variables are attached in the Supplementary Materials. The multiplier is obtained by shifting to the right. The integral term of the PI controller adopts the method of expanding the bit width. Figure 6(b) shows the Verilog code of the PI controller and the final output of the PI controller, where the larger the KI_WIDTH, the smaller the value after intercepting the upper 13 bits. The D flip-flop is used to delay the signal to ensure the synchronization of each operand.

A time division multiplexing method called the folding technique is used, where multiple algorithm operations (such as multiplication and addition operations) are arranged to share a single functional hardware unit (such as a pipelined multiplier and adder). By executing multiple operations on a single functional unit, the number of hardware implementations is reduced significantly.

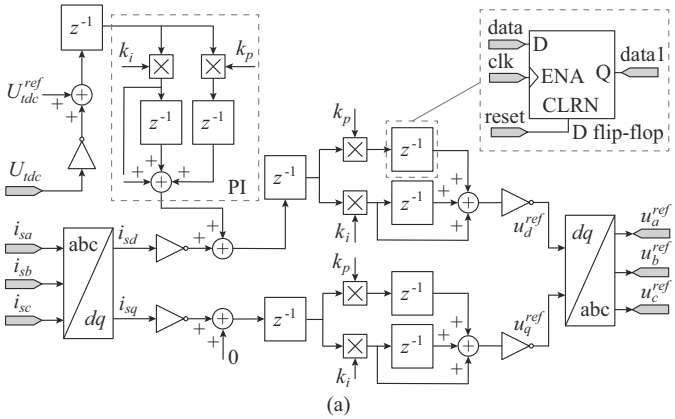
The structure of three-phase circulating current suppression is shown in Fig. 7. The program design process is the same as that in Fig. 6(a), and it will not be analyzed here. The bandwidth of the BPF is 40 Hz and can retain signals from 80 Hz to 120 Hz. The 100 Hz component in i_{szl} can be obtained through this BPF.

C. Single-phase Controller

The architecture-based implementation of single-phase controller is shown in Fig. 8(a). An LPF is used to filter out the pulsation signal in the product of i_s and $2\sin\omega_s t$, as shown in (6). A second-order filter is used, and the Verilog code is shown in Fig. 8(b). The filter is equivalent to a process of multiplication and accumulation.

The architecture-based implementation of single-phase circulating current suppression is shown in Fig. 9.

Compared with three-phase circulating current suppression, a long time delay needs to be used to obtain the active and reactive components of single-phase circulating current. In Fig. 9, the number of delayed clock cycles n_c can be obtained as:



(a)

```
wire error <= TARGET-{iData[11], iData};
wire [KI_WIDTH-1:0] error_KI;
assign error_KI = {{(KI_WIDTH-13){error[12]}}, error};
always @ (posedge g_clk or negedge rst )
begin
if (rst == 1'b0)
begin
Ki_reg <= {(KI_WIDTH-1){1'b0}};
Kp_result <= {13{1'b0}};
PI_output <= {13{1'b0}};
end
else
begin
Kp_result <= {{KP_RS_BIT{error[12]}}, error[12:KP_RS_BIT]};
if ( ( !error_KI[KI_WIDTH-1] && !Ki_reg[KI_WIDTH-1] ) )
Ki_reg <= Ki_reg;
end
else
Ki_reg <= Ki_reg + error_KI;
PI_output <= Kp_result + Ki_reg[KI_WIDTH-1:KI_WIDTH-13];
end
```

(b)

Fig. 6. Architecture and Verilog code of three-phase controller. (a) Folding architecture-based implementation of three-phase controller. (b) Verilog code of PI controller.

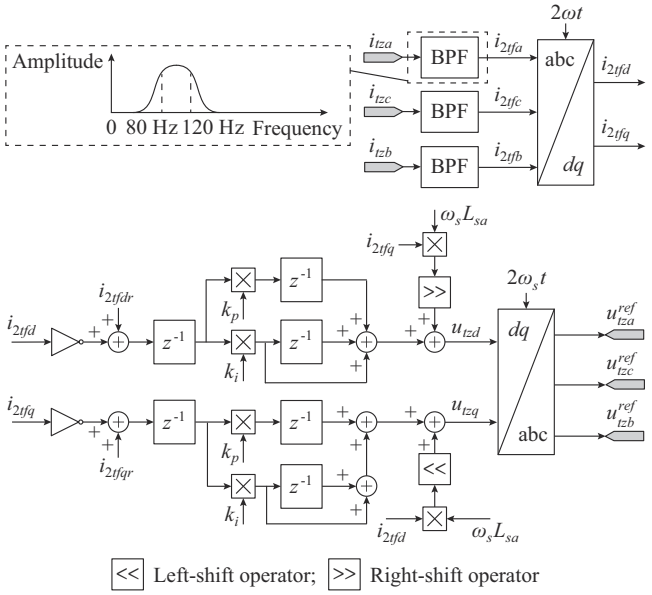
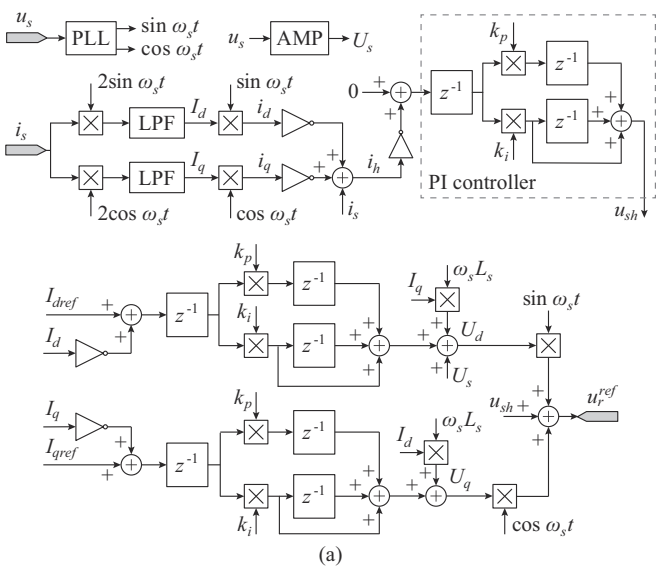


Fig. 7. Folding architecture-based implementation of three-phase circulating current suppression.



(a)

```
always @ (posedge clk or negedge rst_n) begin
if (rst_n == 1'b0) begin
din_r1 <= 0; din_r2 <= 0; din_r3 <= 0;
end
else begin
din_r1 <= din; din_r2 <= din_r1; din_r3 <= din_r2;
end
end
always @ (posedge clk or negedge rst_n) begin
if (rst_n == 1'b0) begin
mul_data1 <= 0; mul_data2 <= 0;
end
else begin
mul_data1 <= (din_r1 + din_r3) >> COEFF1;
mul_data2 <= din_r2 >> COEFF2;
end
end
assign dout = mul_data1 + mul_data2;
```

(b)

Fig. 8. Architecture and Verilog code of single-phase controller. (a) Architecture-based implementation of single-phase controller. (b) Verilog code of LPF.

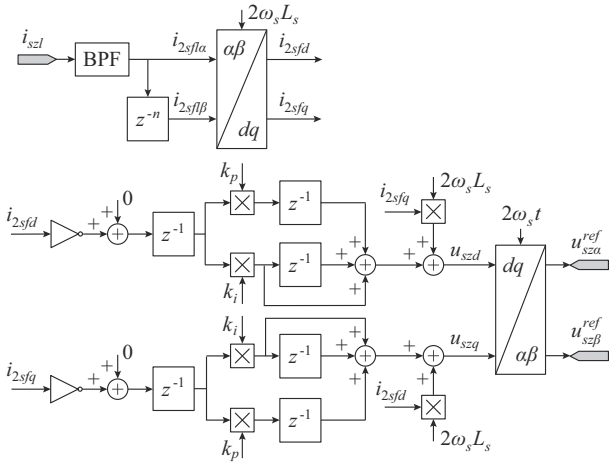


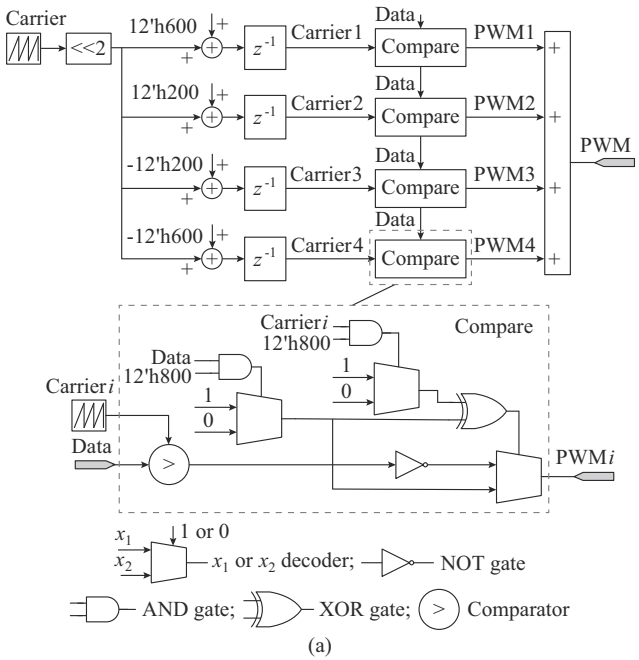
Fig. 9. Architecture-based implementation of single-phase circulating current suppression.

$$n_c = \frac{g\_clk}{0.25 f_c} = \frac{30 \times 10^6}{400} = 75000 \tag{18}$$

where *g_clk* is the system clock frequency; and f_c is the circulating current frequency.

D. Modulation

The carrier disposition pulse width modulation (CDPWM) is adopted in this paper. The architecture-based implementation of CDPWM is shown in Fig. 10(a). The input of this part is the modulated wave which is represented as data in Fig. 10(a), and the output is represented as PWM which means the number of SMs that need to be turned on for each bridge arm, i. e., PWM*i* is the comparison result between data and carrier*i* ($i=1,2,3,4$). The Verilog code that generates four carriers is shown in Fig. 10(b). Since the carrier signal (trig_data_wire) is 12 bits, its range is –2048 to 2047. Each bridge arm has four SMs, so four carriers need to be generated as trig_data*i* ($i=1,2,3,4$), which corresponds to carrier*i* ($i=1,2,3,4$) in Fig. 10(a). The range of trig_data is –512 to 512, and the normalized value is –0.25 to 0.25. trig_data1 is the uppermost carrier, ranging from 1024 to 2047, and the normalized value is 0.5 to 1.



(a)

```
wire [11:0] trig_data_wire, trig_data; //–2048-2047
assign trig_data = {{trig_data_wire[11]}, {trig_data_wire[11]},
                    {trig_data_wire[11:2]}};
reg [11:0] trig_data1, trig_data2, trig_data3, trig_data4;
always @ (posedge g_clk) begin
if (rst_n == 1'b0) begin
trig_data1 <= 12'b0; trig_data2 <= 12'b0;
trig_data3 <= 12'b0; trig_data4 <= 12'b0;
end
else begin
trig_data1 <= trig_data + 12'd1536; //1024-2047
trig_data2 <= trig_data + 12'd512; //0-1023
trig_data3 <= trig_data – 12'd512; //-1024-1
trig_data4 <= trig_data – 12'd1536; //-2048-1025
end
end
```

(b)

Fig. 10. Architecture and Verilog code of CDPWM. (a) Architecture-based implementation of CDPWM. (b) Verilog code of carrier generator.

The traditional sorting algorithms sort all SM voltages in one sorting cycle. Hundreds of SMs are needed in practical application. The traditional sorting algorithms take a long time and are computationally intensive. If the sorting time is too long, the voltage of each SM will be unbalanced, resulting in system instability. When each arm has N SMs, the number of comparison times is expressed as:

$$n_{sort}=\frac{N(N-1)}{2} \tag{19}$$

To reduce the sorting time, an improved sorting algorithm is proposed. The steps are as follows.

1) N SMs are divided into k groups, defined as $U_i, i=1,2,\ldots,k$. The number of SMs per group is t and $N=kt$.

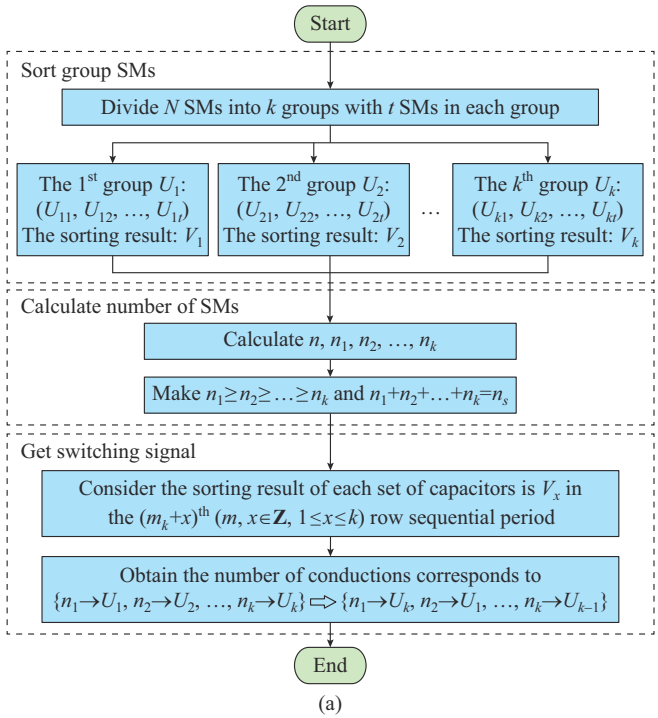
2) The i^{th} sorting cycle sorts the i^{th} group of SMs, and the sorting result is defined as V_i, and all group sorting results are considered as V_i.

3) The number of conducting SMs per arm is defined as n_s, as shown in Fig. 11(a). The number of conducting SMs in each group meets (20).

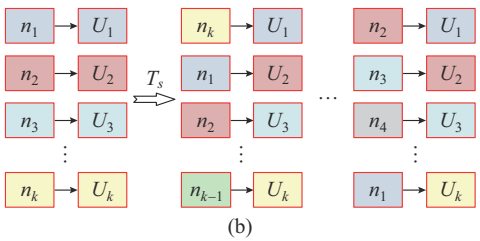
$$\begin{cases} n_1 \geq n_2 \geq \ldots \geq n_k \\ n_1+n_2+\ldots+n_k=n_s \end{cases} \tag{20}$$

where n_i ($i=1,2,\ldots,k$) is the number of conducting SMs in the i^{th} group.

4) The method of dividing the number of SMs in each group is shown in Fig. 11(b).



(a)



(b)

Fig. 11. Improved sorting algorithm. (a) Flowchart for improved sorting algorithm. (b) Number of SMs per group.

After these four steps, the sorting can be completed in a shorter time. The number of comparison times is shown as:

$$n_{sort} = \frac{N}{2}\left(\frac{N-k}{k^2}\right) \tag{21}$$

Assuming $N=40$, the relationship between the number of groups k and the number of comparisons n_{sort} is shown in Table I. As can be observed in Table I, the more groups there are, the fewer comparisons are required. When $k=1$, the number of comparisons is consistent with the traditional sorting algorithm. Compared with the traditional sorting algorithm, the improved sorting algorithm can reduce the computational burden by more than 90% when $k=5$.

TABLE I
NUMBER OF COMPARISON TIMES WITH DIFFERENT k

k	n_{sort}
1 (traditional)	780
2	190
4	45
5	28

V. SIMULATION AND EXPERIMENTAL RESULTS

The simulation results and the description of experimental prototype are included in the Supplementary Materials, and the parameters are shown in Table II. The proposed algorithms are totally coded using Verilog-HDL, synthesized using Quartus II, and programmed onto the FPGA controller EP3C55F484C8, and the modulating signals are transferred through the I/O board to fibers and drive the switching devices.

TABLE II
EXPERIMENTAL PARAMETERS

Parameter	Value	Parameter	Value
N_1	65 V/65 V	L_0	0.5 mH
U_s	60 V	C_1	470 μF
N_2	60 V/60 V	C_2	2.2 mF
U_{tdc}	120 V	f_z	5 kHz
L_{sa}, L_{sb}, L_{sc}	5 mH	IGBT model	IHW20N120R
L_1, L_2	15 mH	FPGA model	EP3C55F484C8

Note: N_1 and N_2 are the ratios of primary and secondary transformers, respectively.

To further verify the capability in regulating any kind of power for the proposed algorithm in Fig. 3(b), the power transfer experimental verification of the MMC-ACTPS system at a steady state has been performed. In Fig. 12(a), when the active power command is not enabled, it still outputs a little amount of currents i_{sa} and i_s in the three-phase MMC and single-phase MMC to compensate for the power loss of phase legs, respectively. Once the active power command is given, the currents i_{sa} and i_s are generated and they are in phase with the voltages u_{sa} and u_s, which reflect the minimization of the AC circulating currents, as shown in Fig. 12(b).

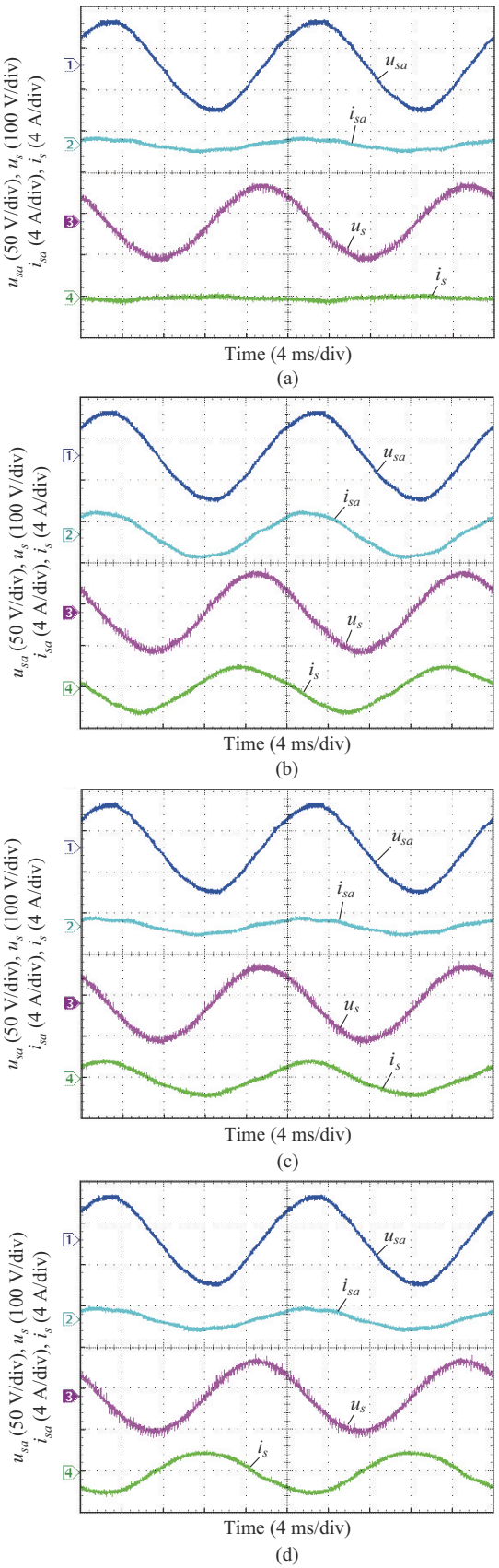


Fig. 12. Experimental verification in power delivery capability. (a) Waveforms under light load in active power delivery mode. (b) Waveforms under medium load in active power delivery mode. (c) Waveforms under light load in inductive reactive power delivery mode. (d) Waveforms under medium load in capacitive reactive power delivery mode.

An inductive reactive power delivery mode and a capacitive reactive power delivery mode when reactive power command is enabled are shown in Fig. 12(c) and (d), respectively. In the inductive mode, AC current lags the AC voltage by 90°. Besides, AC voltage lags the AC current by 90° when the capacitive mode is operated. Figure 12 confirms the capability of the proposed strategy in regulating any kind of power.

Figure 13 demonstrates the proposed strategy for handling a sharp load change of the ACTPS system. With respect to Fig. 13(a), the ACTPS system is operated normally within the time interval [0, 1]s. After 1 s, a sharp load is removed and the system can still be operated stably. Similarly, as shown in Fig. 13(b), within the time interval [0, 2.5]s, the ACTPS system is operated under a no-load condition. After 2.5 s, a sharp load is enabled, and the system experiences a short period to the adjusted process and then to be a stable state by the proposed control strategy.

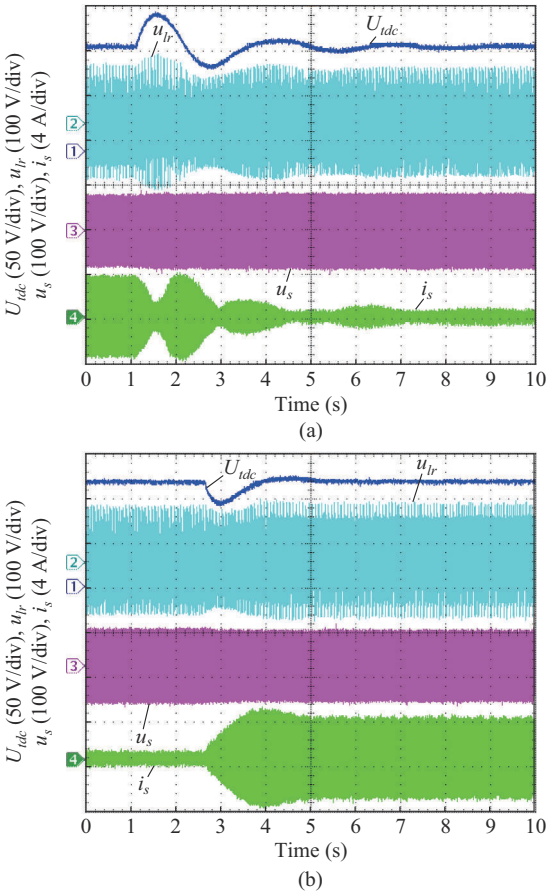


Fig. 13. Experimental verification in dynamic power delivery capability. (a) Waveform of dynamic process from a sharp load condition to a no-load condition. (b) Waveform of dynamic process from a no-load condition to a sharp load condition.

The AC frequency-double circulating current mitigation scenarios are shown in Fig. 14(a) and (b). With respect to Fig. 14(a), the amplitude of AC frequency-double circulating current will be reduced once the proposed circulating current mitigation strategy is enabled. Similarly, the opposite process is presented in Fig. 14(b). The total loss of the ACTPS system includes the conduction losses and switching losses of IGBTs, the conduction losses and switching losses of freewheeling diodes, the core losses and winding losses of inductors, and the losses of capacitors. The power loss analysis of the ACTPS system is included in the Supplementary Materials.

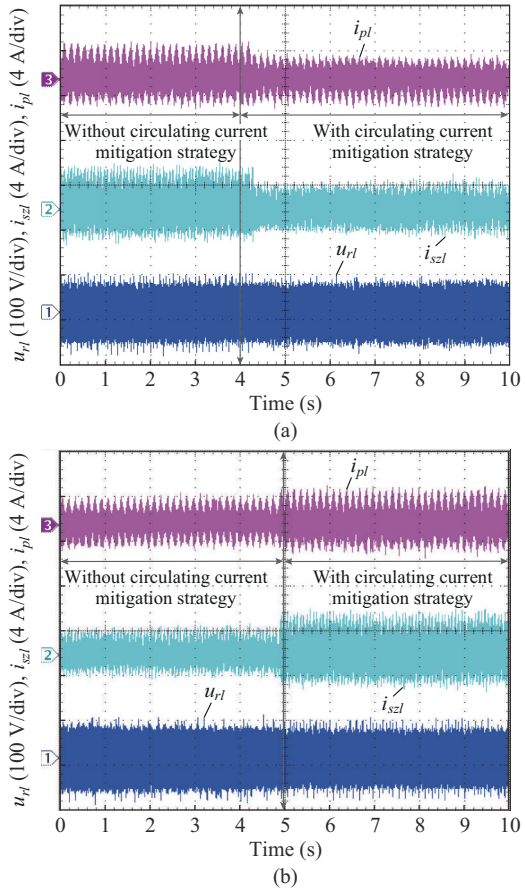


Fig. 14. Circulating current waveforms. (a) Circulating current from without circulating current mitigation strategy to with circulating current mitigation strategy. (b) Circulating current from with circulating current mitigation strategy to without circulating current mitigation strategy.

Table III presents FPGA resource utilization, where the numbers of logic elements (LEs), look-up-table (LUT), register LCs, and LUT/Reg LCs on chips are tabulated by entities. The entire control system requires 5463 LEs, around 10% of total LEs of one medium density FPGA device EP3C55F484C8.

TABLE III
FPGA Resource Utilization

SM	Number			
	LE	LUT	Register LCs	LUT/Reg LCs
ADC	476	160	98	218
Single-phase controller	2480	0	0	19
Three-phase controller	1850	694	453	703
Modulation	574	283	3	286
SysFSM	157	60	1	96
Protection	356	127	24	205
Total	5463	1324	479	1267

As shown in Fig. 5, the control system consists of six SMs. The time delay of the proposed strategy is shown in Fig. 15. The system clock frequency is 30 MHz, the ADC sampling frequency is 35 kHz, the PWM frequency is 10 kHz, and the switching frequency is 5 kHz.

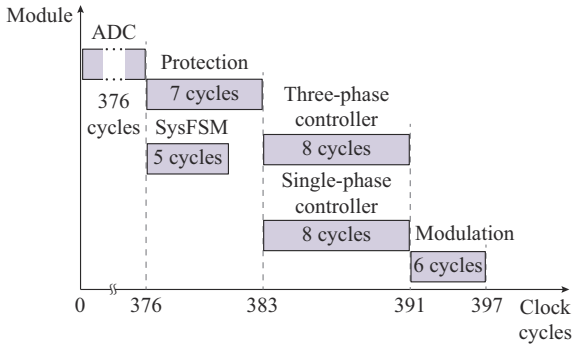


Fig. 15. Time delay analysis of proposed strategy.

The ADC SM needs 376 clock cycles to collect the grid voltage, capacitor voltage, and grid current, which depend on the ADC sampling frequency. If the high-speed AD chip is used, the time delay of the ADC SM will be greatly reduced. The voltage and current signals are transmitted to the protection SM and the state machine SM, and the time delay is 7 clock cycles and 5 clock cycles, respectively. Then, the time delays of the three-phase controller and single-phase controller are both 8 clock cycles. Finally, the time delay of the modulation SM is 6 clock cycles. The overall time delay is 397 clock cycles, i.e., 13 μs, which is applicable to switching frequencies below 75 kHz. From the perspective of time delay, only 14 clock cycles are required for the controller and modulation, i.e., 0.46 μs. If the ADC sampling frequency is high enough, the switching frequency can be MHz theoretically.

The comparison of the proposed strategy and existing ones is shown in Table IV. In [10], [30]-[32], DSP + FPGA is used as the processor, resulting in a complex system because the communication between DSP and FPGA is required. And the current totoal harmonic distortion (THD) is higher than the proposed strategy. References [33], [35], and [36] use DSpace as the processor, which is expensive (about ¥20000) and not suitable for practical applications. From the point of view of the sorting algorithm, the grouping sorting algorithm is only used in this paper. Other studies use traditional sorting algorithms, which take a long time to sort and cannot be applied when there are many SMs. From the perspective of time delay, the operation time of the proposed strategy is only 13 μs, while that of [31] is 62.5 μs, and that of [35] is 78 μs. A shorter operation time can accommodate scenarios with more SMs. On the other hand, EP3C55F484C 8 has 327 I/Os, which can meet the application requirements of dozens of SMs under high-voltage conditions. In general, the proposed strategy has low cost, less resource utilization and time delay, and low current THD, and it is suitable for practical application.

TABLE IV
COMPREHENSIVE COMPARISON OF PROPOSED STRATEGY AND EXISTING ONES

Reference	Current THD (%)	Switching frequency (kHz)	Comparison times	Circulation mitigation	Processor	Time delay (μs)	I/O
[31]	≤5.86	19.55	$N(N-1)/2$	√	DSP + FPGA	62.5	138
[32]	≤4.2	0.45	$N(N-1)/2$	√	DSP + FPGA	-	-
[30]	≤4.8	2.50	$N(N-1)/2$	√	DSP + FPGA	-	232
[10]	≤7.8	10.00	$N(N-1)/2$	√	DSP + FPGA	-	-
[33]	-	1.50	$N(N-1)/2$	-	DSPACE	-	-
[35]	≤2.37	5.00	$N(N-1)/2$	√	DSPACE	78.0	-
[36]	-	10.00	$N(N-1)/2$	√	DSPACE	-	-
Proposed	≤3.8	5.00	$N(N-k)/(2k^2)$	√	FPGA	13.0	327

Note: "-" represents "not provided".

VI. CONCLUSION

In this paper, a flexible energy transmission control strategy is analyzed for the MMC-ACTPS system based on the mathematical model of the single-phase MMC. Moreover, a negative sequence based AC frequency-double circulating current mitigation strategy is designed to effectively suppress the AC frequency-double circulating currents. To reduce resource occupation and operation time, a digital implementation scheme based on the FPGA of the proposed strategy is proposed. The program design of the controller and the modulation are presented. Aiming at the problem of long sorting time when the number of SMs is large, an improved sorting algorithm is proposed. Finally, the effectiveness of the proposed control strategy is confirmed by the simulation and experimental results. The conducted studies are summarized as follows.

1) The proposed strategy can flexibly regulate the active and reactive power transferred from the single-phase traction grid to the traction loads through the ACTPS system without affecting the three-phase MMC.

2) The operation time of the proposed strategy in this paper is only 13 μs which is about one-fifth of the existing methods. The THD of power grid current is less than 3.8%, suitable for grid connection applications.

3) An improved sorting algorithm is proposed, which can reduce the sorting time especially when there are many SMs. By grouping comparison, the sorting time can be reduced more than 90%, and it is easy to expand to more SMs.

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Jiangpeng Yang received the B.S. degree in electrical engineering and automation from Shenyang University of Technology, Shenyang, China, in 2019. He is currently working toward the Ph.D. degree in electrical engineering at Southwest Jiaotong University, Chengdu, China. His research interests include modulation and control techniques of multiport converter and the control techniques of unified power quality conditioner.

Hongjian Lin received the Ph. D. degree in electrical engineering from Southwest Jiaotong University, Chengdu, China, in 2021. From 2019 to 2020, he was a Visiting Researcher with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, USA. From 2021 to 2022, he was a Postdoc Research Associate with the Department of Electrical Engineering, The Hong Kong Polytechnic University, Hong Kong, China. He is currently a Postdoc Research Fellow with the Department of Electrical Engineering, City University of Hong Kong, Hong Kong, China. His research interests include predictive model control of the converters in microgrids, electrical machines and drives control, electric traction supply system, and modulation and control technologies of multilevel converters in the solid-state transformer.

Haotian Zhu received the B.S. degree in electrical engineering and automation from the Southwest Jiaotong University, Chengdu, China, in 2021. He is currently working toward the M. S. degree in electrical engineering with Southwest Jiaotong University. His research interests include control and modulation techniques of the modular multilevel matrix converter, and control techniques of the power electronic traction transformer.

Zeliang Shu received the B. S. and Ph. D. degrees in electrical engineering from Southwest Jiaotong University, Chengdu, China, in 2002 and 2007, respectively. From 2008 to 2009, he was a Lecturer with Southwest Jiaotong University, where he is currently a Professor and Ph. D. Supervisor with the School of Electrical Engineering. His research interests include active power filter, reactive power compensator, pulse width modulation (PWM) rectifier, and digital signal processing with applications to power electronic converters.

Lan Ma received the B. S. degree in automation and the Ph. D. degree in control science and engineering from the University of Electronic Science and Technology of China, Chengdu, China, in 2011 and 2018, respectively. From 2015 to 2017, she was a Visiting Scholar with Future Renewable Electric Energy Delivery and Management Systems Center, Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, USA. She is currently a Research Fellow with the School of Electrical Engineering, Southwest Jiaotong University, Chengdu, China. Her research interests include energy storage and solar system control, power electronics converters, and virtual synchronous machine.

Changsong Cai received the Ph. D. degree in electrical engineering from Wuhan University, Wuhan, China, in 2020. From 2019 to 2020, he was a Visiting Researcher with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, USA. He is currently a Postdoctoral Researcher with the School of Electrical Engineering and Automation at Wuhan University, Wuhan, China. He is the recipient of the First Place Prize Paper Award from the IEEE Transactions on Power Electronics in 2022. His current research interests include engineering electromagnetism, power electronics, and wireless power transfer and its industrial applications.

Pengcheng Zhang received the B. S. degree in electrical engineering and the M.S. degree in control science and engineering from Tiangong University, Tianjin, China, in 2013 and 2016, respectively. He received the Ph.D. degree in electrical engineering from the Hebei University of Technology, Tianjin, China, in 2021. From November 2017 to December 2019, he was a Visiting Researcher with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, USA. He is currently a Postdoctoral Researcher with the Department of Electrical Engineering at Tsinghua University, Beijing, China. He received the First Place Prize Paper Award from the IEEE Transactions on Power Electronics in 2022. His research interests include wireless power transfer and electromagnetic shielding.

Li He received the B. S. degree in electrical engineering and automation from Northeast Agricultural University, Harbin, China, in 2018, and the M.S. degree in electrical engineering from Southwest Jiaotong University, Chengdu, China, in 2021. He is currently an Engineer with Huawei Technologies Company Ltd., Dongguan, China. His research interests include the control technology of modular multilevel converter.

Ruoyu Li received the B.S. and M.S. degrees in electrical engineering from Southwest Jiaotong University, Chengdu, China, in 2018 and 2021, respectively. He is currently a Digital Designer with Mediatek Inc., Hefei, China. His research interests include bi-directional DC-DC converters and digital modulation and control algorithms.

Shasha Song received the M.S. degree in electrical engineering from Southwest Jiaotong University, Chengdu, China, in 2016. She is currently an Engineer with State Grid Nanchong Electric Power Supply Company, Nanchong, China. Her research interests include modular multilevel converters and control strategy of three-phase to single-phase converters.

Josep M. Guerrero received the B. Sc. degree in telecom engineering, the M. Sc. degree in electronics engineering, and the Ph. D. degree from the Technical University of Catalonia, Barcelona. Since 2011, he has been a Full Professor with AAU Energy, Aalborg University, Aalborg, Denmark, where he is responsible for the Microgrid Research Program. From 2019, he became a Villum Investigator by the Villum Fonden, which supports the Center for Research on Microgrids (CROM) at Aalborg University, being Prof. Guerrero the founder and Director of the same center (www. crom. et. aau. dk). In 2020, he initiated neuroscience studies and research. As a result, in 2022, he received the M.Sc. degree in Psychobiology and Cognitive Neuroscience from the Autonomous University of Barcelona, Barcelona. He is currently pursuing an M. Sc. degree in Sleep: Physiology and Medicine at the University of Murcia, Spain. He is an Associate Editor for several IEEE journals. During nine consecutive years, from 2014 to 2022, he was awarded by Clarivate Analytics as Highly Cited Researcher. In 2021, he received the IEEE Bimal Bose Award for Industrial Electronics Applications in Energy Systems, for his pioneering contributions to renewable energy based microgrids. In 2022, he received the IEEE PES Douglas M. Staszesky Distribution Automation Award, for contributions to making the hierarchical control of microgrid systems a practical reality. His research interests are oriented to different microgrid frameworks in applications like neuroscience-based artificial intelligence, digital twins, cybersecurity, block chain and transactive energy in maritime, aerospace and space electrification, micro-bioecological systems, and smart medical systems and cognitive neuroscience, including electroencephalography analysis for sleep research and large-scale brain networks.