

Superconducting Magnetic Energy Storage Integrated Current-source DC/DC Converter for Voltage Stabilization and Power Regulation in DFIG-based DC Power Systems

Ruohuan Yang, Jianxun Jin, Qian Zhou, Mingshun Zhang, Shan Jiang, and Xiaoyuan Chen

Abstract—Unpredictable power fluctuation and fault ride-through capability attract increased attention as two uncertain major factors in doubly-fed induction generators (DFIGs) integrated DC power system. Present solutions usually require complicated cooperation comprising multiple modules of energy storage, current control, and voltage stabilizer. To overcome the drawbacks of existing solutions, this paper proposes a superconducting magnetic energy storage (SMES) integrated current-source DC/DC converter (CSDC). It is mainly composed of a current-source back-to-back converter, and the SMES is tactfully embedded in series with the intermediate DC link. The proposed SMES-CSDC is installed in front of the DC-DFIG to carry out its dual abilities of load voltage stabilization under multifarious transient disturbances and power regulation under wind speed variations. Compared with the existing DC protection devices, the SMES-CSDC is designed on the basis of unique current-type energy storage. It has the advantages of fast response, extensive compensation range, concise hardware structure, and straightforward control strategy. The feasibility of the SMES-CSDC is implemented via a scaled-down experiment, and its effectiveness for DC-DFIG protection is verified by a large-scale DC power system simulation.

Index Terms—Superconducting magnetic energy storage (SMES), DC doubly-fed induction generator (DC-DFIG), current-source converter, voltage stabilization, power regulation.

I. INTRODUCTION

DUE to the growing development of the DC distributed generators and DC loads such as photovoltaic (PV), DC wind generators, data center, and electric vehicles, DC power system has attracted more and more attention in the past few years [1], [2]. The DC power system eliminates the

grid-connected inverter stages and associated disadvantages of frequency stability issues, reactive power issues, and harmonic issues, which is promised to prevail in the near future [3], [4].

Figure 1(a) shows the conceptual structure of the DC power system integrated with various kinds of distributed generators, DC loads, and energy storage devices (ESDs). Among distributed generators in applications of DC power systems, emerged DC doubly-fed induction generator (DC-DFIG) has come into researchers' investigation in recent years. DC-DFIG reserves the advantages of AC-DFIG, e.g., low volume, flexible control, low converter capacity, and enabling the maximization of energy extraction [5], [6]. Ulteriorly, the topology modification of DFIG with the integration into DC power system is configured with an uncontrollable rectifier and a reduced-capacity rotor-side converter (RSC), decreasing the capital cost [7]–[10]. The prominent prospect of the DC-DFIG is abundantly studied in the literature, and is expected for applications in DC microgrids [11], [12], ship power generations [13], and mine sites [14].

However, with the increased penetration of DC power systems into the AC utility grid, the concerns of the energy conversion and fault operation are gradually exposed in DC-DFIG. On one hand, wind energy has strong characteristics of randomness and intermittence handicapping the large-scale integration of wind power, which brings a potential risk of imbalance between power demand and supply [15], [16]. On the other hand, if the capacity of DC power systems occupies a large proportion of the entire power system, the DC power system must be equipped with fault ride-through (FRT) capacity since the considerable loss cannot be accepted anymore [17], [18]. Unfortunately, the DC-DFIG is still vulnerable to voltage disturbances.

For output power undulation, ESDs are the most straightforward one. Facing with the DC-DFIG, various kinds of DC-interfaced ESDs can be introduced to smooth the output power undulation such as lead-acid battery [19], vanadium redox flow battery (VRB) [20], super-capacitor [15], [21], and superconducting magnetic energy storage (SMES) [22]–[25]. However, the inner rotor over-voltage and electromagnetic (EM) torque oscillations of the DC-DFIG cannot be ef-

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ficiently suppressed by parallel-structured ESDs [26]. Moreover, the FRT issue of DC-DFIG in DC power systems differs from that in AC power systems. In AC power systems, the inner parameters of DFIGs such as rotor voltage and EM torque are preferential to be considered [27]–[29]. Therefore, the software-based control improvements are feasible, especially the methods in [30], [31], which reveals the physical mechanism of transient control from the perspective of circuit equivalence, and proposes excellent current controls to achieve precise realization of multiple transient targets.

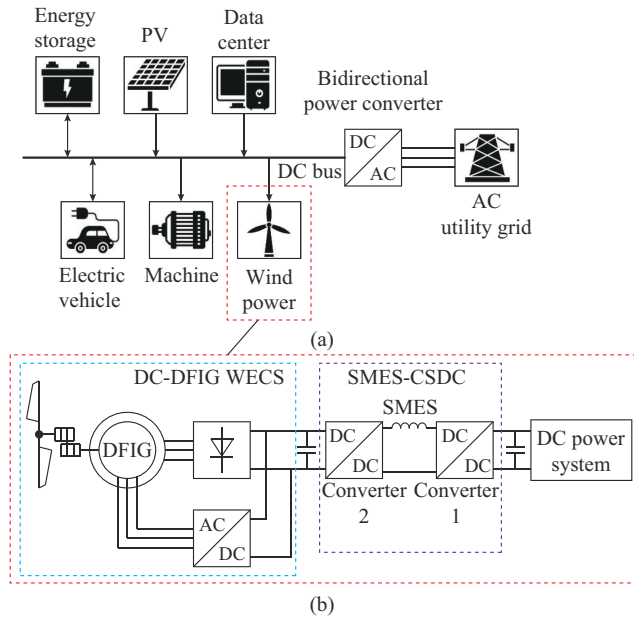


Fig. 1. Structures of DC power system and SMES-CSDC integrated DC-DFIG WECS. (a) Conceptual structure of DC power system. (b) SMES-CSDC integrated DC-DFIG WECS.

However, in DC power systems, the DC grid-side current under grid faults will rapidly increase with a considerable amplitude according to the DC fault characteristics [32], [33]. It will destroy the fragile converters and rectifiers of the DC-DFIG at the DC side. From this perspective, the DC custom power devices are proposed in the literature as series voltage compensation link to maintain the terminal voltage of the DC-DFIG during the whole transient process. DC applicative superconducting fault current limiter (SFCL) proposed in [34], [35] is an effective solution to limit the fault current. However, the terminal voltage at DC-DFIG side cannot be precisely controlled under voltage sag. Two power electronic transformer (PET) based DC dynamic voltage restorers (DC-DVRs) are proposed in [36] and [37]. However, the device presented in [36] fails to govern the voltage swell. Moreover, the compensation range of the two devices is limited due to their passive designs. In [38] and [39], an intelligent uninterruptable power supply (IUPS) and a battery-based DC-DVR is presented. However, the employments of multiple dual active bridges (DABs) and converters increase the system complexity.

Thanks to the technical advantages of extremely high current rating and nearly zero lossy resistance in superconducting materials, a number of superconductor-based electrical fa-

cilities have been widely used in power transmission and distribution networks [40], [41]. As for ESDs, SMES features high power density, high efficiency, and long cycle life. As a magnetic energy storage unit, SMES can be implemented for immediate charging and discharging operation in high-power required scenarios [42]–[44], and many SMES-based custom power devices have been developed to improve the power quality. In [45], a DAB-based DC unified power quality conditioner (UPQC) is proposed. Compared with the IUPS, the DC-UPQC has an extra path to manage the power flow. However, the same problem of the IUPS is also exposed to the DAB-based DC-UPQC, i.e., the system and control complexity. To avoid the immature PET technology, an SMES-based transformer-less series voltage regulator (TLSVR) is intelligently designed in [46]. The SMES coil inside the device is confluent with dual functions of energy storage and inductive-type fault current limiting. Unfortunately, the SMES-TLSVR fails to regulate the output power of the DC-DFIG, and it is also the common disadvantage in [34]–[39].

However, the SMES design in [46] with the combinations of energy storage and fault current limiting is still a state-of-the-art thought. Along with the concept, an SMES-based current-source DC/DC converter (CSDC) is presented in this paper. The proposed SMES-CSDC has dual capabilities of output power smoothing and FRT enhancement. With this structure, the utilization rate of the SMES is obviously increased, making the SMES-CSDC cost-effective for the application in the DC-DFIG wind energy conversion system (WECS). The proposed SMES-CSDC is an external power electronic device. Like DVRs, it can maintain the terminal voltage of the DC-DFIG at the rated profile, regardless of the control selection (vector control or direct control) of the DC-DFIG. Table I shows the comprehensive comparisons among the proposed SMES-CSDC and other existing DC custom power devices. The proposed SMES-CSDC avoids the shortcomings of the existing devices. It has less controlled switches, extensive compensation range, accompanied by multi-functions of voltage sag, voltage swell, and voltage ripple isolation as well as current and power regulation.

The remainder of this paper is organized as follows. Section II presents the overview of SMES-CSDC integrated DC-DFIG. Section III describes the issues of output power undulation and weakness of FRT capability via theoretical model establishments. Section IV indicates the circuit principle, voltage and current stresses, and control strategy of the proposed SMES-CSDC. Section V shows the scaled-down experimental results and related analysis. Section VI discusses the large-power simulation results. Section VII concludes the contribution.

II. OVERVIEW OF SMES-CSDC INTEGRATED DC-DFIG

Figure 1(b) shows the installation position of the SMES-CSDC incorporated with the DC-DFIG WECS. As shown in Fig. 1(b), the stator windings of the DC-DFIG are directly connected to the DC power system via a diode rectifier, and the rotor windings are linked to the grid via an AC/DC insulated gate bipolar translator (IGBT) based inverter.

TABLE I
COMPREHENSIVE COMPARISONS AMONG PROPOSED SMES-CSDC AND OTHER DC CUSTOM POWER DEVICES

Device	Voltage sag	Voltage swell	Voltage ripple	Power management	Compensation range	Energy storage	Transformer	Controlled switches
SFCL [34]	✓	✓	×	×	Uncontrollable		×	
DC-DVR [36]	✓	×	×	×	Small		✓	1
SVR [37]	✓	✓	×	×	Small		✓	12
IUPS [38]	✓	✓	×	×	Large	Battery	✓	16
DC-DVR [39]	✓	✓	×	×	Large	Battery	✓	12
DAB-UPQC [45]	✓	✓	✓	✓	Large	SMES	✓	24
TLSVR [46]	✓	✓	×	×	Large	SMES	×	8
Proposed SMES-CSDC	✓	✓	✓	✓	Large	SMES	×	4

Note: the symbols “×” and “✓” represent that the device is without and with this function, respectively.

Due to this particular structure, there is strong relevance between the stator voltage and the DC grid voltage. Therefore, the DC-DFIG is vulnerable to voltage disturbances. Additionally, the intermittence and the undulation of wind energy make the output power of the DC-DFIG constantly fluctuate.

The SMES-CSDC is a dual-DC-port device incorporating two converters, i.e., converters 1 and 2. Converter 1 is connected to the DC power system for DC grid-side current and power regulation, while converter 2 is interfaced with the DC-DFIG for terminal voltage stabilization. Figure 2 shows the working principle of the proposed SMES-CSDC in DC-DFIG application scenario, where v_L and i_g are the load-side voltage and grid-side current, respectively; P_{SMES} is the compensated power by SMES; and P_L and P_g are the load-side power and grid-side power, respectively.

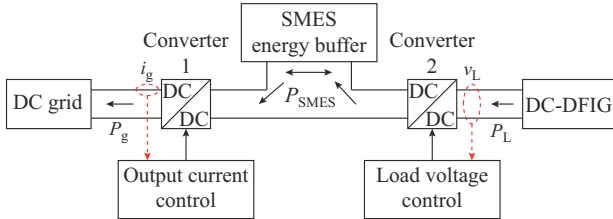


Fig. 2. Power flow among DC-DFIG, DC grid, and SMES-CSDC.

The role of the SMES is an energy buffer between the converters 1 and 2. The SMES-CSDC will re-regulate the output power of the DC-DFIG, and output a demanded power to the DC grid. If the output power of the DC-DFIG is fluctuated owing to the maximum power point tracking (MPPT) under wind gust [47]–[51], the power output to the grid will be maintained without oscillation due to the SMES energy buffer. Under the normal operation with wind speed fluctuation, converter 1 executes the output power smoothing. The surplus energy will be stored in the SMES when the output power of the DC-DFIG is higher than the power command defaulted in converter 1. On the contrary, the energy shortage will be supplemented to the DC power system via converter 1 when the output power of the DC-DFIG is insufficient due to the low wind velocity. Assuming that the required power of the grid is P_g^* , the power relationship

among DC-DFIG, DC grid, and SMES-CSDC can be expressed as:

$$P_g^* = (P_L^* + \Delta P_L) + P_{SMES} \quad (1)$$

where P_L^* is the rated power of the DC-DFIG; and ΔP_L is the fluctuated part of the power of DC-DFIG under wind variation.

Under the DC voltage disturbances, the SMES-CSDC isolates the grid fault, and converter 2 maintains the voltage of the DC-DFIG. Since there is a voltage difference between the DC grid and the DC-DFIG under voltage disturbances, the SMES can absorb the surplus power produced by DC-DFIG, which cannot be sent out under the voltage sag. Whereas, the SMES can also release a specific power to the grid under the voltage swell. The power relationship among DC-DFIG, DC grid, and SMES under voltage changes can be derived from (1) to:

$$(1-p)P_g^* = (P_L^* + \Delta P_L) + P_{SMES} \quad (2)$$

where p is the voltage changing ratio.

Compared with the traditional copper coil, the superiorities of the superconducting technology are reflected from the following two aspects.

1) The utilization of the superconductivity greatly improves the efficiency of the proposed CSDC. In copper coil, there is a tremendously high thermal loss. Furthermore, the thermal loss will be enlarged in a square relation with the increase of the current. With an SMES, there is only a little DC power loss due to the non-superconductive transmission line, and a little AC loss due to small SMES current ripple.

2) According to the structure of SMES-CSDC, the SMES is in series with the two converters. That means, only if the stored current in SMES is over the currents of the two terminals, the SMES has the power control ability. The available energy of the SMES E_a can be expressed as:

$$E_a = \frac{1}{2} L_{SC} i_{SCop}^2 - \frac{1}{2} L_{SC} (\max(i_L, i_g))^2 \quad (3)$$

where i_{SCop} is the operating current of SMES; L_{SC} is the inductance of SMES; and i_L is the DC load current. If the SMES is replaced by a copper coil, the operating current in the DC link will be strongly limited due to the high inner resistance. Therefore, the SMES is necessary in the proposed CSDC for obtaining higher operating current.

III. MODELING OF DC-DFIG

A. Wind Turbine

The mechanical power P_t captured by the wind turbine is relative to the power coefficient $C_p(\lambda, \beta)$, air density ρ , wind speed V_w , and the radius of rotor blades R_t . It can be expressed as:

$$P_t = \frac{1}{2} \rho \pi R_t^2 V_w^3 C_p(\lambda, \beta) \quad (4)$$

The power coefficient $C_p(\lambda, \beta)$ is a function of tip speed ratio λ and the pitch angle β . Its empirical equation can be represented as [52]:

$$\begin{cases} C_p(\lambda, \beta) = k_1 \left(\frac{k_2}{\lambda_i} - k_3 \beta - k_4 \beta^{k_5} - k_6 \right) e^{\frac{k_7}{\lambda_i}} \\ \lambda_i = \frac{1}{\lambda + k_8} \\ \lambda = \frac{R_t \Omega_t}{V_w} \end{cases} \quad (5)$$

where Ω_t is the rotor angular speed. For a specific wind turbine, the coefficients k_1 - k_8 are inherent. Equations (4) and (5) depict that the fluctuation of wind speed substantially handicaps the management and dispatching of wind power. To smooth wind power, the proposals regarding the utilizations of ESDs are demanded.

B. DC-DFIG

Assuming that the diode rectifier works in continuous conduction mode, the stator voltage is clamped to a four-level AC square wave [8]. The three-phase instantaneous stator voltages v_{sabc} can be expressed as:

$$v_{sa} = \frac{2V_L}{\pi} \left[\sin(\omega_s t) + \sum_{n=1}^{\infty} \frac{1}{6n \pm 1} \sin((6n \pm 1)\omega_s t) \right] \quad (6)$$

$$v_{sb} = \frac{2V_L}{\pi} \left[\sin\left(\omega_s t - \frac{2\pi}{3}\right) + \sum_{n=1}^{\infty} \frac{1}{6n \pm 1} \sin\left((6n \pm 1)\left(\omega_s t - \frac{2\pi}{3}\right)\right) \right] \quad (7)$$

$$v_{sc} = \frac{2V_L}{\pi} \left[\sin\left(\omega_s t + \frac{2\pi}{3}\right) + \sum_{n=1}^{\infty} \frac{1}{6n \pm 1} \sin\left((6n \pm 1)\left(\omega_s t + \frac{2\pi}{3}\right)\right) \right] \quad (8)$$

where ω_s is the stator frequency of the fundamental wave; and V_L is the DC load voltage, which can be regarded as a constant V_L under the steady state. The stator and rotor voltages and flux linkages can be expressed in the form of space vectors as [20]:

$$\begin{cases} \mathbf{v}_s^s = R_s \mathbf{i}_s^s + \frac{d\boldsymbol{\psi}_s^s}{dt} \\ \mathbf{v}_r^r = R_r \mathbf{i}_r^r + \frac{d\boldsymbol{\psi}_r^r}{dt} \end{cases} \quad (9)$$

$$\begin{cases} \boldsymbol{\psi}_s^s = L_s \mathbf{i}_s^s + L_m \mathbf{i}_r^s \\ \boldsymbol{\psi}_r^r = L_m \mathbf{i}_s^r + L_r \mathbf{i}_r^r \end{cases} \quad (10)$$

where R and L are the resistance and inductance, respectively; $\mathbf{v}$, $\mathbf{i}$, and $\boldsymbol{\psi}$ are the voltage, current, and stator flux, respectively,

of which the space vector forms are in bold; the superscripts s and r represent the stator and rotor coordinates, respectively; the subscripts s and r represent the stator and rotor, respectively; and L_m is the mutual inductance.

According to (10), the relationship between the stator and rotor flux linkage can be derived as:

$$\boldsymbol{\psi}_r^r = \frac{L_m}{L_s} \boldsymbol{\psi}_s^s + \sigma L_r \mathbf{i}_r^r \quad (11)$$

where σ is the leakage coefficient, which is expressed as:

$$\sigma = 1 - \frac{L_m^2}{L_r L_s} \quad (12)$$

The dynamic equation of rotor voltage can be derived from (6) and (8) as:

$$\mathbf{v}_r^r = \underbrace{\frac{L_m}{L_s} \frac{d\boldsymbol{\psi}_s^s}{dt}}_{\mathbf{e}_r^r} + \left(R_r + \sigma L_r \frac{d}{dt} \right) \mathbf{i}_r^r \quad (13)$$

where $\mathbf{e}_r^r$ is the rotor electromotive force (EMF) induced by the stator flux. Under the rotor open-circuited condition, there is only $\mathbf{e}_r^r$ in the expression of the rotor voltage in (13). The second term of (13) only appears when a current flows in the rotor windings. The mean of the second term is the voltage drop generated from the rotor resistance R_r and the transient inductance σL_r .

Assuming that a voltage sag of depth p occurs at $t=0$, i.e.,

$$\mathbf{v}_s^s = \frac{2(1-p)V_L}{\pi} \left[\mathbf{e}^{j\omega_s t} + \sum_{n=1}^{\infty} \frac{\mathbf{e}^{\pm(6n \pm 1)\omega_s t}}{6n \pm 1} \right] \quad t \geq 0 \quad (14)$$

Since the stator flux is a state variable, it does not change instantaneously. Therefore, the dynamic response of the stator flux $\boldsymbol{\psi}_s^s$ at the fault occurrence contains a steady component $\boldsymbol{\psi}_{sp}^s$ and a transient component $\boldsymbol{\psi}_{sdc}^s$, and they can be expressed as:

$$\boldsymbol{\psi}_s^s = \boldsymbol{\psi}_{sp}^s + \boldsymbol{\psi}_{sdc}^s \quad (15)$$

$$\boldsymbol{\psi}_{sp}^s = \frac{2(1-p)V_L}{\pi} \left[\frac{\mathbf{e}^{j\omega_s t}}{j\omega_s} + \sum_{n=1}^{\infty} \frac{\pm \mathbf{e}^{\pm(6n \pm 1)\omega_s t}}{j\omega_s (6n \pm 1)^2} \right] \quad (16)$$

$$\boldsymbol{\psi}_{sdc}^s = \frac{2pV_L}{\pi} \left[\frac{1}{j\omega_s} + \sum_{n=1}^{\infty} \frac{\pm 1}{j\omega_s (6n \pm 1)^2} \right] \mathbf{e}^{-\frac{t}{\tau_s}} \quad (17)$$

Substituting (15)-(17) into (13), the EMF $\mathbf{e}_r^r$ under the voltage sag can be expressed as:

$$\begin{aligned} \mathbf{e}_r^r &= \frac{L_m}{L_s} \frac{d\boldsymbol{\psi}_s^s}{dt} = \\ &= \underbrace{\frac{2(1-p)V_L}{\pi} \frac{L_m}{L_s} \left(s \mathbf{e}^{j\omega_s t} + \sum_{n=1}^{\infty} \frac{1 \pm s}{6n \pm 1} \mathbf{e}^{\pm j(6n \pm 1)\omega_s t} \right)}_{\mathbf{e}_{rp}^r} + \\ &= \underbrace{\frac{2pV_L}{\pi} \frac{L_m}{L_s} \left[(1-s) + \sum_{n=1}^{\infty} \frac{\pm(s-1)}{(6n \pm 1)^2} \right] \mathbf{e}^{-j\omega_s t}}_{\mathbf{e}_{rdc}^r} \mathbf{e}^{-\frac{t}{\tau_s}} \end{aligned} \quad (18)$$

where ω_{sl} is the slip frequency, i.e., $\omega_{sl} = \omega_s - \omega_r$; and s is the slip, i.e., $s = (\omega_s - \omega_r)/\omega_s$. When an asymmetrical fault occurs in the AC utility grid, without a protection device, the

DC load voltage v_L will contain a residual DC component V_{L1} and a second-order oscillation with the amplitude of V_{L2} , and the stator voltage v_s^s will experience a voltage unbalance and can be transferred to:

$$v_s^s = \frac{2V_{L1}}{\pi} \left(e^{j\omega_s t} + \sum_{n=1}^{\infty} \frac{1}{6n \pm 1} e^{\pm j(6n \pm 1)\omega_s t} \right) + \frac{2V_{L2}}{\pi} \left(e^{-j\omega_s t} + \sum_{n=1}^{\infty} \frac{1}{6n \pm 1} e^{\mp j(6n \pm 1)\omega_s t} \right) \quad t \geq 0 \quad (19)$$

Under the AC-side asymmetrical fault, the dynamic response of the stator flux will additionally contain a negative component ψ_{sn}^s that can be expressed as:

$$\psi_{sn}^s = \frac{2V_{L2}}{\pi} \left[\frac{e^{-j\omega_s t}}{-j\omega_s} + \sum_{n=1}^{\infty} \frac{\mp e^{\mp j(6n \pm 1)\omega_s t}}{j\omega_s (6n \pm 1)^2} \right] \quad (20)$$

Correspondingly, the EMF e_r^r under AC-side asymmetrical voltage sag will mainly contain an additional component e_{rn}^r :

$$e_{rn}^r = \frac{2V_{L2}L_m}{\pi L_s} \left[(2-s)e^{-j(2-s)\omega_s t} + \sum_{n=1}^{\infty} \frac{1 \mp}{6n \pm 1} e^{\mp j(6n \pm 1)\omega_s t} \right] \quad (21)$$

Combining (18) and (21), under the normal operation, there is only e_{rp}^r in the induced EMF. The amplitude of the e_{rp}^r is relative to the slip s . In practical, the synchronous speed is always designed according to the rated wind speed so that the slip can be limit within ± 0.3 , and the maximum slip power is only 30% of the rated power [15], [52], [53]. Therefore, the induced EMF under the normal operation is always small. When an AC-side symmetrical fault occurs, the DC load voltage v_L experiences an amplitude dip, and the component e_{rdc}^r will be induced, resulting in an over-voltage to the converter. Under the AC-side unbalanced voltage fault, a huge EMF oscillation e_{rn}^r will be introduced, with its fundamental amplitude and frequency of $2-s$ and $-(2-s)\omega_s$, respectively. Such an oscillation will lead to a vast pulsation of EM torque and a heating problem of stator and rotor windings, damaging the expensive gearbox and the generator.

IV. PROPOSED SMES-CSDC

Based on the wind power fluctuations and transient dynamics of DC-DFIG analyzed in Section III-A and III-B, the critical issues of the DC-DFIG that urgently need to be addressed can be summarized as: ① an ESD is required to enable the output power of DC-DFIG controllable during wind speed variation; and ② a voltage maintenance method is demanded for FRT improvement of DC-DFIG under voltage sag/swell and voltage oscillation. In this section, the proposed SMES-CSDC applied in DC-DFIG is introduced from configuration, circuit modeling, control strategy, and voltage and current stress.

A. Configuration

The structure of the proposed SMES-CSDC is shown in Fig. 3. It comprises two symmetrical converters, i.e., converters 1 and 2, and an SMES coil. Converters 1 and 2 are made up of S_1 - S_4 and Q_1 - Q_4 , respectively, where S_1 , S_4 , Q_1 ,

and Q_4 are the controlled switches, and S_2 , S_3 , Q_2 , and Q_3 are the diodes. The switches S_1 and Q_1 have the same on-off state with S_4 and Q_4 , respectively. The SMES coil is connected between the joints A₁ and B₂, as shown in Fig. 3. Joints A₂ and B₁ are directly linked for the current continuation of the SMES. Joints (M₁, M₂) and (N₁, N₂) connect separately with the positive and negative ports of the DC grid side and DC load side. Converter 1 that controls the output current is for power management. In contrast, converter 2 maintains the load voltage to prevent DC voltage disturbances.

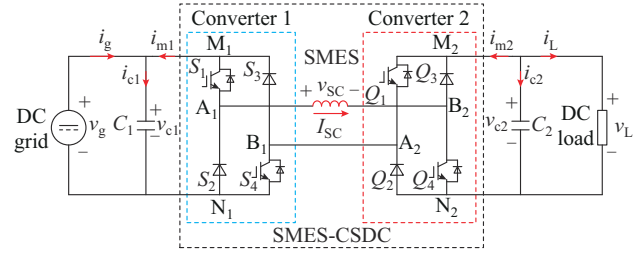


Fig. 3. Structure of proposed SMES-CSDC.

B. Circuit Modeling of SMES-CSDC

Figure 4 shows the operating statuses of the SMES-CSDC.

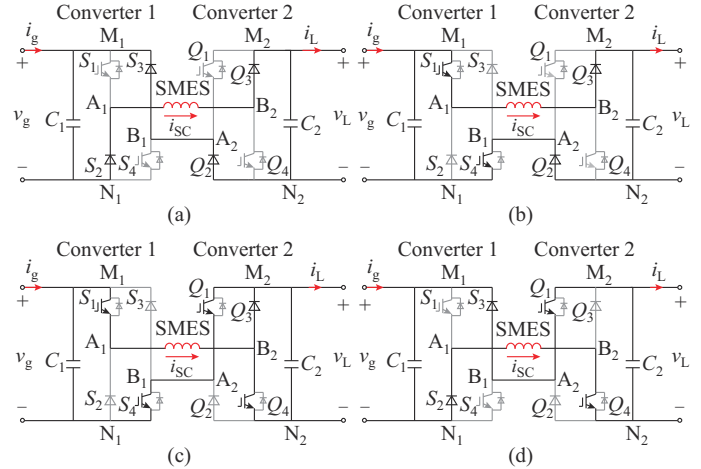


Fig. 4. Operating statuses of SMES-CSDC. (a) Status 1. (b) Status 2. (c) Status 3. (d) Status 4.

Several factors are assumed to simplify the processing of the theoretical analysis as follows.

- 1) Assumption 1: the DC load is resistive-type, and the current flows from the DC source to the DC load.
- 2) Assumption 2: the two capacitors have the same capacity: $C_1 = C_2 = C$.
- 3) Assumption 3: the whole circuit is operating under steady state.
- 4) Assumption 4: under steady state, the SMES current can be approximately regarded as a constant I_{sc} .

There are four statuses depending on the on-off states of S_1 - S_4 and Q_1 - Q_4 : ① status 1: $S_1 = S_4 = 0$, $Q_1 = Q_4 = 0$; ② status 2: $S_1 = S_4 = 1$, $Q_1 = Q_4 = 0$; ③ status 3: $S_1 = S_4 = 1$, $Q_1 = Q_4 = 1$; and ④ status 4: $S_1 = S_4 = 0$, $Q_1 = Q_4 = 1$.

Taking status 1 as the analyzed object, the equation group can be established as:

$$\begin{cases} L_{SC} \frac{di_{m1}}{dt} + R_{SC} i_{m1} + v_{c1} - v_{c2} = 0 \\ i_{m1} + i_g = i_{c1} = C \frac{dv_{c1}}{dt} \\ i_{m2} - i_L = i_{c2} = C \frac{dv_{c2}}{dt} \end{cases} \quad (22)$$

where R_{SC} is the leakage resistance of SMES; i_{c1} , i_{c2} and v_{c1} , v_{c2} are the currents and voltages of capacitors C_1 and C_2 , respectively; and i_{m1} and i_{m2} are the output currents of converters 1 and 2, respectively. According to the circuit principle shown in Fig. 3, $i_{m1} = i_{m2} = i_m$. Equation (22) can be further derived as:

$$L_{SC} C \frac{d^2 i_m}{dt^2} + R_{SC} C \frac{di_m}{dt} + i_g + i_L = 0 \quad (23)$$

The characteristic equation of the homogeneous equation (23) can be expressed as:

$$L_{SC} C s^2 + R_{SC} C s = 0 \quad (24)$$

The characteristic roots $s_{1,2}$ are:

$$s_{1,2} = \frac{-R_{SC} C \pm \sqrt{(R_{SC} C)^2}}{2L_{SC} C} = -\frac{R_{SC} \pm R_{SC}}{2L_{SC}} \quad (25)$$

Since the criterion $\Delta = (R_{SC} C)^2 > 0$, the transient dynamics of the status 1 are over-damped. The force-free response of the current i_m can be then expressed as:

$$i_m = i_m'' = A_1 e^{s_1 t} + A_2 e^{s_2 t} \quad (26)$$

where i_m'' is the homogeneous solution part of i_m . The integration constants A_1 and A_2 depend on the initial conditions of status 1. According to (25), $s_1 = 0$. From the above-defined assumption 4, the initial SMES current is I_{SC} . A_1 and A_2 can be then derived as:

$$\begin{cases} A_1 + A_2 = i_m(0_+) = I_{SC} \\ s_2 A_2 = \frac{di_m(0_+)}{dt} = \frac{v_{c2} - v_{c1}}{L_{SC}} \end{cases} \quad (27)$$

where $i_m(0_+)$ represents the initial current at the beginning of status 1. The response of i_m under status 1, which is denoted as $i_{m,s1}$, can be then re-written as:

$$i_{m,s1} = I_{SC} - \frac{v_{c1} - v_{c2}}{R_{SC}} + \frac{v_{c1} - v_{c2}}{R_{SC}} e^{-\frac{R_{SC}}{L_{SC}} t} \quad (28)$$

As shown in Fig. 3, the direction of i_{m1} is the same as that of the SMES current I_{SC} . From (28), the response of the i_m under status 1 is monotone-decreasing. That is, the SMES is in discharging mode.

Status 3 has a similar circuit operation with status 1. The value of i_m under status 3, i.e., $i_{m,s3}$, can be calculated as:

$$i_{m,s3} = -I_{SC} + \frac{v_{c1} - v_{c2}}{R_{SC}} - \frac{v_{c1} - v_{c2}}{R_{SC}} e^{-\frac{R_{SC}}{L_{SC}} t} \quad (29)$$

Note that the direction of the $i_{m,s3}$ is opposite to that of the SMES current I_{SC} . Equation (29) shows that the $i_{m,s3}$ is a monotone-increasing function. Under this status, the SMES is in charging mode.

Under statuses 2 and 4, (22) can be renewed as:

$$\begin{cases} L_{SC} \frac{di_{m1}}{dt} + R_{SC} i_{m1} + v_{c1} - v_{c2} = 0 \\ i_{m1} + i_s = i_{c1} = C \frac{dv_{c1}}{dt} \\ -i_{m2} - i_L = i_{c2} = C \frac{dv_{c2}}{dt} \end{cases} \quad (30)$$

Equations (23) and (24) can be accordingly re-derived as:

$$L_{SC} C \frac{d^2 i_m}{dt^2} + R_{SC} C \frac{di_m}{dt} + 2i_m + i_s + i_L = 0 \quad (31)$$

$$L_{SC} C s^2 + R_{SC} C s + 2 = 0 \quad (32)$$

The characteristic roots $s_{1,2}$ are then transferred as:

$$s_{1,2} = -\frac{R_{SC}}{2L_{SC}} \pm \sqrt{\left(\frac{R_{SC}}{2L_{SC}}\right)^2 - \frac{2}{L_{SC} C}} = -\beta \pm \sqrt{\beta^2 - \omega_0^2} \quad (33)$$

Due to the superconductivity, the R_{SC} is extremely small, and the criterion $\Delta = (R_{SC} C)^2 > 0$. The transient dynamics of the statuses 2 and 4 are under-damped. The force-free response can be then re-written as:

$$i_m'' = e^{-\beta t} (A_1 \cos \omega' t + A_2 \sin \omega' t) \quad (34)$$

$$\omega' = \sqrt{\omega_0^2 - \beta^2} \quad (35)$$

The coefficients A_1 and A_2 can be solved from the following equation groups based on the characteristics of inductance current.

$$\begin{cases} A_1 = i_m(0_+) = -I_{SC} \\ -\beta A_1 + \omega' A_2 = \frac{v_{c2} - v_{c1}}{L_{SC}} \end{cases} \quad \text{status 2} \quad (36)$$

$$\begin{cases} A_1 = i_m(0_+) = I_{SC} \\ -\beta A_1 + \omega' A_2 = \frac{v_{c1} - v_{c2}}{L_{SC}} \end{cases} \quad \text{status 4} \quad (37)$$

Under statuses 2 and 4, the solutions of A_1 and A_2 are respectively expressed as:

$$\begin{cases} A_1 = -I_{SC} \\ A_2 = \frac{\beta I_{SC} + \frac{v_{c2} - v_{c1}}{L_{SC}}}{\omega'} \end{cases} \quad \text{status 2} \quad (38)$$

$$\begin{cases} A_1 = I_{SC} \\ A_2 = \frac{-\beta I_{SC} + \frac{v_{c1} - v_{c2}}{L_{SC}}}{\omega'} \end{cases} \quad \text{status 4} \quad (39)$$

According to (34), (38), and (39), the monotonicity of i_m under statuses 2 and 4 is challenging to determine, mainly depending on the difference between v_{c1} and v_{c2} . When the output sides of converters 1 and 2 have the same voltage level, v_{c1} and v_{c2} are almost equal, and the SMES current barely charges or discharges under statuses 2 and 4.

C. Control Strategy

The control system of the SMES-CSDC is shown in Fig. 5. The actual signals of the DC grid-side current i_g and the DC load voltage v_L are used as the input signals, the differ-

ences between which and the reference signals I_{gref} and V_{Lref} are input to the proportional-integral (PI) controllers 1 and 2, denoted as PI-1 and PI-2, respectively. The outputs of the PI-1 and PI-2 are limited within the range of $[-0.5, 0.5]$. By adding the outputs with an offset constant of 0.5, the duty cycles D_1 and D_2 can be both controlled between 0 and 1. The switching signals of S_1, S_4 and Q_1, Q_4 can be generated from the two triangular-carrier-based comparators, respectively, following the duty cycles D_1 and D_2 .

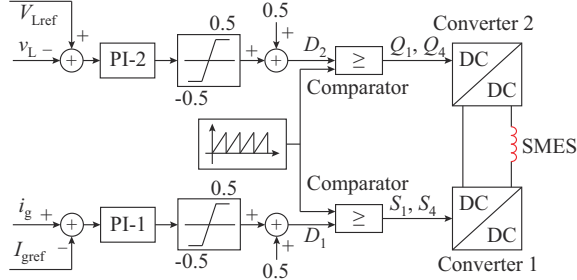


Fig. 5. Control system of SMES-CSDC.

D. Voltage and Current Stresses

Figure 6 shows the voltage and current waveforms of each crucial parameter. According to the configuration shown in Fig. 3, the capacitors C_1 and C_2 are used for voltage and current filters. Considering that L_{SC} is quite large as an SMES inductance and the control of converters 1 and 2 are in high-frequency, the variations of the charging and discharging current during one period are small, and i_{m1} and i_{m2} can be considered as high-frequency AC square signals. Combining with aforesaid theoretical analyses, the waveforms of i_{m1} , i_{m2} , i_{c1} and i_{c2} during one period can be estimated as:

$$i_{m1} = \begin{cases} I_{\text{SC}} & 0 < t \leq D_1 T_{\text{SW}} \\ -I_{\text{SC}} & D_1 T_{\text{SW}} < t \leq T_{\text{SW}} \end{cases} \quad (40)$$

$$i_{m2} = \begin{cases} -I_{\text{SC}} & 0 < t \leq D_2 T_{\text{SW}} \\ I_{\text{SC}} & D_2 T_{\text{SW}} < t \leq T_{\text{SW}} \end{cases} \quad (41)$$

$$i_{c1} = \begin{cases} I_{\text{SC}} + i_{\text{g}} & 0 < t \leq D_1 T_{\text{SW}} \\ -I_{\text{SC}} + i_{\text{g}} & D_1 T_{\text{SW}} < t \leq T_{\text{SW}} \end{cases} \quad (42)$$

$$i_{c2} = \begin{cases} I_{\text{SC}} - i_{\text{L}} & 0 < t \leq D_2 T_{\text{SW}} \\ -I_{\text{SC}} - i_{\text{L}} & D_2 T_{\text{SW}} < t \leq T_{\text{SW}} \end{cases} \quad (43)$$

where T_{SW} is the switching period, and the directions of the above-mentioned signals are in accordance with the labels in Fig. 3.

The voltage waveform of v_{SC} is shown in Fig. 6, corresponding to the switch sequence. During $(0, D_1 T_{\text{SW}})$ and $(D_2 T_{\text{SW}}, T_{\text{SW}})$, the SMES coil withstands the sum of the voltages, the two capacitors v_{c1} and v_{c2} . During $(D_1 T_{\text{SW}}, D_2 T_{\text{SW}})$, the voltage of the SMES coil is the difference between the v_{c1} and v_{c2} . v_{SC} is expressed as:

$$v_{\text{SC}} \approx \begin{cases} -(v_{c1} + v_{c2}) & 0 < t \leq D_1 T_{\text{SW}} \\ v_{c1} - v_{c2} & D_1 T_{\text{SW}} < t \leq D_2 T_{\text{SW}} \\ v_{c1} + v_{c2} & D_2 T_{\text{SW}} < t \leq T_{\text{SW}} \end{cases} \quad (44)$$

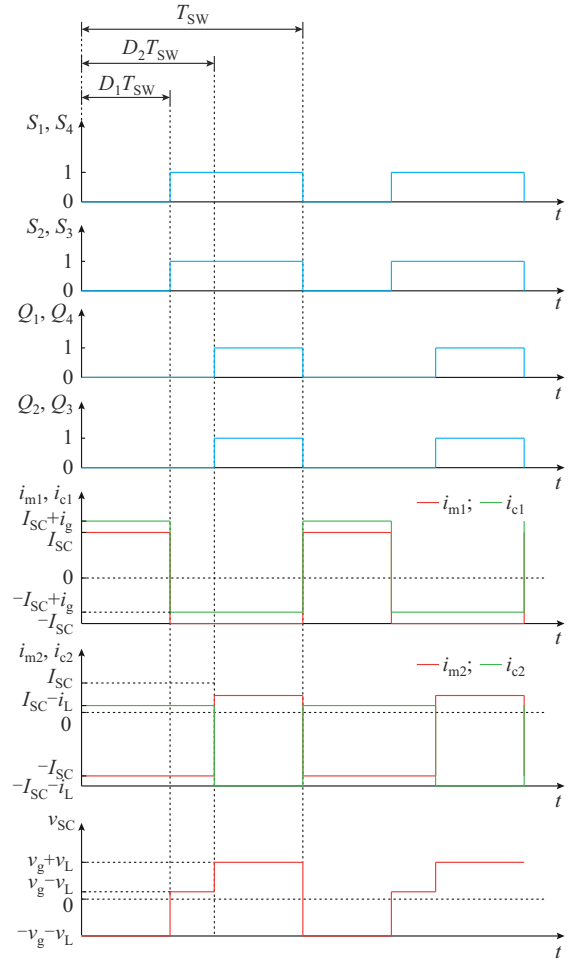


Fig. 6. Voltage and current waveforms of each crucial parameter.

According to the principle of the current source converter, it is apparent that the values of the duty cycles D_1 and D_2 are in connection with the relationship among the output current of converter 1 i_{g} , input current of converter 2 i_{L} , and SMES current I_{SC} . The duty cycles D_1 and D_2 can be expressed as:

$$\begin{cases} D_1 = \frac{1}{2} \left(1 - \frac{i_{\text{g}}}{I_{\text{SC}}} \right) \\ D_2 = \frac{1}{2} \left(1 + \frac{i_{\text{L}}}{I_{\text{SC}}} \right) \end{cases} \quad (45)$$

According to (45), in load protection scenario, the current directions of i_{g} and i_{L} are positive with the marks in Fig. 3. The ranges of the D_1 and D_2 are in $(0, 0.5)$ and $(0.5, 1)$, respectively. The status sequence of the circuit during one period is: statuses 1→2→3. In DC-DFIG application scenario, the current flows of i_{g} and i_{L} are opposite to the marks in Fig. 3. The duty cycles D_1 and D_2 are always in the range of $(0.5, 1)$ and $(0, 0.5)$, respectively. Also, D_1 is always larger than D_2 , and the status sequence of the circuit during one period is always as: statuses 1→4→3. When a voltage or current disturbance occurs, both of the two duty cycles are changed along with the variation of the stored energy I_{SC} .

V. EXPERIMENT OF SMES-CSDC

A scaled-down experiment platform of SMES-CSDC is established to verify the working principle and the function feasibility. The experimental prototype and schematic circuit diagram are shown in Fig. 7. A kW-class 10 mH/120 A SMES is adopted in this experiment. The experimental voltage and current specifications of the DC source and DC load are 36 V and 12 A, respectively. The adopted SMES has a varying-axial-gap structure, which comprises six series-connected double-pancake coil assemblies. The high temperature superconducting (HTS) material used to wind the SMES is ReBCO, and the commercial tape is processed by Shanghai Superconductor Technology Co., Ltd. Detailed design about this kind of SMES can be referred to [45]. The two converters are driven by DSP (TMS320F28335), and the selected power-electronic switches in this experiment are Infineon IPT007N06N.

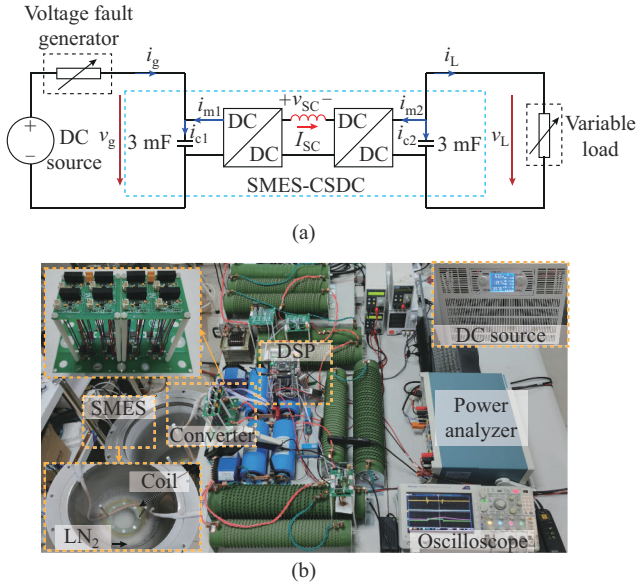


Fig. 7. Equivalent circuit of experiment and platform. (a) Equivalent circuit of experiment. (b) Experimental platform.

A. Voltage and Current Stresses

Figure 8(a) shows the responses of i_{m1} , i_{m2} , i_{c1} , i_{c2} , and v_{sc} under the normal operation. Under the normal operation, the SMES current is about 51 A. According to (40)-(43), the currents i_{m1} , i_{m2} , i_{c1} , and i_{c2} are all square waves with the duty cycles D_1 and D_2 . The amplitudes of i_{m1} and i_{m2} are both about 52 A. As can be observed from Fig. 8(a), a DC current bias with the value of $|i_g|$ exists in the i_{c1} . Accordingly, there is a DC current bias with the value of $|i_L|$ in the current i_{c2} .

Under normal operation, the values of v_{c1} and v_{c2} are equal to the DC grid and DC load voltages, respectively. The DC grid voltage is slightly higher than the DC load voltage, as the SMES requires an excitation from the DC grid to generate a high magnetic field for energy storage [54]. As depicted in (44), v_{sc} is a three-step square wave. From Fig. 8(a), the amplitudes of v_{sc} during $(0, D_1T_{sw})$, (D_1T_{sw}, D_2T_{sw}) , and (D_2T_{sw}, T_{sw}) are about -75 V, 3 V and 75 V, respectively, approximately equal to the values of $-v_g - v_L$, $v_g - v_L$, and $v_g + v_L$.

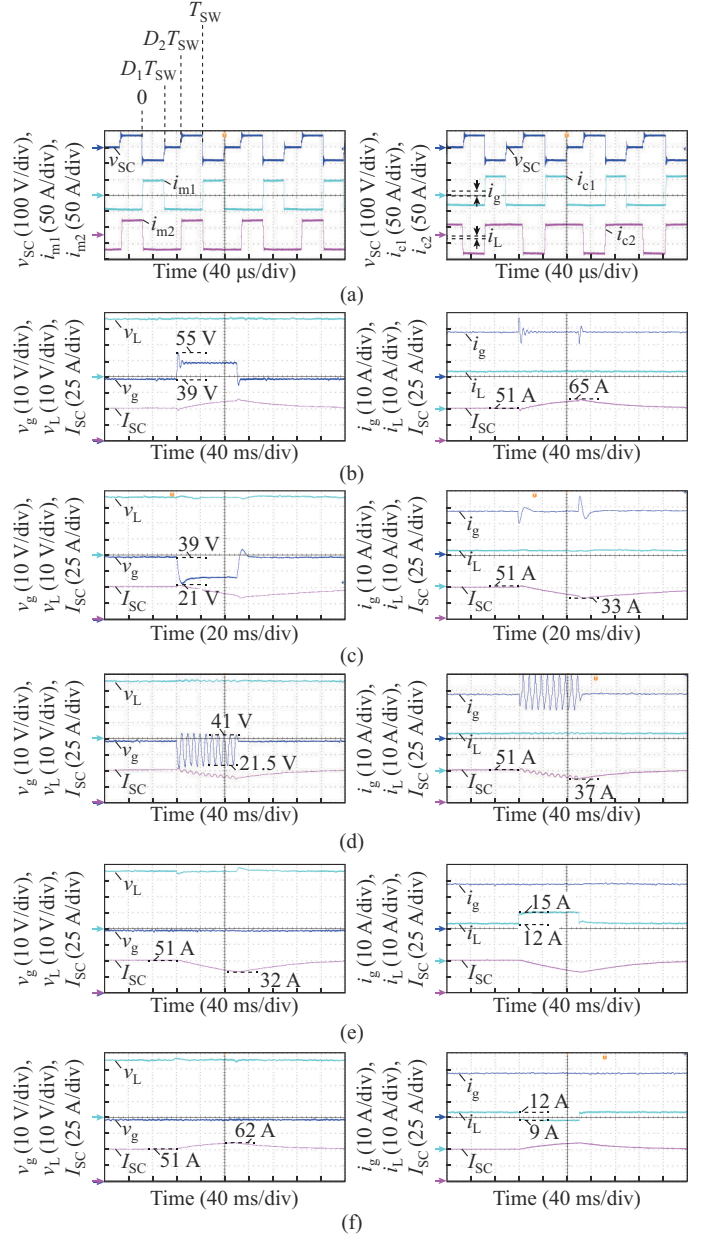


Fig. 8. Test results of SMES-CSDC. (a) Voltage and current stresses. (b) Voltage sag. (c) Voltage swell. (d) Second-order voltage oscillation. (e) Load current increment. (f) Load current reduction.

As illustrated above, all the critical waveforms shown in Fig. 8(a) are consistent with the aforesaid working principle shown in Fig. 6. Therefore, the experiment verifies the correctness of the theoretical analysis.

B. Voltage Sag and Swell

The responses of v_g , v_L , i_g , i_L , and I_{sc} under DC voltage sag and swell conditions are shown in Fig. 8(b) and (c), respectively. As can be observed from Fig. 8(b), although the DC grid voltage temporarily raises to 55 V, the DC load voltage is sustained at 36 V during the whole transient process, and the SMES current is charged from 51 A to 65 A. Under voltage sag, the DC source voltage drops from 39 V to 21 V. The stored energy discharges from SMES to DC load, and the SMES current varies from 51 A to 33 A.

It is noteworthy that there are two spikes of the DC grid current i_g at the fault occurrence and clearance. It is caused by the charging and discharging of capacitors. With the comparison between i_g and i_L , the SMES-CSDC can efficiently isolate the influence of the fault current spikes on the DC load.

C. Second-order Voltage Ripple

As reported in the literature, the AC voltage imbalance will cause the second-order voltage ripple in the DC power system [55]. An experiment is implemented to describe the behaviors of the SMES-CSDC under the second-order DC voltage oscillation, and the results are shown in Fig. 8(d). As can be observed from Fig. 8(d), a second-order DC voltage ripple is set in the DC source. Although the oscillation of the DC grid current i_g cannot be well-suppressed, both the voltage and current of the DC load can be well-compensated with almost no second-order oscillations.

D. Load Current Variation

An experiment of load current variation is carried out to verify the current control of converter 1, and the results are shown in Fig. 8(e) and (f). In the scenario shown in Fig. 8(e), a 36 V/12 Ω load is abruptly switched into the DC load side, and the DC load current fast increased from 12 A to 15 A. Since there is no voltage disturbance in the whole system, both voltages v_g and v_L are almost not changed. To maintain the DC grid current constant, the SMES stored current is released to the DC load, and I_{sc} discharges from 51 A to 32 A. Conversely, when part of the DC load excises, as shown in Fig. 8(f), the DC load current drops from 12 A to

9 A, and the SMES current charges from 51 A to 62 A.

Conclusively, the above experimental results confirm the consistency of the theory and prove that the proposed SMES-CSDC can comprehensively protect the DC load from the perspectives of voltage maintenance, oscillation isolation, and the current and power management.

VI. CASE STUDY

In Section V, the voltage protection as well as the current and power management capabilities of the SMES-CSDC have been proven via a scaled-down experiment. To further verify the superiorities of the proposed device in the application of DC power systems, a DC-DFIG is established in simulation via MATLAB/Simulink to observe the protection performance of the SMES-CSDC. The scheme and the control strategy of the SMES-CSDC integrated DC-DFIG is shown in Fig. 9. The scale of the DC-DFIG in simulation is 3 kV/1 MW. Its cut-in and cut-off wind speeds are 3 m/s and 25 m/s, respectively, and the nominal wind speed is 11 m/s. The inductance and critical current of the SMES is 5.14 H and 900 A, respectively. The design of the SMES is with the varying-axial-gap structure [54]. It is made up of Q single pancakes, among which m single pancakes have a fundamental gap of g , and a gap increment of Δx while other $Q/2 - m$ single pancakes have a constant axial gap d . The fundamental element of the designed SMES is 2.57 H/900 A. In the simulation, two SMES elements are connected in parallel for utilization, and the inductance can be enlarged to 5.14 H. The initial current of the SMES is set to be 570 A. Two typical conditions are analyzed in the simulation, i.e., ① variable wind speed; and ② DC voltage disturbances.

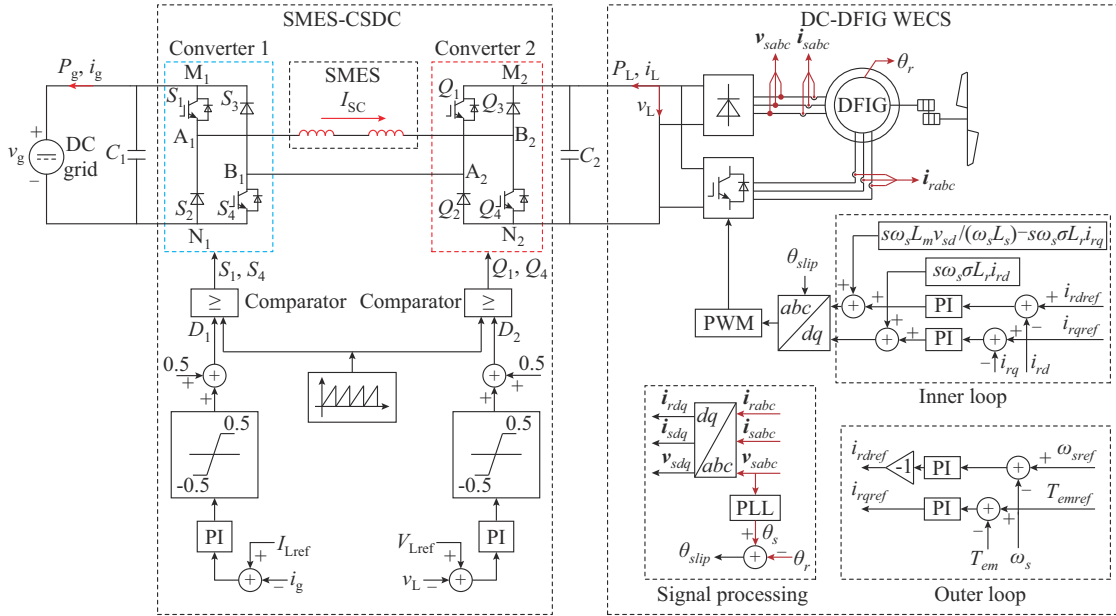


Fig. 9. Scheme and control strategy of SMES-CSDC integrated DC-DFIG.

A. Variable Wind speed

Under the random wind speed shown in Fig. 10(a), the control target of converter 1 is to manage the DC output cur-

rent. Since the DC voltage is constant under the normal operation, the regulation of DC output current brings the regulation of the DC output power. In this simulation, a filter-

based output power management strategy is used to save the requirement of the SMES capacity [20]. The current command can be dynamically adjusted from the filtered output current of the DC-DFIG:

$$I_{Lref} = \frac{1}{1 + T_{filter}s} i_L \quad (46)$$

where T_{filter} is the filter time constant. By this means, the required energy storage capacity can be significantly reduced. As seen from Fig. 10(a) and (b), the wind speed varies from 9 m/s to 14 m/s, and the output power flows from 0.8 p.u. to 1.3 p.u.. With the SMES-CSDC, when the wind power output by the DC-DFIG P_g is larger than the power command P_L , the SMES will be charged to absorb the surplus energy and vice versa. The DC output power via the regulation of the SMES-CSDC can be obviously optimized. The SMES current is shown in Fig. 10(c), reflecting the energy conversion during time-varying wind speed condition.

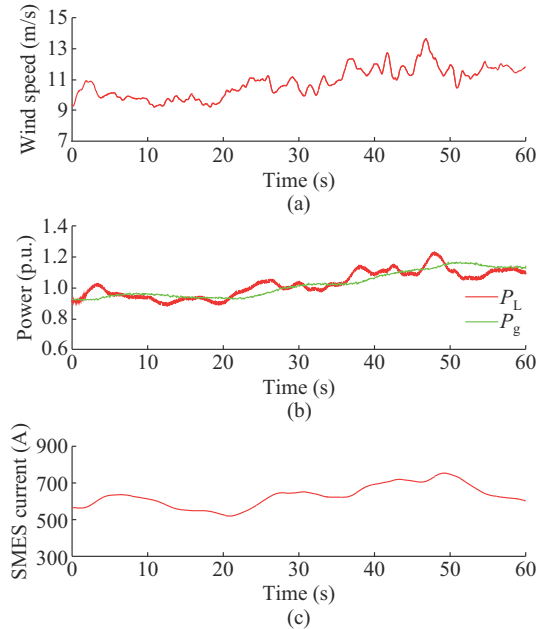


Fig. 10. Effect of SMES-CSDC in wind power smoothing. (a) Wind speed. (b) Output power of DC-DFIG and DC grid. (c) SMES current.

B. DC Voltage Disturbances

To comprehensively investigate the performance of SMES-CSDC in FRT capability enhancement of DC-DFIG, three kinds of DC voltage disturbances are set in the simulation, including DC voltage sag, voltage swell, and second-order voltage oscillation. The DC voltage sag and swell are produced by an 80% depth and a 50% height of the AC symmetrical fault, whereas the DC second-order voltage oscillation is caused by the AC-side voltage unbalance fault (80% depth of the single-phase-to-ground fault). The configurations of these three faults are in accordance with the grid code of U.S. PREPA [56]. To simplify the simulation, the wind speed is assumed constant at 11 m/s.

Figure 11 shows the responses of critical parameters without protection, i. e., terminal voltage, output current, EM torque, rotor current, and rotor speed, under three DC voltage disturbances without any protection. Overall, the responses

of these crucial parameters are in consistent with the analyses in Section III-B. Besides, the severe problems that DC voltage disturbances bring to the DC-DFIG can be concluded as follows.

1) There are two huge spikes in the EM torque and the rotor current at the fault occurrence and clearance, as analyzed in Section III. The peak values of these critical parameters are all beyond the maximum allowable values (2.0 p.u.). The rotor speed begins to fluctuate, and there is a risk of instability of the wind turbine.

2) According to the DC fault characteristic, the DC-side fault current will be rapidly changed with a considerable amplitude. As can be observed from Fig. 11, the spikes of the DC fault current all exceed 4.0 p.u. and will destroy the fragile IGBT-based converter.

3) There are vast pulsations of DC output current and DC-DFIG rotor current under DC voltage oscillations. Such tremendous pulsations will lead to severe unbalance problems in EM torque, stator, and rotor, shredding the gearbox and causing acute heating problems in the wind turbine.

Figure 12 shows the responses of those critical parameters with the protection of SMES-CSDC. The terminal voltage of DC-DFIG can be well-maintained by converter 2. All the critical parameters can be well-protected under three kinds of DC voltage disturbances. Although the spikes of the DC grid-side current cannot be eliminated, the DC grid-side current can be limited within 2.0 p.u. by converter 1. Under second-order DC voltage oscillation, the DC current pulsation can be partly suppressed within an acceptable range. Under DC voltage sag and DC voltage oscillation sag, the generated power that cannot be sent out can be temporarily stored into the SMES. Under voltage swell, the stored energy in SMES will be released by converter 1 to adjust the grid-side current. The energy conversion under three transient conditions can be reflected from the SMES current shown in Fig. 12.

C. Applications of SMES-CSDC in Multiple DC-DFIG Scenarios

To interface multiple DC-DFIGs into the DC main grid, two conceptual schemes are designed for further studying in future work.

1) Single SMES-CSDC scheme: multiple DC-DFIGs share with a common SMES-CSDC. The conceptual design of this configuration is shown in Fig. 13. The proposed SMES-CSDC can be used to connect the DC sub-grid into the DC main grid. The DC sub-grid includes multiple DC-DFIGs, ESDs, and loads. To use this scheme, it should be noted that the total output current of the DC sub-grid should be controlled within a certain range considering the available energy of the SMES in (1). A large output power of the DC sub-grid may bring a higher critical current requirement of the SMES, increasing the SMES capital cost.

2) Multiple SMES-CSDC scheme: each DC-DFIG is equipped with individual SMES-CSDC. The conceptual design of this configuration is shown in Fig. 14. Since the proposed SMES-CSDC has the potentiality of DC transformer, each DC-DFIG can be equipped with an individual SMES-CSDC.

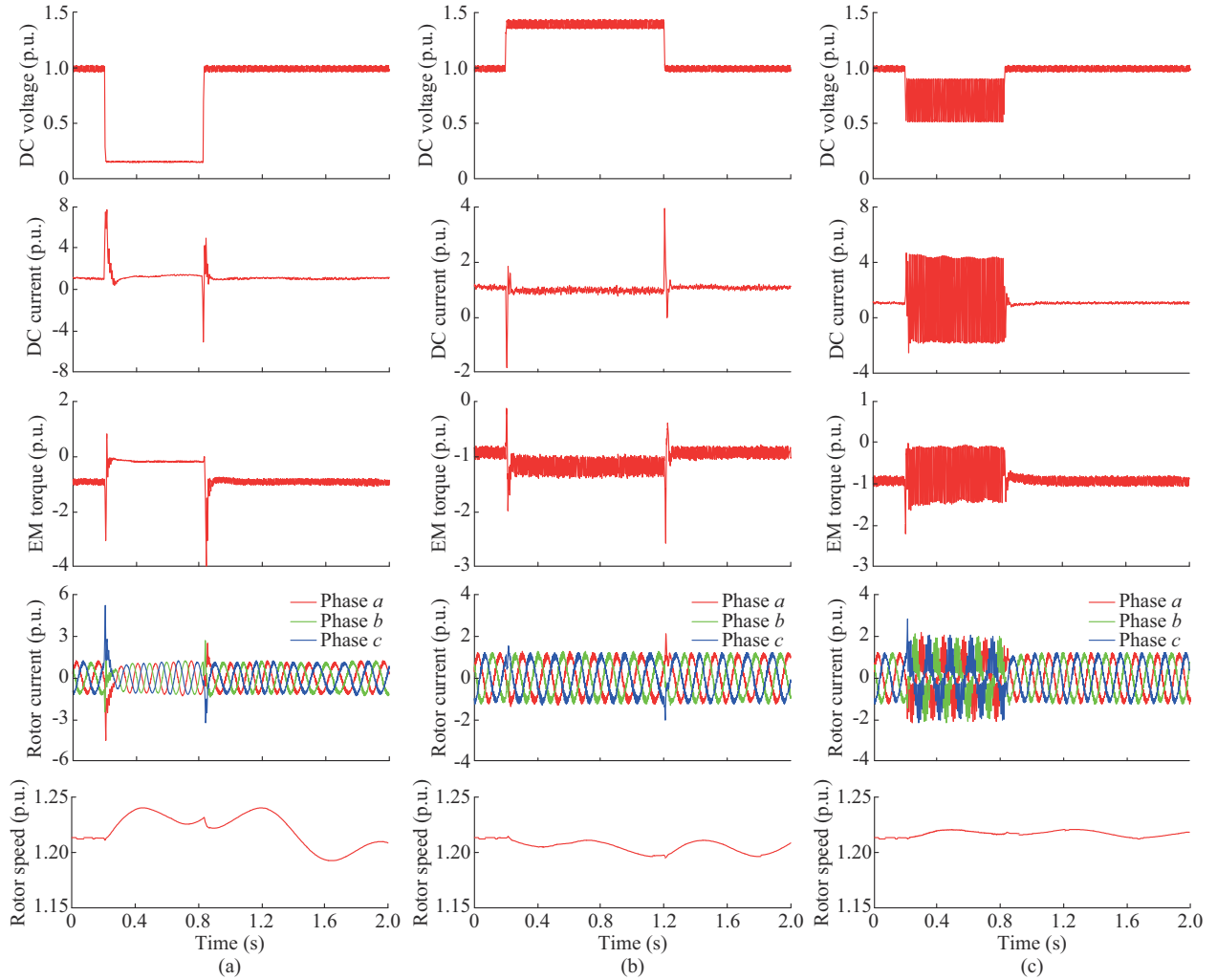


Fig. 11. Responses of of critical parameters for DC-DFIG without any protection. (a) Under DC voltage sag. (b) Under DC voltage swell. (c) Under DC voltage oscillation sag.

By this means, the DC-DFIG can be directly connected to the medium-voltage DC (MVDC) grid without using additional DC transformer. To maintain a relatively-constant SMES stored current for energy/power management, the power relationship between the two terminals of the CSDC should satisfy:

$$v_g i_g = v_L i_L \quad (47)$$

To use this scheme, it should be noted that the converters of the SMES-CSDC may require modification, as the IGBT may not afford the high voltage requirement. Input-series output-parallel (ISOP) topology [57], modular multilevel converter (MMC) [58], or multiple series IGBTs [32] can be considered in the future work.

VII. CONCLUSION

This paper depicts the power fluctuations and the transient dynamics of the emerged DC-DFIG under wind speed variations and DC voltage quality disturbances. Regarding these two urgently-addressed issues, an SMES-embedded CSDC is proposed for power management and voltage maintenance of sensitive DC renewable sources in DC power systems.

A scaled-down experiment is carried out to comprehensively validate the feasibility of the proposed SMES-CSDC. A MW-level DC-DFIG with the integration of SMES-CSDC is also established in simulation to verify the effectiveness and advantages of the SMES-CSDC for application in DC power systems. The characteristics of the SMES-CSDC are summarized as follows.

1) Serial-embedded ESD structure. Different from conventional applications of SMES which requires a multi-stage structure to interface the DC bus, the proposed device embeds the SMES in series in the DC link of the two converters. This embedded design avoids using additional converter to access the ESD.

2) Unified management of voltage and current. Regarding the design in 1), the proposed SMES-CSDC provides a combined function of maintaining the DC load voltage and regulating the grid-side current and power simultaneously.

3) Ripple elimination. It is noteworthy that with an SMES-CSDC as a buffer, the second-order harmonic influences can be well-suppressed without additional complex control strategies like PI-R controller.

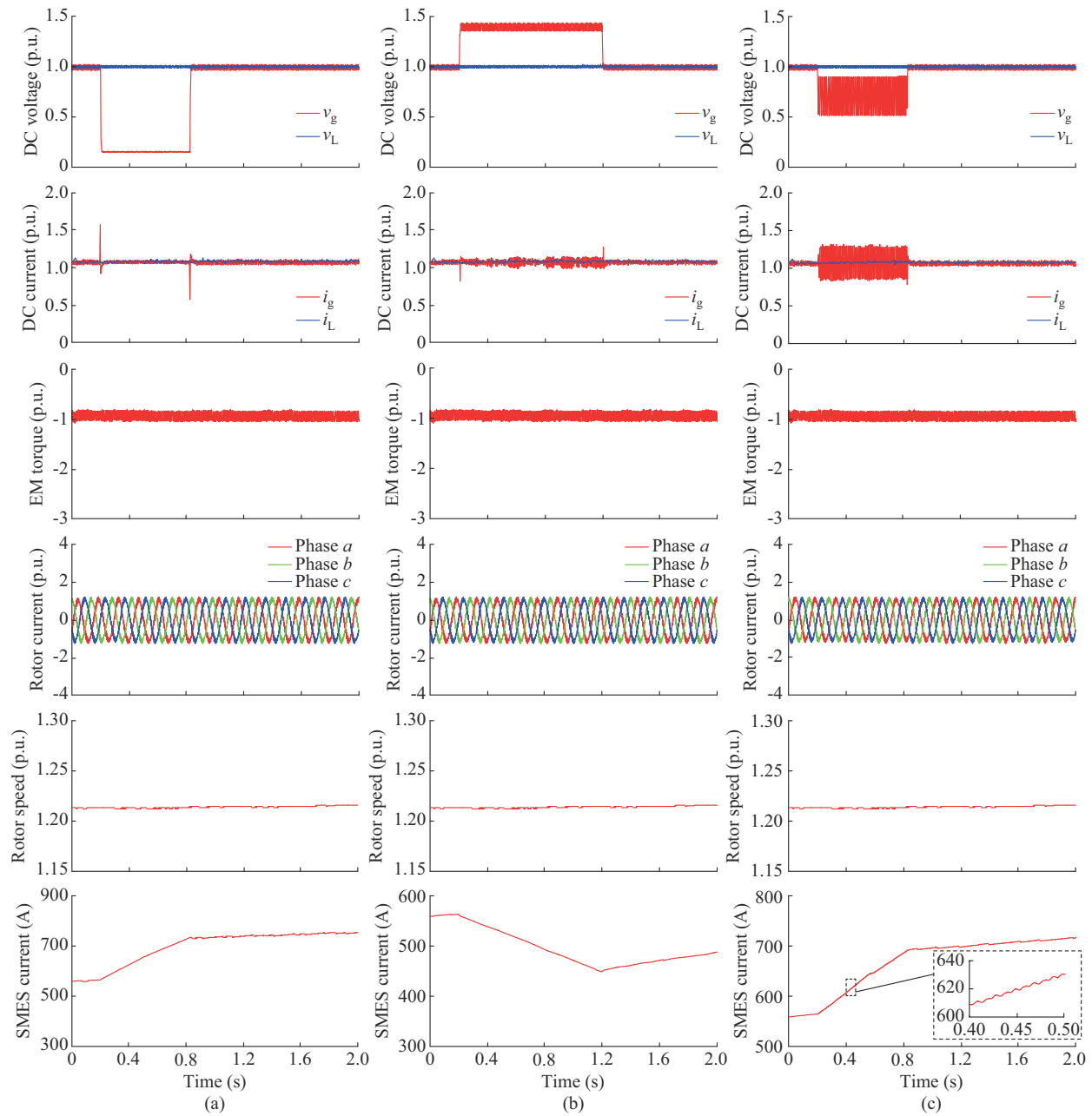


Fig. 12. Responses of critical parameters for DC-DFIG with SMES-CSDC. (a) Under DC voltage sag. (b) Under DC voltage swell. (c) Under DC voltage oscillation sag.

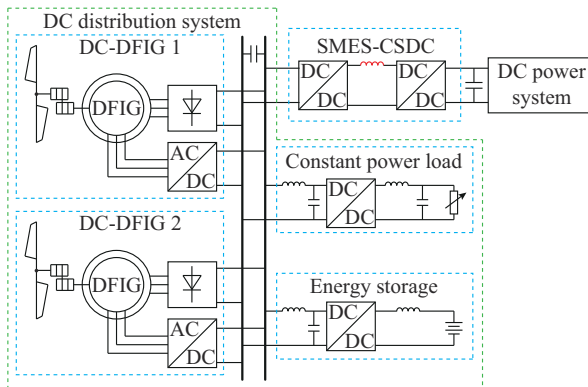


Fig. 13. Conceptual design of multiple DC-DFIGs connected into main grid for scheme 1.

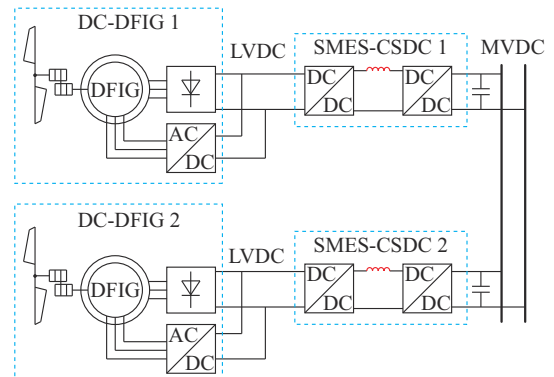


Fig. 14. Conceptual design of multiple DC-DFIGs connected into main grid for scheme 2.

APPENDIX A

TABLE AI
EXPERIMENTAL PARAMETERS OF SMES-CSDC

Parameter	Symbol	Value
SMES inductance	L_{SC}	10.1 mH
Critical current of SMES	I_{SCmax}	120 A
Capacitor	C_1, C_2	3 mF
DC source		300 V/40 A
Rated load voltage	V_L	36 V
Rated load current	I_L	12 A
Metal-oxide-semi conductor field-effect transistor (MOSFET)		IPT007N06N, 60 V/300 A

TABLE AII
SIMULATION PARAMETERS OF 1 MW DC-DFIG

Parameter	Symbol	Value
Rated power	P_L	1 MW
Rated DC voltage	V_L	3 kV
Rated stator frequency	f_s	60 Hz
Rated stator voltage	V_s	2 kV
Mutual inductance	L_m	2.9 p.u.
Stator resistance and inductance	R_s, L_s	0.007 p.u., 3.071 p.u.
Rotor resistance and inductance	R_r, L_r	0.005 p.u., 3.056 p.u.
Pair of poles	N_p	2
Turn ratio	N_s/N_r	0.4

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