

Enhanced AC Fault Ride-through Control for MMC-integrated System Based on Active PCC Voltage Drop

Haihan Ye, Wu Chen, Heng Wu, Wu Cao, Guoqing He, and Guanghui Li

Abstract—When a renewable energy station (RES) connects to the rectifier station (RS) of a modular multilevel converter-based high-voltage direct current (MMC-HVDC) system, the voltage at the point of common coupling (PCC) is determined by RS control methods. For example, RS control may become saturated under fault, and causes the RS to change from an equivalent voltage source to an equivalent current source, making fault analysis more complicated. In addition, the grid code of the fault ride-through (FRT) requires the RES to output current according to its terminal voltage. This changes the fault point voltage and leads to RES voltage regulation and current redistribution, resulting in fault response interactions. To address these issues, this study describes how an MMC-integrated system has five operation modes and three common characteristics under the duration of the fault. The study also reveals several instances of RS performance degradation such as AC voltage loop saturation, and shows that RS power reversal can be significantly improved. An enhanced AC FRT control method is proposed to achieve controllable PCC voltage and continuous power transmission by actively reducing the PCC voltage amplitude. The robustness of the method is theoretically proven under parameter variation and operation mode switching. Finally, the feasibility of the proposed method is verified through MATLAB/Simulink results.

Index Terms—Modular multilevel converter-based high-voltage direct current (MMC-HVDC) system, fault ride-through (FRT), voltage loop saturation, continuous power transmission, point of common coupling (PCC), active voltage drop control.

I. INTRODUCTION

WITH the increase in the number of installations of large-scale renewable energy stations (RESs), their

stable control and transmission are urgently demanded. A modular multilevel converter based high-voltage direct current (MMC-HVDC) can not only avoid commutation failure and reactive power compensation, but also build grid-connected voltage at the point of common coupling (PCC), thereby avoiding the need for large-capacity thermal power plant construction or AC grid expansion in remote areas. Thus, MMC-HVDC is a mainstream option for islanded renewable energy transmission.

Each RES interfaces the rectifier station (RS) of the MMC-HVDC through the PCC, which poses a high risk for an AC fault due to the large number of interconnected transmission lines. With a focus on fault analysis and fault ride-through (FRT), numerous studies have been conducted. However, they have mainly focused on grid-connected systems. References [1]–[3] considered the existence of equilibrium points of permanent magnetic synchronous generator (PMSG) systems under low-voltage ride-through (LVRT), and eigenvalue trajectory was adopted to analyze system stability during the fault steady state. Both symmetric and asymmetric faults of modular multilevel converter (MMC) connected to a power grid were analyzed in [4], and q -axis current reduction was recommended to suppress the overcurrent. Directed arm current control was proposed to suppress DC current oscillation in [5], and the superiority of vertical balance control was demonstrated in comparison with energy-based control under an asymmetric fault in [6].

These previous studies focused on grid-connected systems, where the power grid could be Thevenin equivalent to an ideal voltage source in series with line impedance. Unlike the classic grid-connected system, the RS external response in an MMC-integrated system is determined by the RS AC voltage loop, which may become saturated under the fault, causing the RS to change from an equivalent voltage source to an equivalent current source [7]. Under these conditions, the voltage at the fault point is affected by multiple factors that produce greater challenges for fault analysis. The AC fault of an MMC-integrated system was analyzed in [8], and DC voltage oscillation was determined to have been caused by unbalanced MMC internal energy. However, analysis was limited to the DC side, thus mostly ignoring the AC side of the FRT. The PCC overvoltage caused by the saturation of the RS AC voltage loop was reported in [9], and several strategies were then proposed to clear the integrator of the

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proportional-integral (PI) controller. This overvoltage can be suppressed by the anti-windup in the PI controller. This is a commonly used method but has little to do with fault response. PCC overvoltage suppression under an asymmetric fault without introducing negative sequence (NS) current was studied in [10]. However, the theoretical analysis in the study was insufficient, and numerical calculations were not conducted, thus preventing the veracity of the analysis from being verified. Unlike NS current suppression, NS voltage suppression was recommended in [11] because NS current suppression control maintains NS PCC voltage following single-phase-to-ground (P-G) fault clearance, which hinders system restoration from the fault and results in FRT failure. However, NS voltage suppression does not generate a response under a symmetric fault and thus does not additionally contribute to symmetric AC FRT. Fault current injection in an RS q -axis current reference was adopted in [12] to trigger overcurrent protection. This type of method realizes AC FRT through reasonable fault detection and circuit breaker configuration. However, considerable transmitted power is lost, and recovery after fault clearance is required, which is time-consuming. In addition, the aforementioned studies mainly focused on the solid fault, where the resistance of the fault point was 0. The validation under the solid fault only proves the validity of the proposed method under specific case, but it does not ensure its effectiveness under uncertainties.

Based on existing studies, the fault response under RES and RS control switching must be further examined, and the FRT method for an MMC-integrated system under multiple uncertainties must be improved. Accordingly, symmetric and asymmetric faults of an MMC-integrated system are fully analyzed in this study, and a high-performance FRT method is proposed, with its effectiveness demonstrated under parameter variations. The contributions of this study are described as follows.

1) The responses of symmetric and asymmetric faults under an MMC-integrated system are demonstrated. Under a symmetric fault, the MMC-integrated system has five operation modes and three common characteristics, and controllable PCC voltage and continuous power transmission are possible by optimizing PCC voltage. Under an asymmetric fault, NS voltage suppression rather than NS current suppression is adopted, and RS overcurrent and saturated modulation can be observed.

2) A high-performance AC FRT method is proposed. The proposed method can maintain continuous power transmission under fault, which is very helpful in blocking the unbalanced power that flows from the DC grid to the fault point. In addition, RS overcurrent and saturated modulation under an asymmetric fault can be effectively suppressed.

The remainder of this paper is organized as follows. Section II introduces the system description, where a basic block of the system model is presented to describe the research scope of the study. Section III analyzes the symmetric AC faults, including the RES and RS operation modes and solutions to the RS equilibrium points under fault resistance variation. Section IV analyzes asymmetric AC faults based

on the findings from the Section III. Section V presents the active PCC voltage drop control, where the RS continuous power transmission area is identified and the maximum power transmission curve is derived. Moreover, the effective range calculation is conducted, and the robustness of the method is verified. Section VI presents simulation verification, where the veracity of the theoretical analysis and of the proposed method are proven through MATLAB/Simulink results. Finally, conclusions are given in Section VII.

II. SYSTEM DESCRIPTION

The block of an RES connected to the MMC-HVDC system is shown in Fig. 1, where u_r and i_r are the RS terminal voltage and input current, respectively; and R_f is the fault resistance.

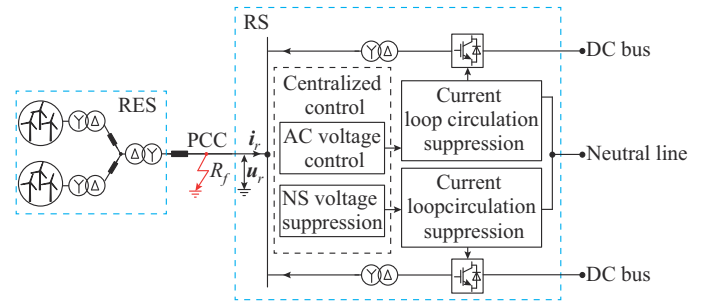


Fig. 1. Block of an RES connected to MMC-HVDC system.

RESs are commonly used as models of lumped controllable current sources with choppers and grid-side inverters [13], [14], where the current references of all RESs must be determined by FRT grid code [15], [16]. An RES control algorithm is composed of a DC voltage loop, current loop, NS current suppression, and phase locked loop (PLL) based on the all-pass filter [17], [18].

The AC transmission line can be characterized by lumped resistor-inductor (RL) model [9], [19] because the results between the aggregated parameter model and distributed line model under fault detection and analysis have proven to be very similar [20], [21]. In this study, measured data from the Zhangbei DC project of China was adopted for calculating equivalent line impedance, where 0.175 p.u. of reactive power is required when 1 p.u. of active power is transmitted.

The AC fault, marked red in Fig. 1, is generally modeled by fault resistance R_f [22]-[24]. Both symmetric and asymmetric faults are studied, and the NS voltage suppression recommended by [11] is adopted in the RS. Analysis can be conducted in a classic two-terminal system, a multi-terminal system, or even a DC grid, as AC and DC fault characteristics are decoupled by MMC internal energy under unsaturated modulation [13], [25].

The RS adopts a bipolar configuration, where both positive and negative converters are half-bridge MMCs with identical parameters. The MMC in the RS adopts a detailed equivalent model based on double diodes [26], and its control algorithms are composed of classic rated AC voltage control, NS voltage suppression, current loop, circulating current suppression [27], and third harmonic injection [28].

Wherein classic AC voltage control and NS voltage suppression form a centralized control, but the other control methods are distributed in both poles.

III. SYMMETRIC AC FAULT ANALYSIS

A. Normal Operation Mode with RS Positive Power Flow

If the power loss at the fault point is less than the RES output power, the RS receives the residual power and continuously transmits it to the DC bus. In this case, the absolute value of RS current reference i_{rdref} is less than its limitation value I_{rmax} , and thus, the d -axis PI controller of the RS AC voltage loop is not saturated, and u_r can be controlled to be the rated value U_{rn} .

The critical R_f value can be calculated by the constraint that the RS received power is greater than 0:

$$\begin{cases} P_r = P_s - 1.5 U_r^2 / R_f \geq 0 \\ U_r = U_{rn} \end{cases} \quad (1)$$

where P_s and P_r are the active power output by the RES and that transmitted to the RS, respectively; and U_r and U_{rn} are the measured and rated amplitudes of u_r , respectively.

The main parameters of simulation are listed in Table I, where P_{base} is the base of the power; P_{sn} and u_{dcn} are the rated values of the RES output power and DC bus voltage, respectively; ω_s is the rated angular frequency; k_s and k_r are the turn ratios of the RES- and RS-side transformers, respectively; and L_{ac} is the equivalent collector line inductance. Figure 2 presents the simulation results when $R_f = 30 \Omega$, where u_{sa} is the a-phase voltage waveform of the equivalent RES terminal voltage u_s ; and i_{sq} is the q -axis current of the equivalent RES terminal current i_s . The fault occurs at 0.6 s and clears at 1 s.

TABLE I
MAIN PARAMETERS OF SIMULATION

Symbol	Value	Symbol	Value	Symbol	Value
P_{base}	3000 MW	P_{sn}	2250 MW	U_{rn}	230 kV
u_{dcn}	500 kV	ω_s	100π	k_s	35/230
L_{ac}	13.08 mH	I_{rmax}	1.133 p.u.	k_r	230/290

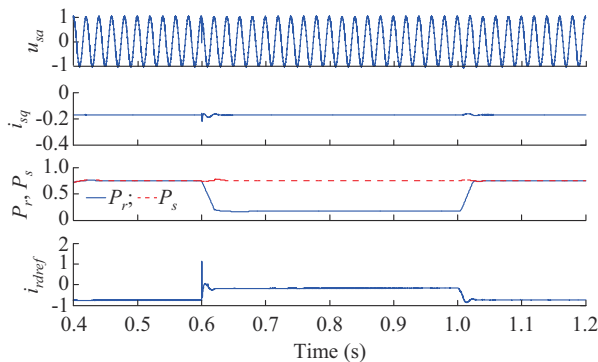


Fig. 2. Simulation results when $R_f = 30 \Omega$.

In Fig. 2, u_{sa} and i_{sq} remain stable during the fault, indicating that PCC voltage can be controlled to be the rated value,

and the RES continues to operate in the rated mode. P_r decreases but is greater than 0, and therefore the continuous power transmission holds. $|i_{rdref}|$ does not reach I_{rmax} , and thus the RS voltage loop is valid in maintaining rated PCC voltage.

B. Normal Operation Mode with RS Negative Power Flow

When the RES output power is less than the power loss of the fault point, the RS active power flow is reversed. If $|i_{rdref}| < I_{rmax}$, the PI controller of the RS AC voltage loop is not saturated, and u_r is still controlled to be the rated value under the AC fault:

$$\begin{cases} P_s - 1.5 U_r^2 / R_f \leq -P_{rmax} \\ U_r = U_{rn} \end{cases} \quad (2)$$

where $P_{rmax} = 1.5 U_r I_{rmax}$ is the RS output power limitation.

Figure 3 presents the simulation results when $R_f = 15 \Omega$. The waveforms of u_{sa} and i_{sq} are similar to those shown in Fig. 2, and the RES operates under rated mode during the fault. However, P_r decreases to less than 0 during the period of 0.6–1 s. Thus, the RS power flow is reversed. In addition, i_{rdref} is increased but does not reach I_{rmax} , which means the RS voltage loop remains effective in this case.

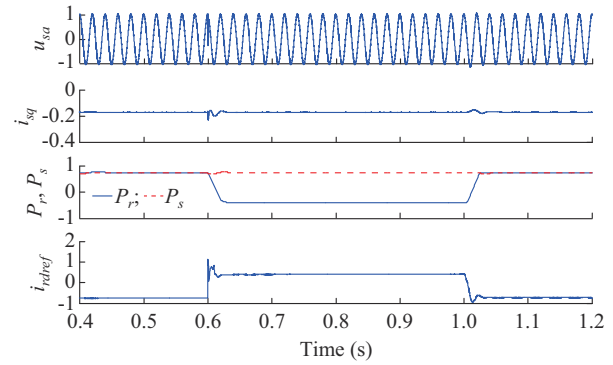


Fig. 3. Simulation results when $R_f = 15 \Omega$.

C. RES Normal Operation Mode Under RS Current Limitation Mode

If $|i_{rdref}|$ reaches I_{rmax} , the PI controller of the RS AC voltage loop is saturated, and RS becomes a constant current source. In this case, the PCC voltage is out-of-control and its amplitude is determined by the RES output current, I_{rmax} , and R_f .

If the amplitude of u_s remains higher than 0.9 p.u., the RES does not enter LVRT mode:

$$\begin{cases} \frac{0.9 U_{sn}}{k_s} \geq j \omega_s L_{ac} k_s (i_{sd} + j i_{sq}) + U_r \\ U_r = R_f (k_s i_{sd} + I_{rmax}) \end{cases} \quad (3)$$

where U_{sn} is the rated value of the amplitude of u_s ; and i_{sd} is the d -axis current of i_s , which can be regarded as a rated value because the RES remains in normal operation mode.

Figure 4 shows the simulation results when $R_f = 8.5 \Omega$. The amplitude of u_{sa} drops from 1.04 to 0.96 p.u., and i_{sq} remains stable during the AC fault. Thus, RES does not enter

LVRT mode. Because $i_{rdref} = I_{rmax}$, the PI controller of the voltage loop is saturated, and the PCC voltage is out-of-control. P_r decreases to less than 0, and thus the power transmission is reversed in this case.

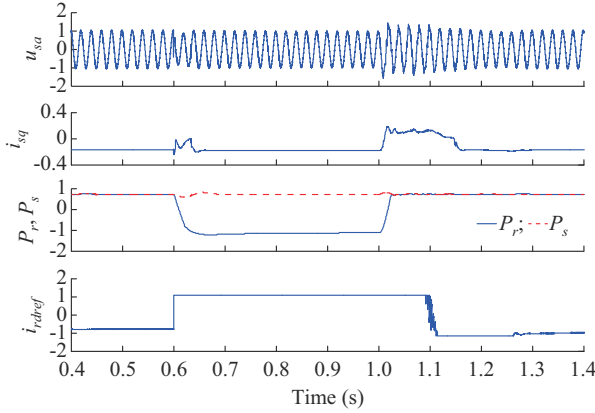


Fig. 4. Simulation results when $R_f = 8.5 \Omega$.

Because of the saturation of the voltage loop, the output value of the PI integrator keeps increasing and causes overvoltage of u_{sa} [9]. Thus, i_{sq} is reversed and RES enters high-voltage ride-through (HVRT) after fault clearance, as shown in Fig. 4, where the anti-windup PI controller should be adopted to terminate the output value of the PI integrator and suppress PCC overvoltage.

D. RES LVRT Mode with RS Current Limitation Mode

When R_f is further decreased, the RES and RS output power can no longer maintain normal PCC voltage, and thus the RES begins to enter LVRT mode.

In this case, the fault point voltage is:

$$U_r = R_f \left(k_s \sqrt{I_{sn}^2 - i_{sq}^2} + i_{rmax} \right) \quad (4)$$

where I_{sn} is the rated value of i_s .

Based on the LVRT standard [15], [16], the RES output reactive current is expressed as:

$$i_{sq} = -1.5 \times \left(0.9 - U_s/U_{sn} \right) I_{sn} \quad (5)$$

According to (4) and (5), the relationship between U_r and U_s must first be solved to obtain the critical value of R_f in this case.

The voltage equation given in Fig. 1 under the $\alpha\beta$ frame is:

$$\frac{u_{sa\beta}}{k_s} = L_{ac} k_s \frac{di_{sa\beta}}{dt} + u_{ra\beta} \quad (6)$$

where subscript $\alpha\beta$ denotes the $\alpha\beta$ frame.

Equation (6) is transformed into the PLL frame:

$$u_{sdq} = k_s^2 L_{ac} (s + j\omega_{PLL}) i_{sdq} + k_s u_{rdq} \quad (7)$$

where subscript dq denotes the PLL frame; and ω_{PLL} is the angular frequency measured by the RES PLL.

Combined with the final value theorem, the fault steady-state equation of (7) becomes:

$$u_{sdq} = j\omega_s k_s^2 L_{ac} i_{sdq} + k_s u_{rdq} \quad (8)$$

As u_s is oriented to the d -axis by the RES PLL, (8) can be simplified as:

$$\begin{cases} U_s = -\omega_s k_s^2 L_{ac} i_{sq} + k_s u_{rd} \\ 0 = \omega_s k_s^2 L_{ac} i_{sd} + k_s u_{rq} \end{cases} \quad (9)$$

where u_{rd} and u_{rq} are d - and q -axis components of u_r , respectively.

Equation (9) can be revised as:

$$U_s = k_s \sqrt{U_r^2 - (\omega_s k_s L_{ac} i_{sd})^2} - \omega_s k_s^2 L_{ac} i_{sq} \quad (10)$$

As i_{sd} is calculated by I_{sn} in the AC fault, we can obtain:

$$U_s = k_s \sqrt{U_r^2 - \omega_s^2 k_s^2 L_{ac}^2 (I_{sn}^2 - i_{sq}^2)} - \omega_s k_s^2 L_{ac} i_{sq} \quad (11)$$

Equation (11) can then be solved as:

$$i_{sq} = \frac{k_s^2 U_r^2 - I_{sn}^2 \omega_s^2 L_{ac}^2 k_s^4 - U_s^2}{2\omega_s L_{ac} U_s k_s^2} \quad (12)$$

When (5) is combined with (12), PCC voltage amplitude U_r under the fault steady state can be expressed as:

$$U_r = \frac{1}{k_s} \sqrt{U_s^2 + I_{sn}^2 \omega_s^2 L_{ac}^2 k_s^4 - 3\omega_s L_{ac} U_s I_{sn} k_s^2 \left(0.9 - \frac{U_s}{U_{sn}} \right)} \quad (13)$$

When (5) and (13) are substituted into (4), the relationship between R_f and U_s can be solved.

Figure 5 shows the simulation results when $R_f = 5 \Omega$. The amplitude of u_{sa} is close to 0.59 p.u., which can be obtained by (13). i_{rdref} reaches I_{rmax} , and thus the RS AC voltage loop is saturated, and the PCC voltage is out-of-control in this case. i_{sq} increases in the opposite direction, indicating that the RES enters LVRT mode. The RS becomes the constant current source with the value of I_{rmax} , and transmission power is reversed. Overvoltage is suppressed (compare this with Fig. 4) because anti-windup is added to the PI controller of the RS AC voltage loop.

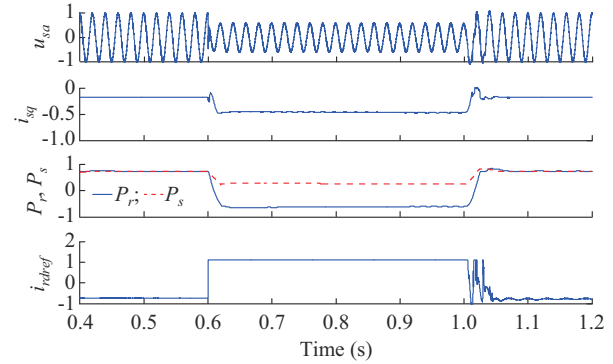


Fig. 5. Simulation results when $R_f = 5 \Omega$.

E. Current Limitation Mode of RES and RS

When R_f further decreases, the RES output current reaches its limitation, and therefore, both the RES and RS become constant current sources. Substituting these constraints into (10) and (4) yields:

$$\begin{cases} U_s = k_s U_r - \omega_s L_{ac} i_{sq} k_s^2 \\ U_r = R_f I_{rmax} \end{cases} \quad (14)$$

Simulation results when $R_f = 0.01 \Omega$ are shown in Fig. 6. Both i_{sq} and i_{rd} reach their limitations, and thus RES and RS can be treated as constant current sources with limitation values. Substituting these limitations into (14) obtains $U_s =$

0.184 p.u., which is consistent with the amplitude of u_{sa} shown in Fig. 6. As $R_f \approx 0$, PCC voltage is very close to 0 and thus $P_r = 0$, as shown in Fig. 6.

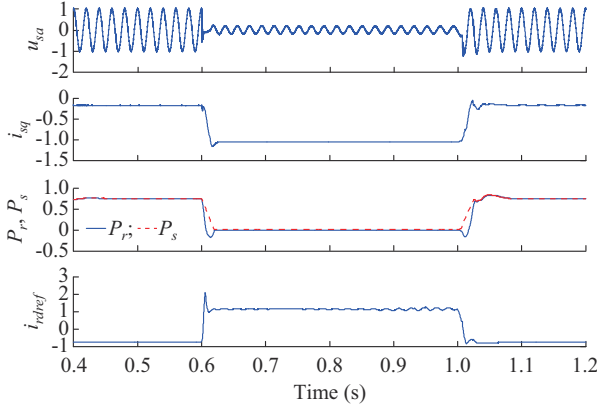


Fig. 6. Simulation results when $R_f = 0.01 \Omega$.

The system operation mode under R_f variation is shown in Fig. 7. Based on (1)-(4), (13), (14), and Table I, the RS equilibrium curve under a symmetric fault is shown in Fig. 8. In Figs. 7 and 8, the green line indicates the area of controllable PCC voltage and continuous power transmission; the red line denotes the area of the controllable PCC voltage but interrupted power transmission; and the purple line indicates the area of the out-of-control PCC voltage and interrupted power transmission.

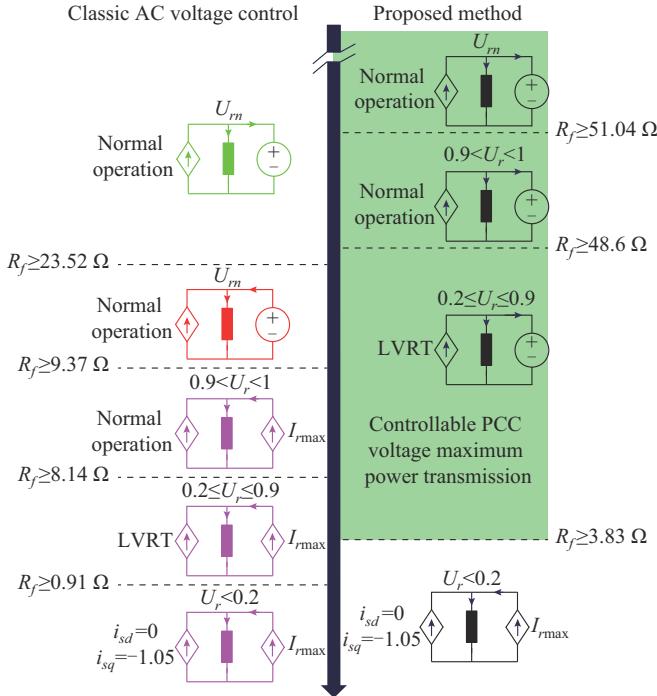


Fig. 7. System operation mode under R_f variation.

Figures 7 and 8 show that the system has five operation modes and three fault characteristics. Thus, the state space equations are discontinuous, making fault calculation and optimized design rather challenging. In addition, out-of-control PCC voltage and RS power transmission interruption occur under multiple modes.

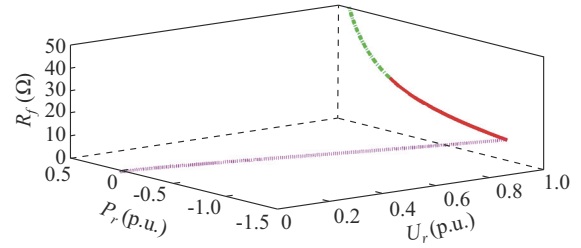


Fig. 8. RS equilibrium curve under a symmetric fault.

IV. ASYMMETRIC AC FAULT ANALYSIS

Asymmetric fault characteristics are studied based on the results presented in Fig. 8, and the P-G fault is adopted as an example for analysis.

Three-phase voltages, u_a , u_b , and u_c are expressed as:

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = \begin{bmatrix} U^+ \cos(\omega_s t + \theta^+) \\ U^+ \cos(\omega_s t + \theta^+ - 2\pi/3) \\ U^+ \cos(\omega_s t + \theta^+ + 2\pi/3) \end{bmatrix} + \begin{bmatrix} U^- \cos(\omega_s t + \theta^-) \\ U^- \cos(\omega_s t + \theta^- + 2\pi/3) \\ U^- \cos(\omega_s t + \theta^- - 2\pi/3) \end{bmatrix} \quad (15)$$

where the superscripts + and - denote the positive sequence (PS) and NS components, respectively; and U and θ are the magnitude and phase of the voltage, respectively.

The Clarke transformation is applied to (15), and the result can be rewritten in an exponential form:

$$\mathbf{u}_{\alpha\beta} = U^+ e^{j(\omega_s t + \theta^+)} + U^- e^{-j(\omega_s t + \theta^-)} \quad (16)$$

Transforming (6) into the global PS and NS rotating frame yields:

$$\mathbf{u}_{dq} = U^+ e^{j\theta^+} + U^- e^{-j\theta^-} = \mathbf{u}_{dq}^+ + \mathbf{u}_{dq}^- \quad (17)$$

where $\bar{(\cdot)}$ means the conjugate. Equations (15)-(17) show that a conjugate operation is required to transform the NS component from the three-phase frame to the rotating frame. Based on the aforementioned transformations, the sequential network is built in the rotating frame to connect the control method of the RS and RES and the response of the fault point.

Reference [11] recommends NS voltage suppression, where the sequence network under the P-G fault is shown in Fig. 9, in which the superscript z denotes the zero sequence (ZS) component; and R_{sg} and R_{rg} are the transformer grounding resistance at the RES and RS sides, respectively.

Figure 9 shows that the current operation mode of the RES and RS must be judged in real time, and thus an iterative calculation is needed for fault analysis.

According to the superposition theorem, we can obtain:

$$\begin{cases} \mathbf{u}_s^+ = k_s^2 \mathbf{i}_s^+ \mathbf{Z}_{ac} + k_s \mathbf{u}_r^+ \\ \mathbf{u}_s^- = k_s^2 \mathbf{i}_s^- \mathbf{Z}_{ac} \\ \mathbf{i}_r^+ = k_s \mathbf{i}_s^+ - \mathbf{u}_r^+ / \mathbf{Z}_{dem} \\ \mathbf{i}_r^- = k_s \mathbf{i}_s^- - \mathbf{u}_r^- / \mathbf{Z}_{dem} \\ \mathbf{Z}_{dem} = 3R_f + \frac{3R_{rg}(\mathbf{Z}_{ac} + 3R_{sg})}{3R_{sg} + \mathbf{Z}_{ac} + 3R_{rg}} \end{cases} \quad (18)$$

where \mathbf{Z}_{ac} denotes the line impedance.

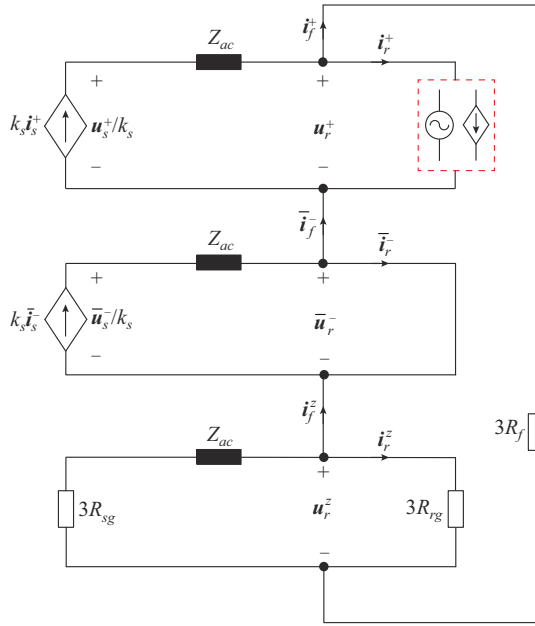


Fig. 9. Sequence network under a P-G fault when RS adopts NS voltage suppression.

The absolute value of the NS voltage equation in (18) is:

$$U_s^- = k_s^2 \sqrt{R_{ac}^2 + (\omega_s L_{ac})^2} |\bar{i}_s^-| \quad (19)$$

where U_s^- is the amplitude of \bar{u}_s^- ; and R_{ac} is the resistance component of Z_{ac} .

The NS current specified by the grid code is:

$$\begin{cases} i_{sd}^- = 0 \\ i_{sq}^- = k_{iq}^- I_{sn} U_s^- / U_{sn} \end{cases} \quad (20)$$

where k_{iq}^- is the NS reactive current coefficient.

Combining (19) and (20) yields:

$$U_s^- = k_s^2 \sqrt{R_{ac}^2 + (\omega_s L_{ac})^2} k_{iq}^- I_{sn} U_s^- / U_{sn} \quad (21)$$

Obviously, the solution to (21) is $U_s^- = 0$. From (20), i_{sq}^- equals 0. Therefore, no NS component exists in the RES during a P-G fault. However, an NS current is generated, which may cause RS overcurrent and saturated modulation during AC FRT.

The MMC valve-side voltage equation and modulation ratio M_r in Fig. 1 are expressed as:

$$\begin{cases} \mathbf{u}_r / k_r e^{j\frac{\pi}{6}} = j\omega_s L_{req} k_r \mathbf{i}_{rp} + \mathbf{u}_m \\ M_r = 2U_m / (1.15u_{dcn}) \end{cases} \quad (22)$$

where L_{req} is the equivalent MMC inductor; \mathbf{u}_m is the MMC valve-side voltage; U_m is the amplitude of \mathbf{u}_m ; and \mathbf{i}_{rp} is the current of the RS positive pole, which equals $(\mathbf{i}_r^+ + \mathbf{i}_r^-)e^{j\pi/6}/2$.

Solving (18) and (22) yields M_r and the amplitude of \mathbf{i}_{rp} (I_{rp}), as shown in Fig. 10 and verified by Fig. 11. In Fig. 11, \mathbf{i}_s exhibits a pure sinusoidal shape, and thus the NS component is not contained. The amplitude of \mathbf{i}_r is 1.56 p.u., and RS modulation \mathbf{m}_r is saturated, which must be considered under FRT design.

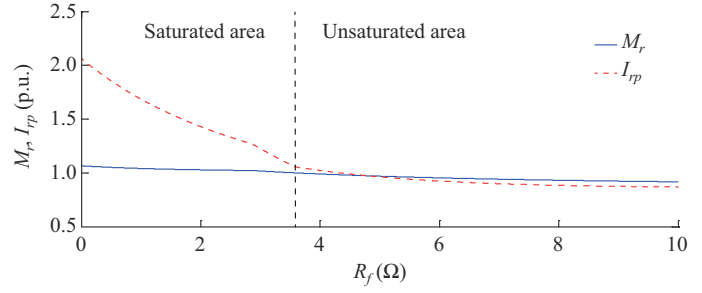


Fig. 10. I_{rp} and M_r under a P-G fault.

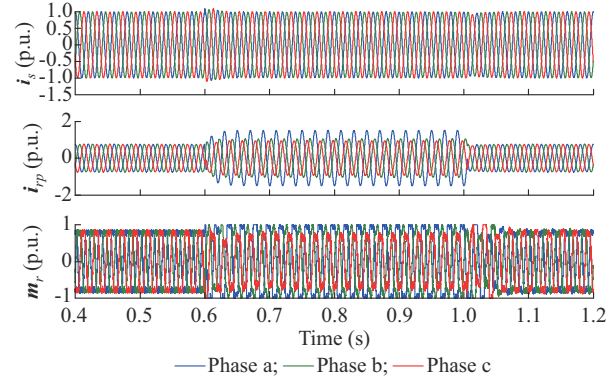


Fig. 11. Simulation results under a P-G fault ($R_f = 1 \Omega$).

V. ACTIVE PCC VOLTAGE DROP CONTROL

A. Control Design

Figure 7 shows that although RES has the modes of rated operation, LVRT, and current limitation under an AC fault, the response of the LVRT mode should strictly meet the FRT grid code, and the rated operation and current limitation modes cannot be easily optimized. Thus, the RES leaves little degree of freedom for improvement. For this reason, this study optimizes the FRT curve shown in Fig. 8 by changing the RS fault response.

From the analysis in Section III, if U_m is adopted as the reference of RS AC voltage control, the fault response is uniquely determined, as shown in Figs. 7 and 8, and thus the freedom of RS optimization remains lost. Therefore, the reference of RS AC voltage control is changed as an independent variable to provide the freedom for FRT optimization, after which an optimal voltage reference is determined by analyzing the influence of the RES on the RS during the AC fault. This is necessary when designing an enhanced FRT control and optimizing the equilibrium curve.

If the RS AC voltage loop is unsaturated, the general expression of transmitted power is:

$$P_r = 1.5U_s \sqrt{I_{sn}^2 - i_{sq}^2} - 1.5U_r^2 / R_f \quad (23)$$

Combined with RES LVRT mode analysis, (5) and (13) are substituted into (23), and the result of $P_r \geq 0$ is plotted in Fig. 12.

In Fig. 12, the three-dimensional (3D) surface is the solution to (23) larger than 0, the solid grid plane is $P_r = 0$, and the 3D curve equals the equilibrium curve shown in Fig. 8, where the pink, red, and green segments in the 3D curve cor-

respond to the pink, red, and green modes in the left of Fig. 7, respectively. The solid and dashed segments in the 3D curve are below the solid grid plane, which means the RS input power is reversed under this part. However, the corresponding 3D surface remains, and thus continuous power transmission during the fault period is theoretically feasible. Therefore, continuous power transmission during an AC fault can be realized by moving the RS equilibrium point from the 3D curve to the 3D surface, where the reversed power shown in Figs. 3-5 and the red and pink modes presented in Figs. 7 and 8 can be effectively avoided. In addition, the optimal selection of the equilibrium point on the 3D surface can realize the maximum power transmission under a fault steady state.

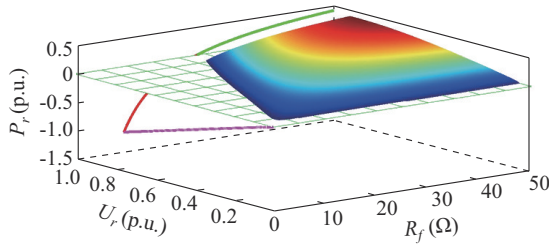


Fig. 12. RS active power under LVRT mode.

Both the colored surface and green areas of the 3D curve in Fig. 12 satisfy $P_r \geq 0$, where the green areas of the 3D curve indicate that the RES and RS are in rated operation modes. Solving (23), i.e., $P_r \geq P_{sn} - 1.5U_{rn}^2/R_f$ to obtain optimal transmitted power yields the result shown in Fig. 13. The 3D curve is the maximum power transmission curve of the 3D surface and yields the desired equilibrium points for obtaining the maximum transmission under different R_f scenarios. The specific derivation of this curve can be found in Appendix A. To reduce the requirement for fault detection, the relationship between P_r and U_r on the solid line in Fig. 13 is fitted to Fig. 14.

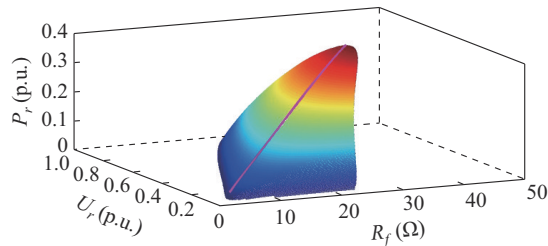


Fig. 13. RS active power optimization.

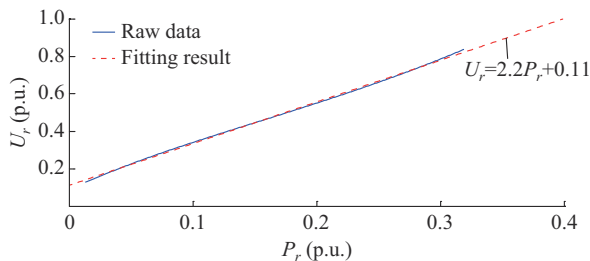


Fig. 14. Proposed fault ride-through function.

In addition to the maximum power transmission, active PCC voltage drop can not only help reduce voltage error, desaturate the PI controller, and suppress the PCC overvoltage after fault clearance, but also decrease the current loop feed-forward to avoid over-modulation, as shown in Fig. 11. When combined with (18), the NS current can also be suppressed after PCC voltage is reduced. Thus, the RS overcurrent shown in Fig. 10 can be significantly improved. Therefore, the aforementioned method is more advanced than the widely used current limitation mode of all sources under an AC fault.

To avoid algorithm switching during a fault, the fitting result shown in Fig. 14 is extended to $U_r = 1$:

$$U_r = (2.2P_r + 0.11)U_{rn} \quad P_r \in [0.01, 0.4] \text{ p.u.} \quad (24)$$

According to (24), when an AC fault occurs, P_r decreases immediately, and thus the proposed method actively reduces U_r to move the RS equilibrium point to the maximum power transmission curve shown in Fig. 13. When the fault is cleared, P_r increases immediately, and the proposed method actively increases U_r . From Fig. 14, P_r is further increased, and the positive feedback is constituted until U_r reaches U_{rn} . Therefore, fault detection is not required. To avoid steady-state undervoltage under low wind speed, a trigger signal k_t is added:

$$k_t = \begin{cases} 1 & U_r < 0.9U_{rn} \text{ and } P_r < 0.4P_{base} \\ 0 & \text{otherwise} \end{cases} \quad (25)$$

where 0.9 p.u. is the lower limitation of normal PCC voltage; and 0.4 p.u. is the maximum value of P_r in (24).

Combining (24) and (25) enables us to generate the proposed method, given as Fig. 15, where k_p is the coefficient of the minimum power constraint; and $0.13U_{rn}$ is derived from the lower limitation of (24).

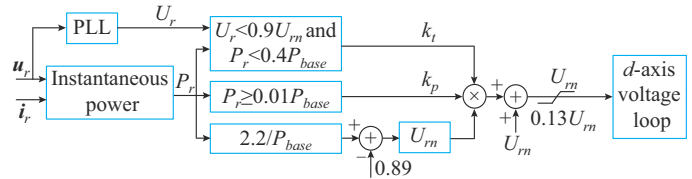


Fig. 15. Block of proposed method.

When $P_r < 0.01$ p.u., the RS equilibrium point violates the constraint in (24), $k_p = 0$, and the proposed method is equal to the rated AC voltage control. Similarly, when U_r and P_r violate (25), $k_t = 0$ and the proposed method also becomes the rated AC voltage control to avoid steady-state PCC undervoltage. When $k_p = k_t = 1$, the output of (24) is activated to output the reference of the d -axis RS voltage loop.

The design guidelines of the proposed method are presented in Fig. 16. It can be observed that the proposed method does not require either fault detection, R_f measurement, operation mode identification, or parameter tuning, and the method is very easy to implement.

B. Effective Range Calculation and Contribution Analysis

The effective range of the proposed method is shown in the green area of Fig. 7, and its effect on the continuous power supply is presented in Fig. 17.

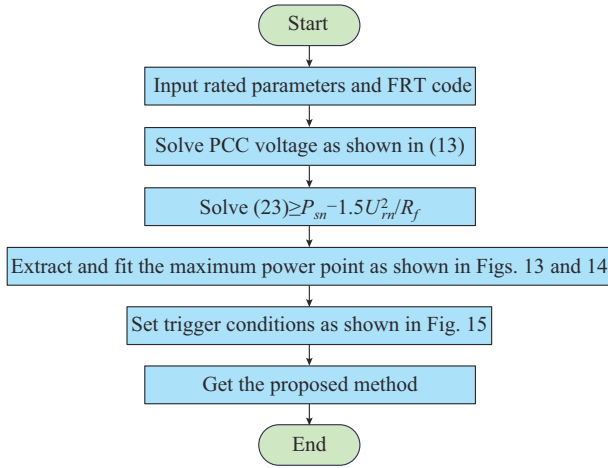


Fig. 16. Design guidelines of proposed method.

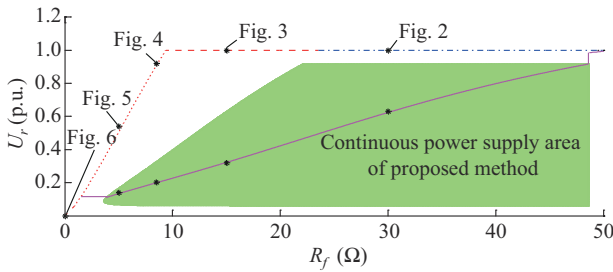


Fig. 17. Effect of proposed method on continuous power supply.

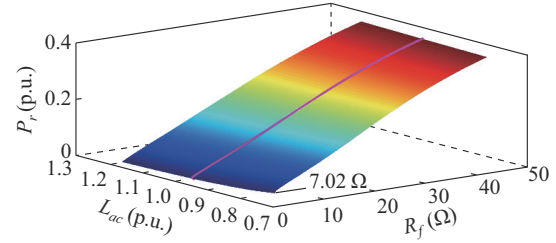
The dotted-dashed and dotted lines indicate the RS equilibrium points under rated AC voltage control, where the dotted-dashed line indicates the continuous power transmission area. The green area represents the continuous power transmission area of the proposed method, which is a projection of the surface shown in Fig. 12. The solid line in this green area is the optimized RS equilibrium curve, which is a projection of the maximum power transmission curve shown in Fig. 13.

As Fig. 17 shows, the RS continuous power transmission area can be significantly expanded by the proposed method. Combined with Figs. 3-6, the RS equilibrium points in the aforementioned four cases are all located in the power transmission interruption area of Fig. 17, which can be proven based on the reversed P_r from the respective simulation under fault. To achieve continuous power transmission during the fault, the aforementioned equilibrium points must be dropped to the green area, or most specifically to the solid line in this green area, to maintain the maximum power transmission under fault. It can be concluded that excessive PCC voltage amplitude is the main cause of RS voltage loop saturation and power transmission interruption and can be optimized by the proposed method.

C. Robustness Analysis

With the results in Figs. 9-11 calculated by (5), (13), and (23), L_{ac} is the most likely parameter to introduce a calculation error. Therefore, the robustness of the proposed method under L_{ac} variation is verified in Fig. 18, where the pink 3D

curve is equal to that shown in Fig. 13. Combined with the green area in Fig. 7, the effective area decreases from $R_f \geq 3.83 \Omega$ to only $R_f \geq 7.02 \Omega$ under 20% L_{ac} variation. Therefore, the proposed method is effective under severe measurement distortion.

Fig. 18. Proof of robustness under L_{ac} variation.

In addition, if the topology in Fig. 1 changes and an additional 0.25 p.u. RES is connected to the PCC, the original maximum power transmission curve as shown in Fig. 19 exhibits a small failure interval of $1.66 \Omega \leq R_f \leq 2.83 \Omega$, which can be easily compensated by updating the calculation data.

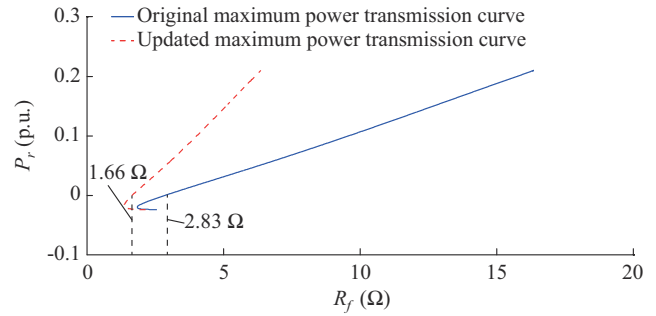


Fig. 19. Proof of robustness under a newly connected RES.

As the wind speed usually changes in practice, the proposed method should be tested under a steady-state low-power operation. The results are shown in Fig. 20, where P_{smax} is the RES maximum output active power. When the maximum output active power decreases from 0.75 p.u. to 0.3 p.u. due to the decrease in wind speed, the effective range of the proposed method remains unchanged, but the transmitted power reduces after 15.2Ω .

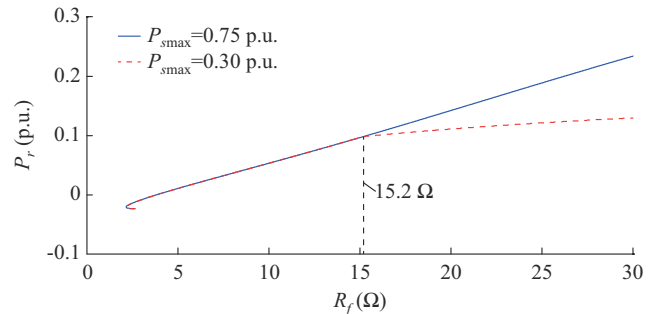


Fig. 20. Proof of robustness under a steady-state low-power operation.

Therefore, the proposed method is robust under inaccurate parameter measurements, unplanned RES expansion, and wide variations in wind speed.

VI. SIMULATION VERIFICATION

To prove the veracity of the analysis presented in Figs. 7, 8, 15, and 16, the proposed method shown in Fig. 14 is applied to all cases shown in Figs. 2-5. In addition, the performance of the proposed method under an asymmetric fault is also tested and analyzed. In each simulation case, the dotted and solid lines in the figures denote the results of rated AC voltage control (original method) and of the proposed method, respectively. The system as shown in Fig. 1 enters into steady state at 0.4 s, and an AC fault occurs at 0.6 s and is cleared at 1 s. In Figs. 21-27, i_{diff} is the MCC circulating current, u_{sm} is the voltage of submodule capacitors, and u_{dc} is the DC bus voltage.

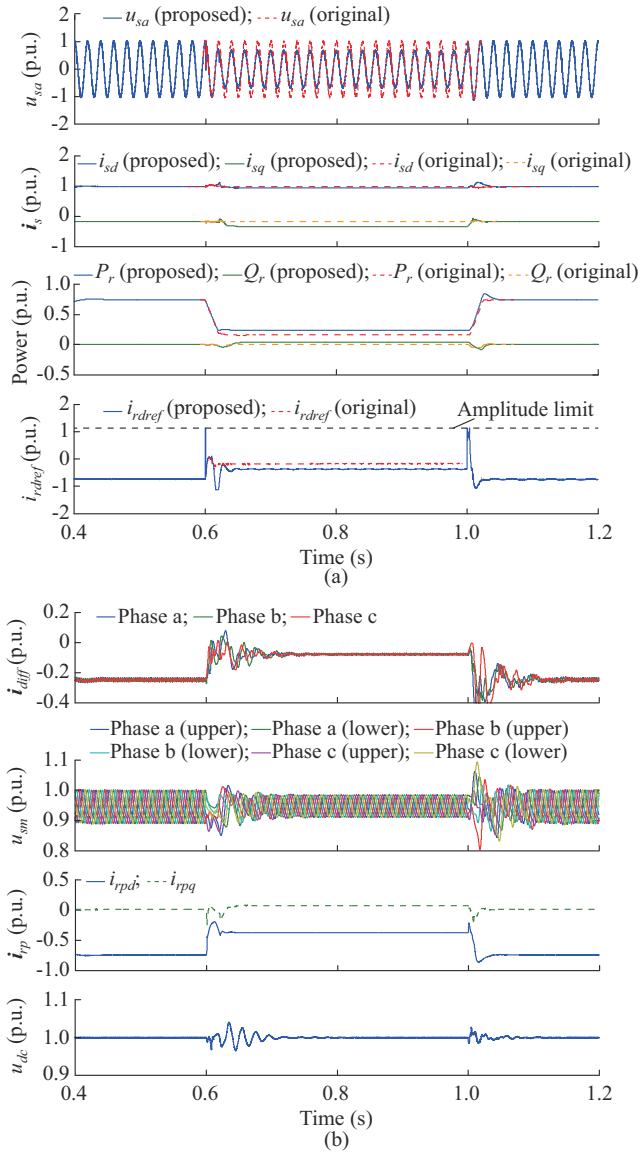


Fig. 21. Simulation comparisons when $R_f=30 \Omega$. (a) Fault response. (b) MMC internal states under proposed method.

A. Comparisons with Case Shown in Fig. 2

The dotted lines in Fig. 21(a) indicate the results that are equivalent to those shown in Fig. 2. Figure 21(a) shows that u_{sa} is reduced by the proposed method during an AC fault.

According to (13), U_r equals 0.63 p.u. in this case, which corresponds to the black point on the solid curve shown in Fig. 17. Here, i_{sq} increases in the reverse direction, which means that the proposed method drives the RES into LVRT mode. Under the proposed method, the transmitted power during the fault increases from 0.15 to 0.24 p.u., which is consistent with the solid line shown in Fig. 20. From Fig. 21(b), MMC internal states are stable under the duration of the fault, and the DC bus voltage can be maintained in the normal range. Thus, the DC grid has little effect on the AC bus.

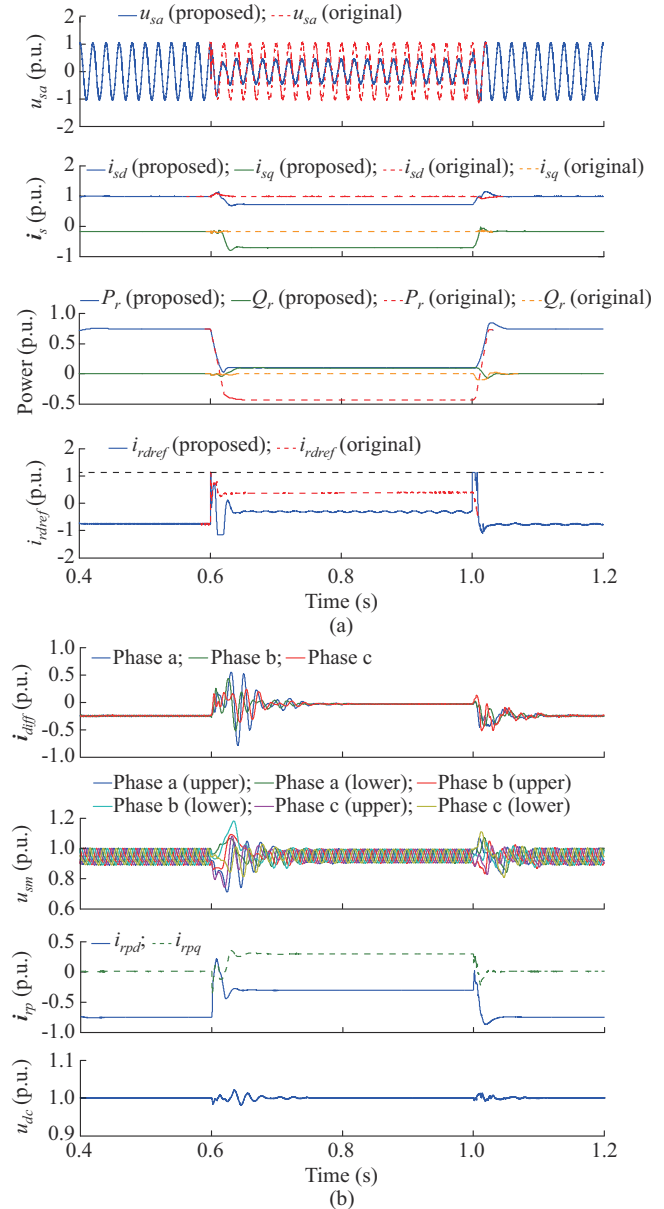


Fig. 22. Simulation comparisons when $R_f=15 \Omega$. (a) Fault response. (b) MMC internal states under proposed method.

B. Comparisons with Case Shown in Fig. 3

The dotted lines in Fig. 22(a) indicate the results that are equivalent to those shown in Fig. 3. According to Fig. 18(a) and (b), the amplitude of u_{sa} is lower than 0.9 p.u. and i_{sq} increases in reverse direction during the fault. Thus, the RES

operates in LVRT mode. According to (13), U_r is 0.33 p.u. in this case, which corresponds to the black point on the solid curve shown in Fig. 17. Under the proposed method, the obtained active power of the RS during the AC fault increases from -0.43 to 0.1 p.u., which is consistent with the curve shown in Fig. 14. The reversed i_{rdref} is suppressed by the proposed method to prevent the power from flowing into the fault point.

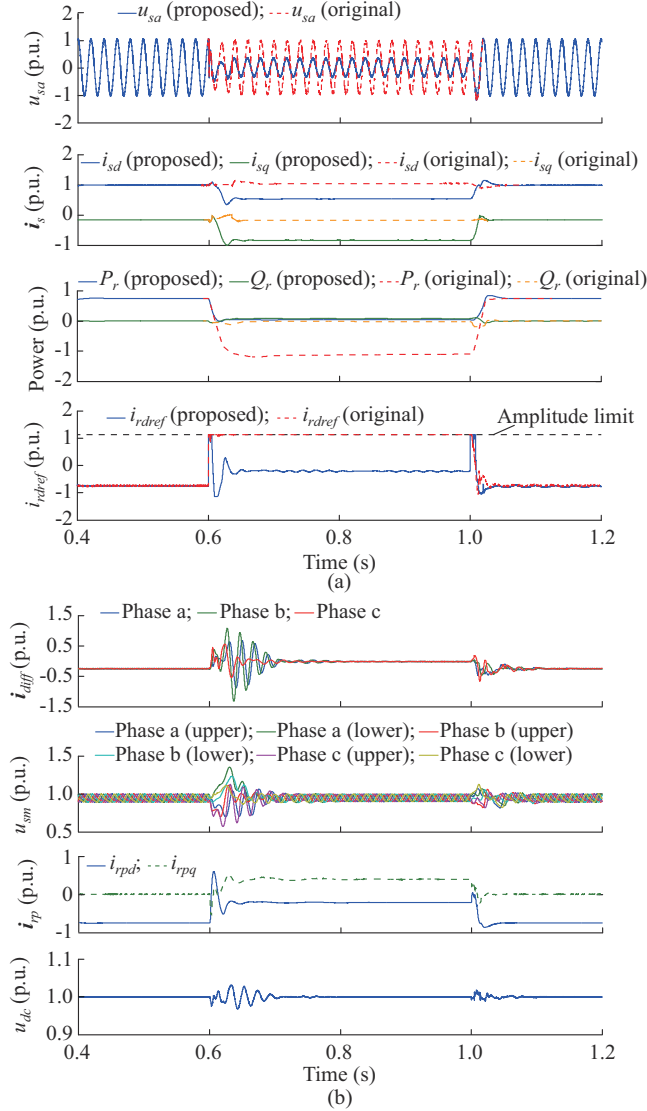


Fig. 23. Simulation comparisons when $R_f=8.5 \Omega$. (a) Fault response. (b) MMC internal states under proposed method.

C. Comparisons with Case Shown in Fig. 4

The dotted lines in Fig. 23(a) indicate the results that are equivalent to those shown in Fig. 4. As Fig. 23(a) shows, under the proposed method, the amplitude of u_{sa} is reduced during the fault and restored without overvoltage at fault clearance. According to (13), U_r equals 0.21 p.u. in this case, which corresponds to the black point on the solid curve shown in Fig. 17. Here, i_{sq} increases in a reverse direction during the fault, and thus the RES operates in LVRT mode. From the power waveforms, the proposed method can not only avoid RS power reversal but can also receive 0.042 p.u.

of active power during the fault, which is consistent with the solid line in Fig. 20. In addition, under the proposed method, the RS AC voltage loop is no longer saturated, and thus PCC voltage is controllable during the fault period. Combined with the analysis under (3), i_{rdref} is no longer greater than 0 at fault clearance after voltage loop desaturation. Thus, the steep rise in modulation amplitude stops, and PCC overvoltage is clearly suppressed by the proposed method.

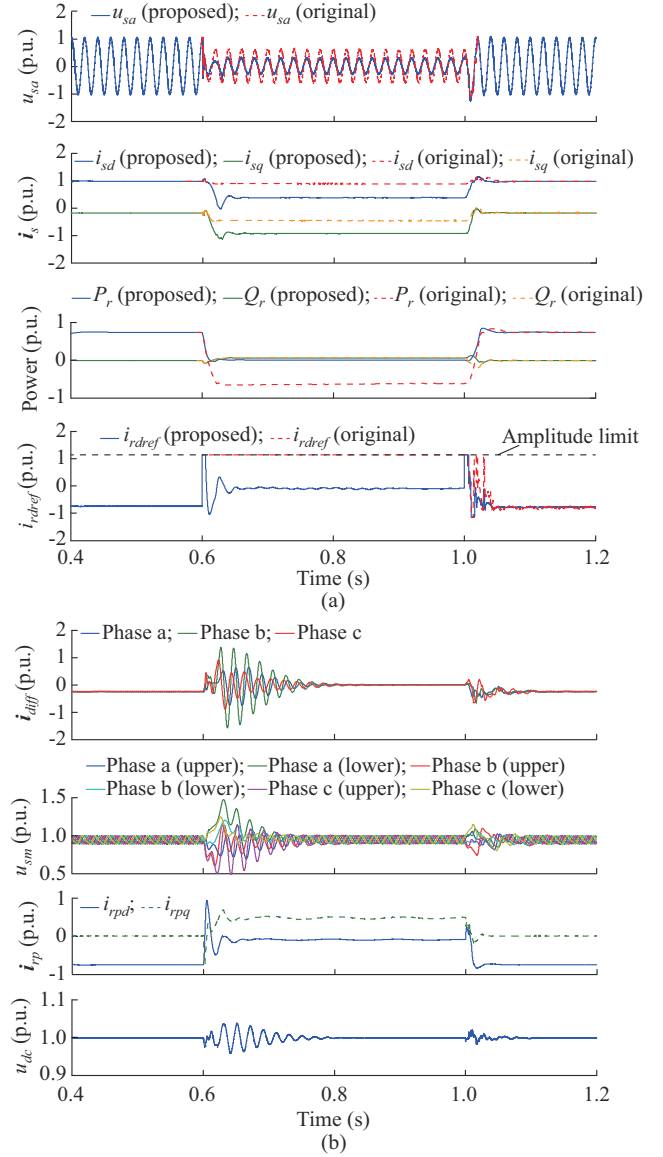


Fig. 24. Simulation comparisons when $R_f=5 \Omega$. (a) Fault response. (b) MMC internal states under proposed method.

D. Comparisons with Case Shown in Fig. 5

The dotted lines in Fig. 24(a) indicate results that are equivalent to those shown in Fig. 5. It can be observed that the amplitude of u_{sa} is further reduced and i_{sq} is further increased in the reverse direction under the proposed method, which can optimize the RES LVRT mode. According to (13), U_r equals 0.14 p.u. in this case, which is consistent with the data point on the solid curve shown in Fig. 17. The power reversal is optimized by the proposed method, and

the RS receives 0.013 p.u. of active power during the AC fault, which is consistent with the curve shown in Fig. 14. In addition, under the proposed method, the RS voltage loop is no longer saturated, and thus PCC voltage is controllable during the fault, and PCC overvoltage is obviously suppressed.

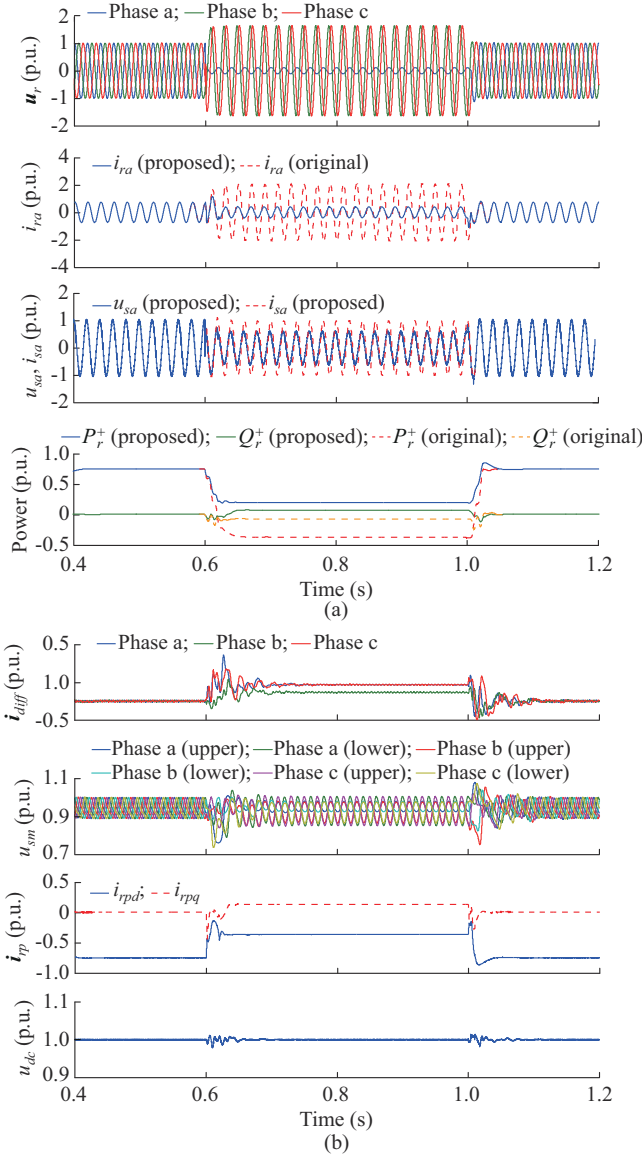


Fig. 25. Verification under a P-G fault ($R_f=1 \Omega$). (a) Fault response. (b) MMC internal states under proposed method.

E. Verification Under a P-G Fault

The proposed method was verified under a P-G fault, and the results are shown in Fig. 25. Since the RS adopts NS voltage suppression as shown in Fig. 1, NS voltage is suppressed but ZS voltage remains, and thus, PCC voltage is not sinusoidal. Under the proposed method, AC bus overcurrent is effectively suppressed and the transmitted power increases under the fault, thus showing that the proposed method is effective under a P-G fault. RES terminal voltage is sinusoidal because ZS voltage is blocked by the YD11 transformer. The terminal current is also sinusoidal due to NS negative current suppression. Figure 25(b) shows that circu-

lating current waveforms are stable but do not overlap, which is consistent with the results presented in [27].

F. Verification Under a Phase-to-phase-to-ground (2P-G) Fault

The proposed method was verified under a 2P-G fault, and the results are shown in Fig. 26. In this case, PCC PS voltage is equal to NS voltage [11], but PS voltage is controlled to be the rated value, whereas NS voltage is controlled to be 0 by the RS. Thus, a control conflict is initiated and RS modulation is saturated. When the proposed method is used, overcurrent is suppressed and modulation is desaturated, and thus RS control capability is restored. Reverse power flow is suppressed and continuous power transmission is maintained. The proposed method is effective under a 2P-G fault.

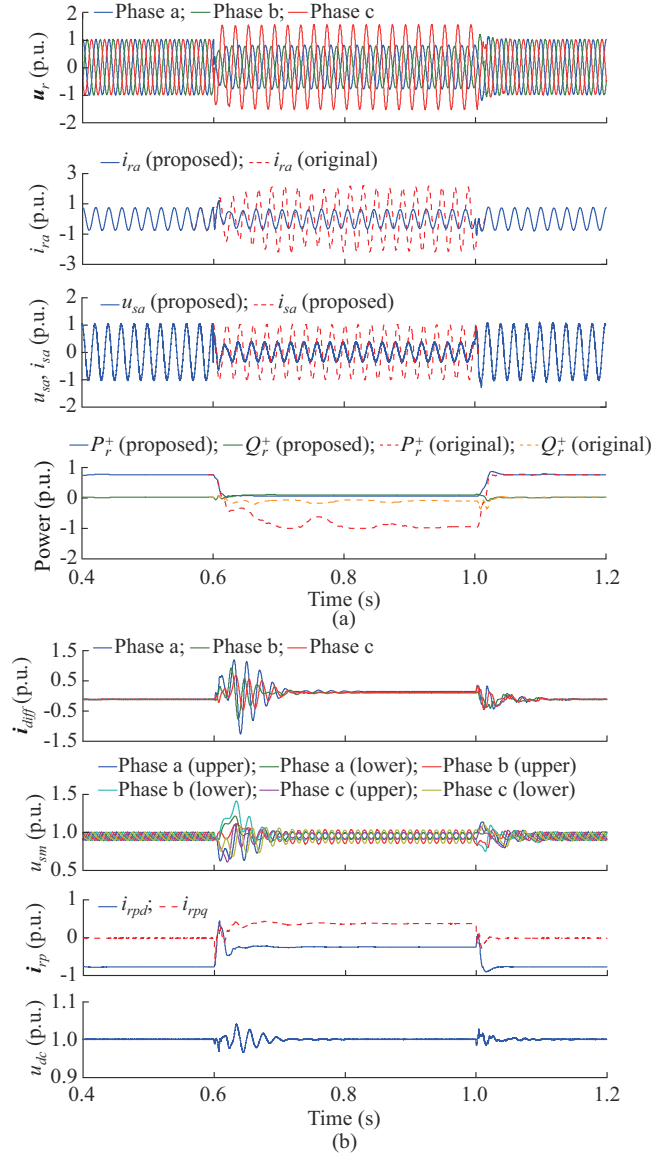


Fig. 26. Verification under a 2P-G fault ($R_f=5 \Omega$). (a) Fault response. (b) MMC internal states under proposed method.

Although the ZS voltage and current are 0, the responses of a phase-to-phase (P-P) fault are similar to those of a 2P-G fault [11]. Accordingly, the same analysis and results are

not repeated here.

G. Verification Under a Newly Connected RES

Under a newly connected RES, the topology in Fig. 1 changes and an additional 0.25 p.u. RES is connected to the PCC. Results are presented in Fig. 27, where subscript i indicates the i^{th} RES. Figure 27(a) and (b) shows that both RESs exhibit similar responses under the fault because they must fulfill the FRT grid code. Here, P_s is greater than 0 under the duration of the fault, which is consistent with Fig. 19. DC bus voltage can be controlled under a normal range. Thus, the AC fault is decoupled with a DC-side response, which can be simplified by an ideal voltage source under fault.

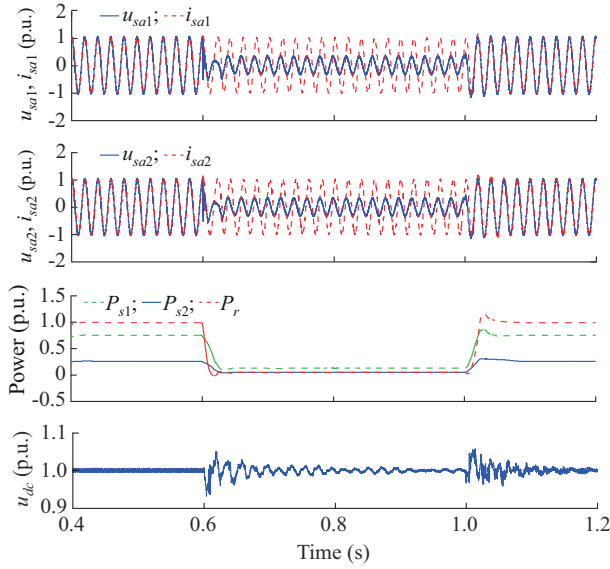


Fig. 27. Verification under a newly connected RES ($R_f = 5 \Omega$).

H. Comparisons with Existing Method

In this section, the latest version of the voltage-optimized FRT method [11] is introduced and compared with the proposed method. A control block is presented in Appendix A, where U_r^- and U_r^z are the NS and ZS amplitudes of \mathbf{u}_r , respectively.

As the NS and ZS values are 0 under a symmetric fault, the method presented in Appendix A shows the similar response as the rated voltage control and its current loop. Thus, the response of this method is equal to that shown in Figs. 2-6 under fault resistance variation, and the superiority of the proposed method is well demonstrated in Figs. 21-24.

Figure 28 presents the results of the method in [11] under a P-G fault when the RES adopts NS current suppression. Figure 28(a) shows that RES PLL output frequency f_{pll} is stable and RES terminal waveforms are sinusoidal under the fault. The d -axis NS RES voltage u_{sd}^- is not zero, but i_s^- maintains zero output because the RES adopts NS current suppression. As Fig. 28(b) shows, $P_r^+ = 0.25$ p.u., which is 5% greater than the result presented in Fig. 25(a). The d -axis NS current of RS i_{rd}^- reaches its limited value (0.25 p.u.), and thus the negative voltage loop presented in Fig. A6 is saturated and the d -axis NS voltage u_{rd}^- is not zero.

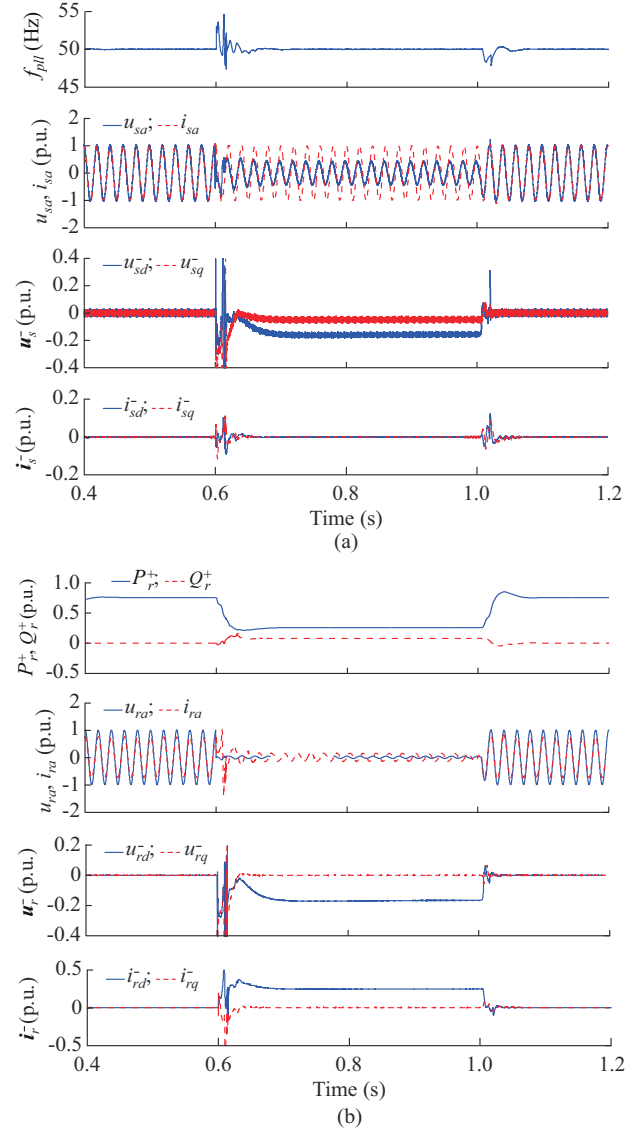


Fig. 28. Results of method in [11] under a P-G fault ($R_f = 1 \Omega$) when RES adopts NS current suppression. (a) RES response. (b) RS response.

When FRT grid code is used in the RES, (20) requires that the RES output an NS current according to its NS terminal voltage, which changes the fault point voltage and in turn generates RES voltage regulation and current redistribution, resulting in a fault response interaction. From (19) - (21), the NS RES current is maintained at 0 in all cases when the RS adopts NS voltage suppression. Thus, the interaction is blocked. However, both the RES and RS become NS current sources when the method in [11] is used, which exacerbates the fault interactions and results in divergence. This can be verified by Fig. 29, where the RES and RS adopt FRT code and the method in [11], respectively, under a P-G fault.

Thus, although the method in [11] can improve the power transmission by 5% when the RES adopts NS current suppression, it cannot achieve performance optimization under a symmetric fault; and in fact, it leads to divergence when the RES adopts FRT code under an asymmetric fault.

$$\begin{aligned}
 P_r &= \frac{A}{B} + 0.75 \frac{2.7a+b}{U_{sn} + 3a/U_{sn}} \sqrt{I_{sn}^2 \left[1 - 2.25 \times \left[0.9 - (1.35a + 0.5b)/(U_{sn}^2 + 3a) \right]^2 \right]} \\
 A &= 1.46 \times 10^{15} I_{sn}^2 U_{sn}^2 U_r^3 (0.18 + U_r^2) + a U_{sn} (-0.73 + 3U_r^2) - 3a^3/U_{sn}^3 - 4.1 \times 10^{-7} a/U_{sn} \sqrt{c} + U_{sn} (-1.18a^2/U_{sn}^2 - 4.1 \times 10^{-7} \sqrt{c}) \\
 B &= (U_{sn}^2 + 6a + 9a^2/U_{sn}^2) \sqrt{c I_{sn}^2 \left[U_{sn}^3 (-1.43 \times 10^{16} - 3.9 \times 10^{16} U_r^2) + a U_{sn} (9.22 \times 10^{15} - 1.17 \times 10^{17} U_r^2) + d \right] \left[U_{sn} (U_{sn} + 3a/U_{sn})^2 \right]} \\
 c &= U_{sn} (1.08 \times 10^{13} U_{sn}^3 U_r^2 + 3.25 \times 10^{13} a U_{sn} U_r^2 + 8.9 \times 10^{12} a^2/U_{sn} - 3.25 \times 10^{13} a^3/U_{sn}^3) \\
 d &= 1.17 \times 10^{17} a^3/U_{sn}^3 + 3.2 \times 10^{10} a/U_{sn} \sqrt{c} + U_{sn} (5.28 \times 10^{16} a^2/U_{sn}^2 + 2.13 \times 10^{10} \sqrt{c})
 \end{aligned} \tag{A2}$$

D. Control Block of Method in [11]

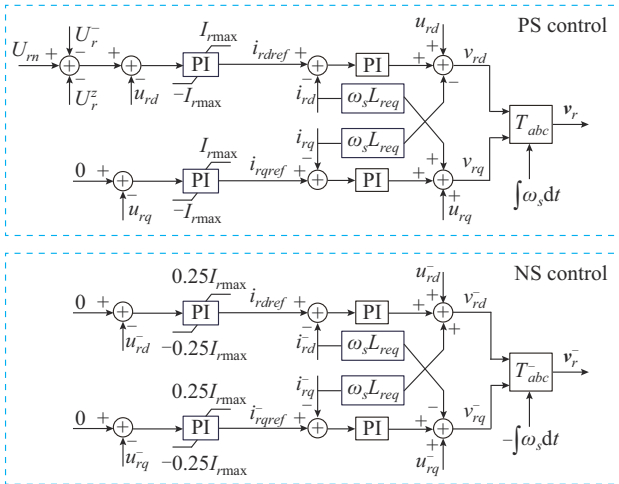


Fig. A6. Control block of method in [11].

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