Application of MMC with Embedded Energy Storage for Overvoltage Suppression and Fault Ride-through Improvement in Series LCC-MMC Hybrid HVDC System

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***Abstract*—The series line-commutated converter (LCC) and modular multilevel converter (MMC) hybrid high-voltage direct current (HVDC) system provides a more economical and flexible alternative for ultra-HVDC (UHVDC) transmission, which is the so-called Baihetan-Jiangsu HVDC (BJ-HVDC) project of China. In one LCC and two MMCs (1+2) operation mode, the sub-module (SM) capacitors suffer the most rigorous overvoltage induced by three-phase-to-ground fault at grid-side MMC and valve-side single-phase-to-ground fault in internal MMC. In order to suppress such huge overvoltage, this paper demonstrates a novel alternative by employing the MMC-based embedded battery energy storage system (MMC-BESS). Firstly, the inducements of SM overvoltage are analyzed. Then, coordinated with MMC-BESS, new fault ride-through (FRT) strategies are proposed to suppress the overvoltage and improve the FRT capability. Finally, several simulation scenarios are carried out on PSCAD/EMTDC. The overvoltage suppression is verified against auxiliary device used in the BJ-HVDC project in a monopolar BJ-HVDC system. Further, the proposed FRT strategies are validated in the southern Jiangsu power grid of China based on the planning data in the summer of 2025. Simulation results show that the MMC-BESS and proposed FRT strategies could effectively suppress the overvoltage and improve the FRT capability.**

***Index Terms*—Line-commutated converter (LCC), modular multilevel converter (MMC), MMC-based embedded battery energy storage system (MMC-BESS), fault ride-through (FRT) capability, overvoltage suppression.**

I. Introduction

To fulfill the ever-growing energy demand, high-voltage direct current (HVDC) transmission technology has played an essential role in long-distance and bulk-capacity power transmission occasions [1], [2]. Now, two types of converters are mainly adopted for HVDC projects: line-commutated converter (LCC) and modular multilevel converter (MMC) [1].

LCC-based HVDC (LCC-HVDC) has been applied in most of practical HVDC projects, due to its high-technology maturity, low-investment cost, and sufficient practical experience. However, the LCC-HVDC introduces some inherent drawbacks such as excessive consumption of reactive power and the incapability to connect weak AC systems. Besides, with the wide application of LCC-HVDC, multi-infeed HVDC frame has been gradually formed in the China East and Guangdong power grid, leading to several serious problems [3], [4]. As an alternative, MMC-based HVDC (MMC-HVDC) has many attractive features such as no commutation failure (CF) and potentially smaller footprint. However, compared with LCC-HVDC, the MMC-HVDC has several obstacles such as smaller power rating, higher installation cost, and higher loss [5].

In order to make full use of the superiorities of both LCC and MMC, the hybrid HVDC technology has been paid increasing attention to the future power transmission [6], [7]. The varieties of novel schemes for hybrid HVDC systems have been proposed by global scholars [8] - [12]. Among these schemes, a series LCC-MMC hybrid HVDC project called Baihetan-Jiangsu HVDC (BJ-HVDC) project is under construction. As shown in Fig. 1, the rectifier consists of two 12-pulse LCCs, and one 12-pulse LCC in series with three paralleled MMCs adopted at the inverter.

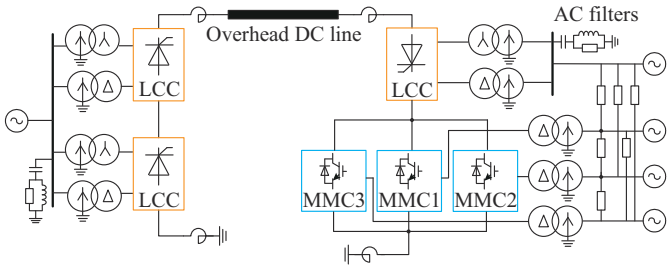

Fig. 1. Basic topology of BJ-HVDC.

It should be noted that, the four AC systems at the inverter are accessed with varying degrees of electrical coupling, rather than the ideal dispersion. The AC grid-side fault, which may occur at any inverter-side converter, will occur in

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the decrease of all AC voltages in varying degrees simultaneously. Then, the inverter LCCs may suffer the CF, and the MMC power delivery is also impeded. The rectifier LCCs are disenable to respond rapidly due to the time delay, e.g., communication delay and trigger delay, resulting in vast power surplus at the inverter. Consequently, the sub-modules (SMs) in MMCs are compelled to overcharge, and eventually, the SM capacitor voltages may exceed these safety thresholds. Besides, the valve-side single-phase-to-ground (VSPG) fault in internal MMCs also forces severe upper-arm SM overvoltage [13], [14]. Though the occurrence probability of VSPG faults is arguably low, their serious aftermaths should be considered. According to the simulations and research works conducted by the research institutes of State Grid Corporation of China (SGCC), under one LCC and two MMCs (1+2 mode) operation mode, the grid-side three-phase-to-ground (GTPG) fault at grid-side MMC and the VSPG fault in internal MMC are the most serious [15], [16]. In this case, the electrical coupling of the remaining three AC systems at the inverter is closest to each other, and the SM capacitors suffer the most rigorous overvoltage. Such huge overvoltage will threaten the insulation of the SM devices, and even damage the equipment, leading to inestimable loss.

Although some additional fault ride-through (FRT) controls have been proposed to mitigate the SM overvoltage [17]-[20], such huge overvoltage is beyond restraint only depending on those controls. Thus, the auxiliary energy consumption devices are necessary, which are mainly DC choppers (DCCs) [21]-[23]. Similar to the DCC, the research institutes of SGCC have developed a controllable and adaptive energy consumption (CAEC) device based on the controllable metal oxide arrester (MOA), which is installed in parallel at the MMC DC port, i.e., ±400 kV DC bus [15]. Although the CAEC has low cost and low change rate of voltage and current compared with other DCCs, the large energy absorption with long period will accelerate the MOA aging. Additionally, the overvoltage suppression shows unsatisfactory effect under the VSPG faults, and the CAEC introduces the risk of trigger failure, eventually reducing the security and reliability of the BJ-HVDC system.

Currently, an emerging topic on MMC-based embedded battery energy storage system (MMC-BESS) attracts the interest of both the academic and industrial worlds [24]-[26]. Here, the BESS is interfaced to the SM capacitor using a bidirectional DC-DC converter. Serving as an AC-DC conversion with additional energy storage capability, the MMC-BESS could not only absorb the surplus power, but also provide fast power support. Therefore, we demonstrate a novel alternative for SM overvoltage suppression by adopting the MMC-BESS. Further, the MMC-BESS could improve the FRT capability under AC and DC line faults. Even if the practical application of MMC-BESS may be astricted due to some intractable problems such as intensive cost and excessive footprint. In the context of the goals of carbon emission peak and carbon neutrality, with the continuous development of energy storage technology, it is believed that the MMC-BESS will show incremental potential and demand in the modern power system for the system stability and the power supply reliability, particularly in the areas of enormous load demands and high-penetration renewables.

The main contributions are summarized as follows.

1) The mechanisms of the SM overvoltage induced by the VSPG and GTPG faults are thoroughly analyzed.

2) Coordinated with the MMC-BESS, new FRT strategies are proposed to suppress SM overvoltage and improve the FRT capability under different faults.

3) The overvoltage suppression of the MMC-BESS is verified against the CAEC in the monopolar BJ-HVDC system on PSCAD/EMTDC, as shown in Fig. 1.

4) The proposed FRT strategies are validated by applying the rectifier-side severe AC fault in the southern Jiangsu power grid of China, where the power grid is benchmarked based on the planning data in the summer of 2025 on PSCAD/EMTDC.

The rest of this paper is organized as follows. Section II describes the structure and control of the BJ-HVDC. The inducements of the SM overvoltage are analyzed in Section III. In Section IV, the overview of MMC-BESS is presented. Coordinated with the MMC-BESS, new FRT strategies are proposed in Section V. In Section VI, the simulation verifications are carried out on PSCAD/EMTDC. Section VII dawns the conclusion.

II. Structure and Control of BJ-HVDC

A. Structure

The basic topology of the BJ-HVDC is shown in Fig. 1. Here, the rectifier consists of two series 12-pulse LCCs to bear the ±800 kV DC voltage. For the inverter, a 12-pulse LCC at the upper valve is in series with lower-valve MMCs to share the total ±800 kV DC voltage. The three identical half-bridge SMs (HBSMs) based MMCs are connected in parallel to match the LCC capacity. The equivalent impedances among the four AC systems are listed in [19].

In normal operation mode, the inverter LCC transmits half of the total transmission capacity, and the three MMCs equally share the remaining half, which is the so-called 1+3 mode. When any MMC exits due to the maintenance or failure, the residual two MMCs will deliver half of the capacity, i.e., 1+2 mode. In this mode, the BJ-HVDC maintains full-power operation, and the MMC reaches its rated capacity. One LCC and only one MMC on the inverter side (1+1 mode) are not permitted to operate for a long time, since the MMC will suffer severe overcurrent and overvoltage under the inverter-side AC faults. Thus, only the inverter LCC continues operating in half DC voltage mode, improving the reliability and delivery capacity.

B. Control

The control has been discussed minutely in [12], and will not be repeated here in full depth. The rectifier LCCs adopt constant DC current (CC) control and minimum firing angle (MFA) (5°) control. The inverter LCC adopts constant DC voltage (CV) control as the main control, while the backup extinction angle (BEA) control and the backup DC current (BCC) control are also utilized as auxiliary controls.

The vector current control is adopted for all MMCs.

MMC1 adopts CV control, while both MMC2 and MMC3 adopt constant active power control. In addition, all three MMCs adopt constant reactive power control.

III. Inducements of SM Overvoltage

Due to the diverse electrical coupling among the inverter AC systems, the severity of the faults induced by different fault locations is also variational. In other words, the inverter-side AC faults are complicated and troublesome. Thus, this section only analyzes the two most severe faults: VSPG fault in internal MMC and GTPG fault at grid-side MMC. Analyses and conclusions are only carried out for the positive pole but are equivalently applicable to the negative pole.

A. VSPG Fault in Internal MMC

The classical MMC consists of six arms, and each arm is composed of N HBSMs and an inductor L in series. The arm resistance is equivalent to a resistor R. The transformer is configured with a star/delta (Y/△) connection, and its grid side is arranged with a neutral grounding.

The VSPG fault in internal MMC is usually induced by the insulation failure and flashover of wall bushings, thus, it is normally a permanent fault. For a VSPG fault in internal MMC closes to the valve, the arm currents will immediately increase to intolerable levels. To protect the converter, the insulated gate bipolar transistors (IGBTs) will be rapidly blocked by their internal overcurrent protection. The grid-side AC circuit breakers (ACCBs) will also be tripped after several cycles [13]. Assume that a VSPG fault occurs in phase a of MMC1 at time t_0, once the IGBTs are blocked, the converter becomes an uncontrollable diode bridge, as illustrated in Fig. 2. Here, U_{dcM} and I_{dcM} are the DC voltage and DC current, respectively; u_{vj} and u'_{vj} are the valve-side pre- and post-fault voltages in phase j (j = a, b, c), respectively; C_{equ} is the equivalent capacitor of all SMs on each arm; i_{rj} is the arm current, and the subscript r (r = p, n) denotes the upper and lower arms; and D denotes the diode.

It should be emphasized that, due to the symmetry of three phases, the analysis presented for a fault in phase a would also apply to the other two phases.

The VSPG fault creates a new zero voltage potential in the faulty phase a. Due to the △ connection, the magnitudes of the line voltages remain unchanged, and the other two non-fault phase voltages rise to the line voltages. Due to their forward-bias, diodes D_1, D_3, and D_5 will be reverse-biased once the IGBTs are blocked. Moreover, before blocking the converter, the sum of the total voltage of all SM capacitors $U_{rj,\mathrm{sum}}$, e. g., $U_{\mathrm{pc,sum}}$, on each arm is approximately equal to U_{dcM}, which is higher compared with the valve-side line voltages. Upon the converter is blocked, diodes D'_2, D'_4, and D'_6 will also be reverse-biased, and the voltages of all SM capacitors in the lower arms will remain constant. For the faulty phase a, because of the arm inductor L, D_4 will be reverse-biased until the current i_{na} decays to zero. Conversely, due to the free-wheeling effect of diodes and L, D_6 and D_2 will conduct during every negative half-cycle of u'_{vb} and u'_{vc}, respectively.

1) Negative Half-cycles of Valve-side AC Voltage

For the faulty phase a, the upper-arm SM capacitors will only be charged by the transient overvoltage of DC terminal and the energy stored in L. For non-fault phases, taking phase c as an example, the upper-arm SM capacitors will be charged as shown in Fig. 3:

$$U_{\mathrm{pc,sum}} < U_{\mathrm{dcM}} - u'_{\mathrm{vc}} \tag{1}$$

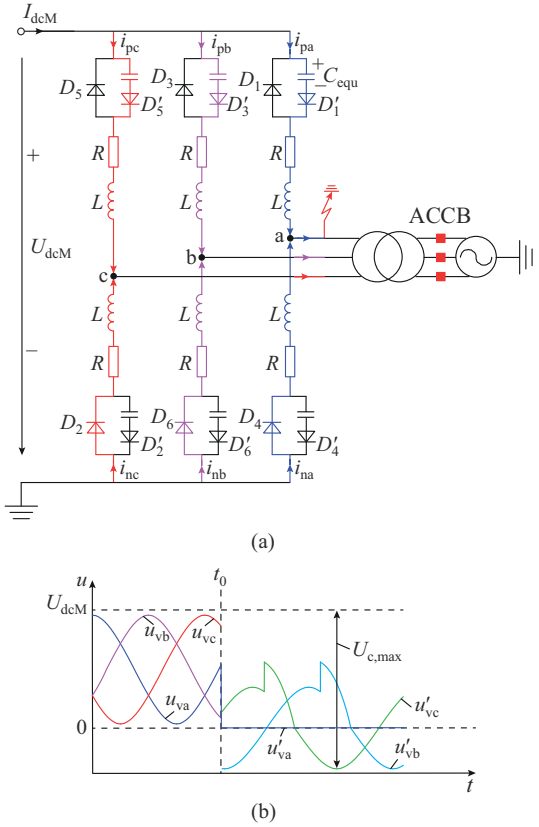

Fig. 2. VSPG fault. (a) Equivalent circuits of blocked MMC1. (b) Valve-side voltage waveform.

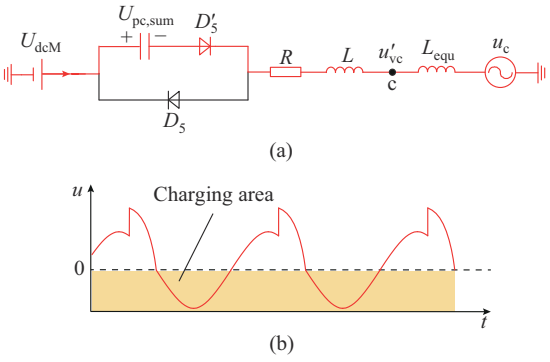

Fig. 3. Post-fault characteristics on upper arm in phase c. (a) Post-fault equivalent circuit on upper arm in phase c. (b) Post-fault valve-side voltage waveform in phase c.

In other words, (1) will be fulfilled only during negative half cycles of u'_{vc}, and the capacitors will stop being charged once $U_{\mathrm{pc,sum}}$ reaches the maximum value $U_{\mathrm{c,max}}$, given by [14]:

$$U_{\mathrm{c,max}} = U_{\mathrm{dcM}} + \max(u'_{\mathrm{vc}}) \tag{2}$$

where $\max(u'_{\mathrm{vc}})$ is the peak value of u'_{vc}. Neglecting the arm

resistor R, $\max(u'_{vc})$ could be approximated as:

$$\max(u'_{vc}) = \frac{L}{L+L_{equ}} \sqrt{3} \times \sqrt{2}\, u_c \tag{3}$$

where u_c is the pre-fault phase voltage of the transformer on the valve side; and L_{equ} is the equivalent reactance of transformer at the valve side. The HBSM-MMC voltage modulation index m is defined as:

$$m = \frac{2\sqrt{2}\, u_c}{U_{dcM}} \tag{4}$$

Assuming U_{dcM} remains constant under the fault, substitute (3) and (4) into (2), then (2) is rewritten as:

$$U_{c,max} = \left(1 + \frac{\sqrt{3}}{2} \frac{mL}{L+L_{equ}}\right) U_{dcM} \tag{5}$$

Supposing that $L_{equ} = 0.5L$ and $m = 0.9$, the maximum upper arm SM capacitor voltage will be $1.52U_{dcM}$ approximately. Considering a 10% ripple during the operation, this value may increase to $1.62U_{dcM}$. Such an overvoltage could damage the SMs, as the SMs are normally designed to withstand a 1.5 p.u. voltage [15].

2) DC Power Transmitted by Rectifier LCCs

The above analysis ignores the impact of DC power sent by the rectifier LCCs. As the VSPG fault is normally permanent, the rectifier LCCs need to be forced retard, and MMC2 has to be blocked. Then, the BJ-HVDC system should be shut down for repairing and maintenance. Whereas, the rectifier LCCs are disenable to respond rapidly due to the time delay, which will affect the voltages of upper-arm SM capacitors.

Assuming that the rectifier LCCs take Δt_D to be forced retard, the voltage increment ΔU_{dc} of the upper-arm SM capacitors could be calculated as:

$$(P_{dc} - P_{ac,IL} - P_{ac,M2})\Delta t_D = \frac{3}{2} C_{equ} (U_{dcM} + \Delta U_{dcM})^2 - \frac{3}{2} C_{equ} U_{dcM}^2 \tag{6}$$

where P_{dc} is the DC power transmitted by the rectifier LCCs; and $P_{ac,IL}$ and $P_{ac,M2}$ are the active power outputs of the inverter LCC and MMC2, respectively. Due to the slight variation of both DC and AC voltages, P_{dc}, $P_{ac,IL}$, and $P_{ac,M2}$ can be kept near the reference values.

As $\Delta U_{dc} \ll U_{dcM}$, (6) is simplified and rewritten as:

$$\Delta U_{dcM} = \frac{P_{dc} \Delta t}{3 C_{equ} U_{dcM}} \tag{7}$$

It could be observed from (7) that, the larger P_{dc} and the longer Δt_D are, the more serious the overvoltage of the upper-arm SM capacitors will be.

B. GTPG Fault at Grid-side MMC

Referred as in [19], in an LCC, MMC1, and MMC2 mode ($1+2_{12}$ mode), the GTPG fault occurring at the grid-side MMC1 will cause the most severe overvoltage.

In normal $1+2_{12}$ mode, both MMC1 and MMC2 reach their rated capacity, and the theory has no extra capability to absorb the excess power. Once a metal GTPG fault occurs at the grid-side MMC1, extensive power will be accumulated at the inverter, inducing unbearable overvoltage.

Based on the instantaneous power theory, the active power delivery of MMC is calculated as:

$$P_{ac,Mi} = 1.5 u_{gd,Mi} i_{vd,Mi} \tag{8}$$

where $P_{ac,Mi}$ is the active power output of the i^{th} ($i = 1, 2, 3$) MMC; $u_{gd,Mi}$ is the d-axis grid-side voltage component; and $i_{vd,Mi}$ is the d-axis valve-side current component. When a GTPG fault occurs, as shown in Fig. 4, the AC voltage of MMC1 will drop to zero, i.e., $u_{gd,M1} = 0$. The power delivery of MMC1 is absolutely obstructed, i.e., $P_{ac,M1} = 0$. Due to the electrical coupling among AC systems, the AC voltage of MMC2 reduces. With the current limiter, the current $i_{vd,M2}$ cannot rise infinitely. Thus, the power output of MMC2 is restricted. Worse still, the inverter LCC suffers the CF, i.e., $P_{ac,IL} = 0$.

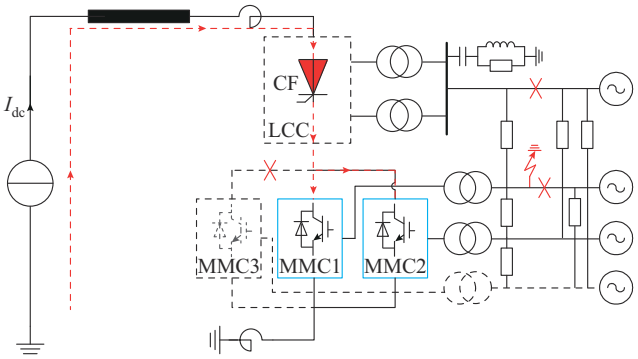

Fig. 4. GTPG fault occurring at grid-side MMC1.

In other words, the huge DC power conveyed by the rectifier LCCs is only partially dissipated through the MMC2, resulting in vast power surplus at the inverter. Consequently, the SMs of both MMC1 and MMC2 are compelled to overcharge, and the overvoltage of SM capacitor $u_{jkx,Mi}(\Delta t_F)$ is derived as:

$$\int_0^{\Delta t_F} (P'_{dc} - P'_{ac,M2})\mathrm{d}t = \frac{1}{2} C_0 \sum_{i=1}^{2} \sum_{j=a,b,c} \sum_{k=p,n} \sum_{x=1}^{N} (u^2_{jkx,Mi}(\Delta t_F) - u^2_{jkx,Mi}(0)) \tag{9}$$

where Δt_F is the duration of the GTPG fault; $u_{jkx,Mi}(0)$ is the pre-fault voltage for SM capacitor; C_0 is the SM capacitor; P'_{dc} is the DC power that the rectifier LCCs transmit to the inverter side during the GTPG fault; and $P'_{ac,M2}$ is the active power that MMC2 transmits to AC system during the GTPG fault.

In conclusion, the SM capacitors will suffer an intolerant overvoltage level induced by the VSPG and GTPG faults. The auxiliary energy consumption device is necessary to reliably relieve the overvoltage problem.

IV. Overview of MMC-BESS

A. Topology

In contrast to asymmetrical distribution [27], the BESS in this paper is evenly allocated in all SMs in order to minimize the size of the BESS. The topology of MMC-BESS is similar to that of traditional MMC, except for SMs. As shown in Fig. 5, each SM consists of a classical HBSM and

a battery bank which is interfaced to the SM capacitor via a bi-directional DC-DC converter. Here, u_C is the SM capacitor voltage; T_1-T_4 are the firing signals of IGBTs; L_{es} is the DC-DC converter inductor; and i_{es} and u_{es} are the current and voltage of the battery bank, respectively.

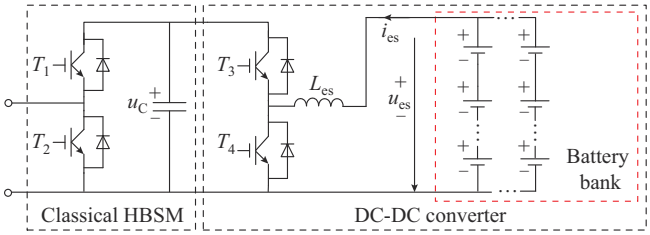

Fig. 5. Structure of HBSM with battery energy storage.

B. Operation Principle

The DC-DC converter operates as a buck converter to charge the battery, or a boost converter to discharge the battery. Figure 6(a) defines the active power flow, which is expressed as:

$$P_{es} = P_{dc} - P_{ac} \tag{10}$$

where P_{es} is the active power output of the BESS; and P_{ac} is the active power output of the MMC-BESS. While all three power flows can be bidirectional, only the positive flows of P_{dc} and P_{ac} are considered due to limited space.

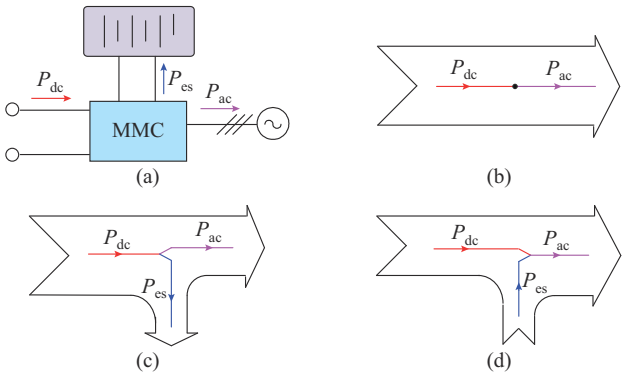

Fig. 6. Operation modes of MMC-BESS and corresponding power flow. (a) Power flow definition. (b) Idle. (c) Charging. (d) Discharging.

Under steady-state operation, the BESS does not work, and the MMC-BESS just works similar to the traditional MMC in Fig. 6(b). As shown in Fig. 6(c) and (d), when the power is in surplus or shortage, the BESS will charge or discharge to meet the active power balance.

C. BESS Requirement

The primary objective of BESS is to suppress overvoltage, and the 1+2 mode is infrequent. Thereby, the rated output power of BESS is designed to be equal to that of MMC in 1+3 mode for size reduction. This will be evidenced later in Section VI.

D. Control

The controller of the MMC-BESS is primarily divided into two parts: the main controller and the BESS controller.

1) Main Controller

The structure of main control is shown in Fig. 7, where the superscript * denotes the reference value; the subscripts d and q are the d- and q- axis components, respectively; Q_s is the reactive power; u^*_{diffj} and u^*_{cirj} are the differential-mode and common-mode voltages in phase j, respectively; and U_{Cav} is the average voltage of SM capacitors [28].

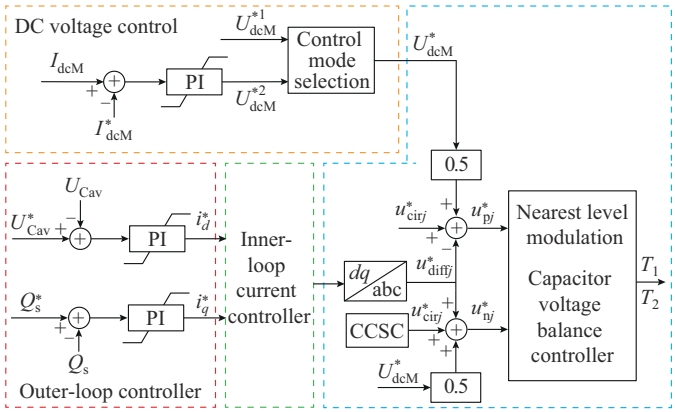

Fig. 7. Structure of main controller.

Different from the traditional MMC control in which DC voltage reference is usually set as the rated DC voltage, U^*_{dcM} relies on the control mode of the MMC-BESS. For the power-control MMC-BESS, U^*_{dcM} is generated by the DC current PI controller, while it is directly set as the upper command value for the DC voltage control converter. Cooperated with BESS, constant average capacitor voltage (ACV) control is employed to regulate the voltage of SM capacitor near the nominal voltage, or to promote it to recover quickly to the pre-fault value under faults. In addition, the SM capacitor may be inserted into or bypassed from the arm using T_1 and T_2.

2) BESS Controller

The BESS controller controls DC-DC converter of each SM independently. As depicted in Fig. 8, the reference of current controller is calculated by the outer controller which will be described in the following section. Through the pulse width modulation (PWM), T_3 and T_4 are generated to adjust the charging/discharging current of BESS, and further manage P_{es}.

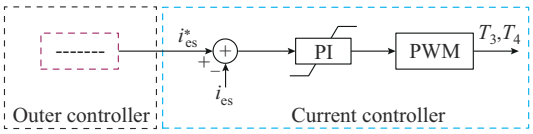

Fig. 8. Structure of BESS controller.

V. Proposed FRT Strategies

Coordinated with the MMC-BESS, new FRT strategies are proposed in this section to achieve controllable power support or dissipation in different fault scenarios.

Under steady-state operation, the SM capacitor voltages are only adjusted by the main controller, and the BESS is dormant. When the system suffers a fault, the BESS will be activated.

A. Overvoltage Suppression

1) VSPG Fault in Internal MMC

Since the VSPG fault is a normally permanent fault, upon the fault is detected (about 1.0 ms) and the faulty MMC is blocked. After several times of delay, force retard (FR) is applied by magnifying the firing angle α_R of the rectifier LCCs to a relatively large angle such as 120°. Since only the upper-arm SM capacitors undergo the severe overvoltage, once the maximum voltage of the SM capacitors on any upper arm exceeds the protection threshold $\underline{U}_{lim}$, the corresponding upper-arm BESSs will be immediately activated, although all lower-arm BESSs remain dormant. When the DC currents of other sturdy MMCs decline close to zero, the healthy MMCs will also be blocked. After several cycles (typically 60-100 ms), the ACCBs are triggered, and then the entire BJ-HVDC system or at least faulty pole is shut down. Summarily, the controls of the upper-arm BESS in faulty MMC and rectifier LCCs are drawn, as shown in Fig. 9, where FD is the fault detection signal; and I_{dcR} is the DC current of the rectifier LCCs. As the fault is permanent, the SM capacitor voltages could be restrained near the protection threshold, i. e., $u_c^{*1}=U_{lim}$ (1.3 p.u.) [15].

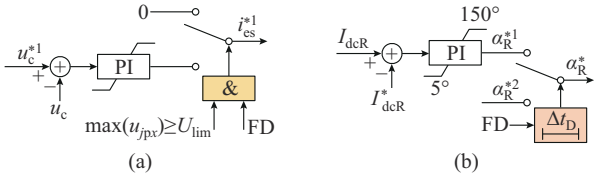

Fig. 9. Controls of upper-arm BESS in faulty MMC and rectifier LCCs. (a) Outer controller of upper-arm BESS in faulty MMC. (b) Controller of rectifier LCCs.

2) GTPG Fault at Grid-side MMC

Due to the saturated transmission capacity in 1+2 mode, the remaining two MMCs will stomach the severe overvoltage when a terrible GTPG fault occurs at any grid-side MMC. In order to shorten the energy absorption of BESS, the DC power transmitted by rectifier LCCs needs to be reduced by minishing the current reference I_{dcR}^*. All BESSs of both MMCs will rouse when the fault is detected and the maximum voltage of the SM capacitors exceeds the protection threshold.

In 1+2 mode, the FRT strategy for the GTPG fault at grid-side MMC is illustrated in Fig.10. To achieve fast fault recovery, the voltage reference of the SM capacitor can be set as the rated value. Besides, to avoid the current cut-off, the current reference I_{dcR}^{*2} should not be assigned too small.

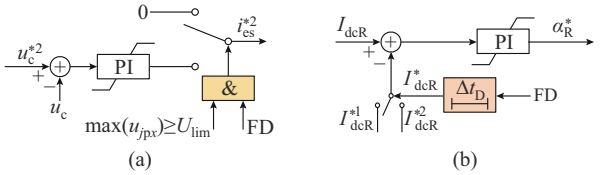

Fig. 10. FRT strategy for GTPG fault at grid-side MMC in 1+2 mode. (a) Outer controller of BESS. (b) Controller of rectifier LCCs.

If the fault occurs at the inverter LCC, the excess power can be absorbed almost alone by the BESSs without reducing the reference I_{dcR}^*. Similarly, in 1+3 mode, depending on about 33% spare delivery capacity of the MMCs, the excess power caused by the fault occuring at any converter could be evacuated by the MMCs and BESSs. Thus, in these cases, only the control in Fig. 10(a) is activated.

B. Power Support

1) AC Fault at Rectifier

When the sending-end AC bus suffers a fault, the DC power P_{dc} is restrained, and the receiving-end AC system sustains a shortage of active power. For the serious sending-end AC fault that the DC voltage at the rectifier LCCs U_{dcR} drops to below U_{dcM}, the DC current I_{dc} will drop to zero rapidly, and P_{dc} will also decrease to zero. Then, this huge deficiency of active power will cause fluctuations on the receiving-end AC system.

To compensate the lack of power, all BESSs of the MMCs are roused to support the power. The outer controller of the BESS under the AC fault at rectifier is shown in Fig. 11, where I_{dcI} is the DC current at the inverter DC bus.

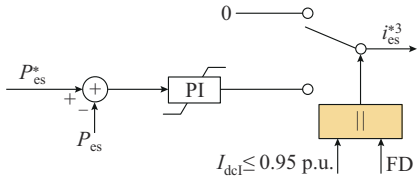

Fig. 11. Outer controller of BESS under AC fault at rectifier.

When the fault is detected, or the current I_{dcI} drops to below 0.95 p.u., the BESS will quickly switch into power output mode. The power reference P_{es}^* relies on the real-time power shortage, which could ensure relatively accurate power compensation. The reference $P_{es,Mi}^*$ is calculated as:

$$P_{es,Mi}^* = \frac{P_{dcN,Mi} - P_{ac,Mi}}{6N} \tag{11}$$

where $P_{dcN,Mi}$ is the rated or steady-state active power of the i^{th} MMC. It is worth noting that P_{es}^* cannot exceed its rated value.

Besides, the current references I_{dcM}^* of the power-control MMC-BESSs are varied with I_{dcI} to escape the uneven flowage of the MMC DC current $I_{dc,Mi}$, or prevent the reverse transmission of the DC-voltage-control MMC-BESS.

2) DC Line Fault

When a DC line fault occurs, the voltage at the fault position drops close to zero, resulting in the fault current produced by the rectifier rising rapidly and benefiting from the unidirectional continuity of the inverter LCC. The current I_{dcI} promptly drops to zero, and the MMCs do not need to block under DC line fault. Hence, the DC fault is similar to the serious sending-end AC fault with the active power deficit lasting longer (over several hundreds of milliseconds), causing grievous detriment on the receiving-end AC system.

Consequently, the FRT strategy for the DC line fault are also similar to that for the AC fault at rectifier, except that P_{es}^* will directly reach its rated value, and I_{dcM}^* quickly minishes to zero. Meanwhile, when I_{dcR} first increases to its

threshold value, the FR is utilized to convert the rectifier LCCs into the operating mode of the inverter to quench the fault arc.

C. Summary

Conclusively, the outer controller of the BESS considering FRT strategies is concluded, as shown in Fig. 12. The references u_c^* and P_{es}^* are determined by the type and severity of the fault. Limits are employed to maintain i_{es} drawn from the BESS within pre-specified safe operation limits.

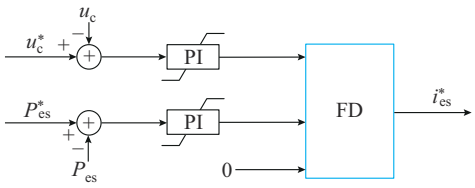

Fig. 12. Outer controller of BESS considering FRT strategies.

VI. Simulation Verifications

In this section, to validate the feasibility and effectiveness of the overvoltage suppression and the FRT improvement for the proposed FRT strategies coordinated with the MMC-BESS, two test systems are implemented on PSCAD/EMTDC. One is a monopolar BJ-HVDC system with only MMC1 and MMC2. The AC systems are imitated with the voltage sources and equivalent impedances listed in [19]. The other is a bipolar BJ-HVDC system involving all converters, which is inserted into the southern Jiangsu power grid. The sending-end AC systems of both systems are replaced by an equivalent voltage source with a short-circuit ratio of 8.0. The main parameters of the bipolar BJ-HVDC system are listed in Table I.

TABLE I
Main Parameters of Bipolar BJ-HVDC System

Type	Item	Rectifier	Inverter
General parameter	Nominal DC power	8000 MW	
	Nominal LCC DC voltage	800 kV	400 kV
	Nominal MMC DC voltage		400 kV
	Nominal DC current	5 kA	
	Length of DC overhead line	2172 km	
Parameter of MMC unit	Normal active power	667 MW (1+3 mode)/ 1000 MW (1+2 mode)	
	Number of SMs on an arm	200	
	Normal voltage of SM capacitor	2.0 kV	
	SM capacitance	16.67 μF	
	Arm reactance	25.33 mH	
Parameter of LCC transformer	Normal capacity	1200 MVA	
	Winding voltage (L-L)	525 kV/ 179.75 kV	510 kV/ 161.50 kV
	Leakage reactance	0.19	0.18
Parameter of MMC transformer	Normal capacity		1125 MVA
	Winding voltage (L-L)		510 kV/ 210 kV
	Leakage reactance		15%

The battery bank in each SM is composed of plenty of lithium-ion cells connected in series and parallel, and the first-order resistor-capacitor model is used as its equivalent circuit model [26]. Then, the MMC-BESSs are modeled in a detailed equivalent model based on [29]. The parameters of the battery bank are shown in Table II.

TABLE II
Parameters of Battery Bank

Type	Item	Value
General parameter	Nominal DC voltage	1.0 kV
	Nominal current	0.56 kA
	DC-DC converter inductor	6 mH
	DC-DC converter switch frequency	750 Hz
	Number of cells in parallel	56
	Number of cells in series	271
Parameter of battery cell	Normal capacity	2.35 Ah
	Normal voltage	3.7 V
	The maximum continuous discharging current	10 A
	Ohmic resistance	0.061 Ω
	Polarization resistance	0.021 Ω
	Polarization capacitance	1990 F

As shown in Table II, the corresponding total rated output power P_{esN} is equal to that of MMC in 1+3 mode, i.e., 667 MW. The total energy stored in one MMC-BESS $W_{es,total}$ is 5.7×10^5 MJ, while the one-kick maximum energy absorption of the CAEC is 200 MJ [15]. Thus, the MMC-BESS is undisputed qualified to suppress the overvoltage. 18650 cylindrical lithium-ion batteries are wildely applied in the industry, whose size is 18 mm in diameter, 65 mm in height, and 45 g in weight [25], [30]. Thus, the volume of the battery bank in each SM is about 0.25 m^3, and the weight is 683 kg. The battery bank is about three times the volume of an HB-SM, which is a thorny challenge for the application.

Assuming that the battery bank operates at the state of charge (SoC) from 20% to 80%, the maximum time that the BESS can maintain a rated power supply $T_{max}=667$ MW is about 256 s, which is calculated as:

$$T_{max}=\frac{SoC_{max}-SoC_{min}}{2P_{esN}}W_{es,total} \tag{12}$$

where SoC_{max} and SoC_{min} are the upper and lower limits of the SoC, respectively.

A. Overvoltage Suppression

In this subsection, the monopolar BJ-HVDC system in $1+2_{12}$ mode is utilized. In order to testify the superiority of the overvoltage suppression, the CAEC device is also involved, whose operation principle is introduced in [15]. As shown in Fig. 13, the CAEC consists of solid part, controllable part, a fast mechanical switch K, and a bypass switch (BPS). Both solid part and controllable part are the MOAs, and the corresponding rated reference voltages U_{ref} are 445 kV and 94 kV, respectively. Under normal operation, both BPS and K are always broken. Once the voltages of SM capacitors reach to the protection threshold (1.3 p.u.), K will be rapidly closed to bypass the MOA2 within 1 ms, thus, the total reference voltage of MOA reduces to consume the excessive energy.

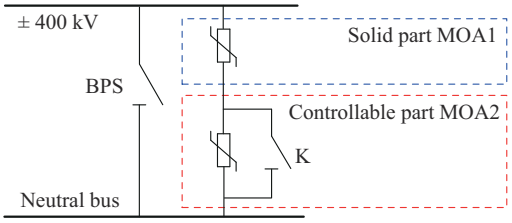

Fig. 13. CAEC device.

Assume that the time delay Δt_D is approximated as:

$$\Delta t_D = \frac{l_L}{\upsilon} + t_{FD} + t_{Tri} \tag{13}$$

where υ is the propagation velocity of the communication; l_L is the distance to one station from the other station, which is estimated to the length of DC line; t_{FD} is the time to detect the fault; and t_{Tri} is the total trigger delay. It is conservatively presumed that $\upsilon = 200$ km/ms, and $t_{Tri} = 3.0$ ms. Since the research on the fault detection methods [31] is beyond the scope of this paper, the detection time of 1.0 ms and 5.0 ms is adopted as the representative values to approximate t_{FD} and analyze the impact of the detection time.

Base quantities in this subsection are 800 kV for DC voltage, 5 kA for DC current, 4000 MW for active power delivered by converters, and 2.0 kV for SM capacitor voltage. Simulation results and corresponding analysis are given in the following subsections.

1) VSPG Fault in Internal MMC

At $t = 1.0$ s, a permanent phase a to ground fault is applied in internal MMC1. Three scenarios are simulated as follows.

1) Scenario A11: the proposed FRT strategy with MMC-BESS. The trigger sequence is referred to as in Section V.

2) Scenario A12: FRT strategy with the CAEC. The trigger sequence is similar to scenario A11, except the CAEC.

3) Scenario A13: only MMC1 blocks without other strategies.

For scenarios A11 and A12, the ACCBs of both MMC1 and MMC2 trip with 5-cycle (100 ms) delay after the fault occurs. In scenarios A12 and A13, all MMCs are classical.

The blocking logic of IGBT is generated by themselves with internal overcurrent fault protection which picks up when the current through any IGBT raises above 2 p.u., i.e., 6 kA in this paper. Thus, t_{FD} for the VSPG fault in internal MMC is short, and only 1 ms is adopted. The response and energy absorption for VSPG fault in internal MMC1 are shown in Figs. 14 and 15, respectively.

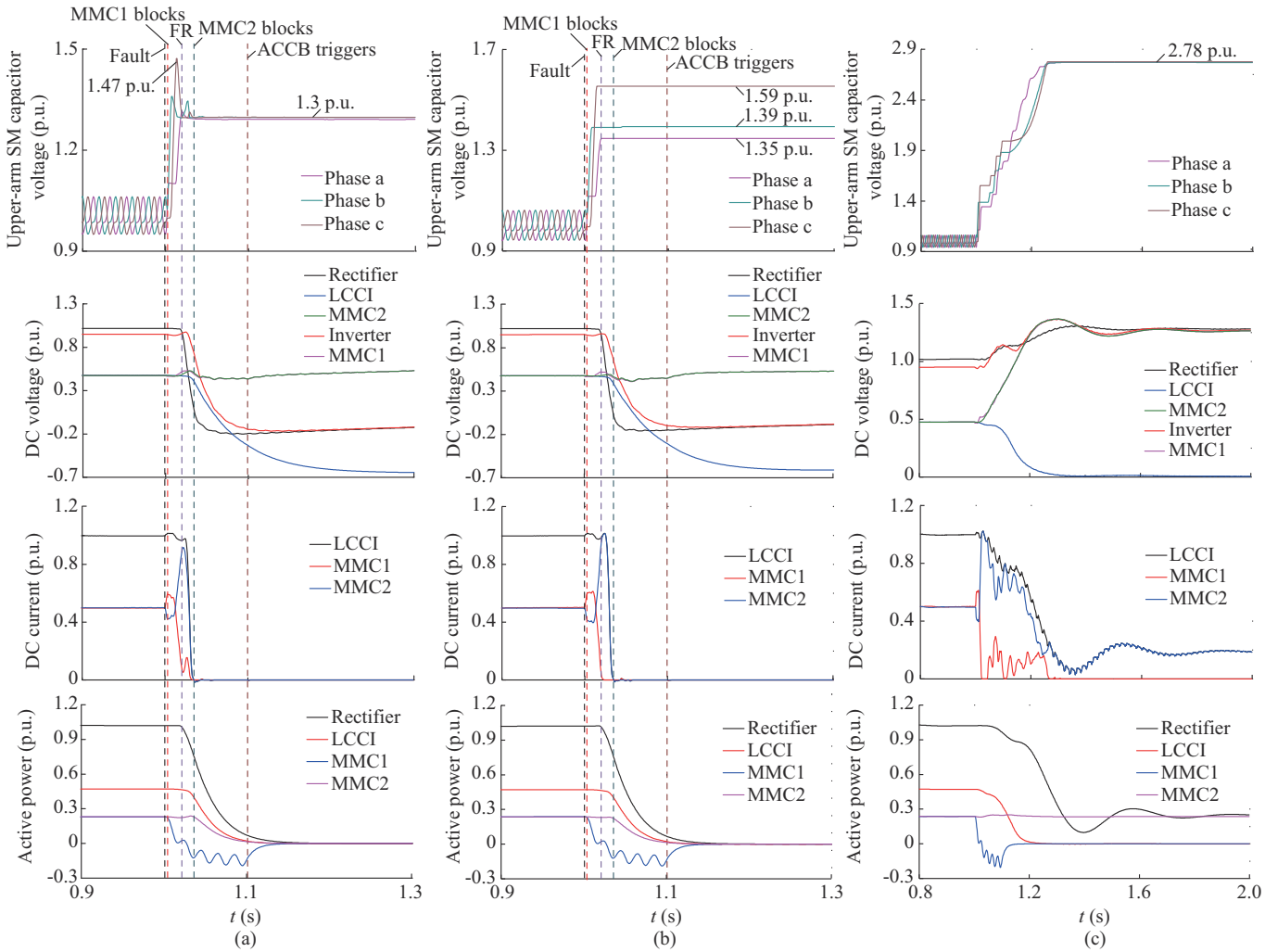

Fig. 14. Response for VSPG fault in internal MMC1. (a) Scenario A11. (b) Scenario A12. (c) Scenario A13.

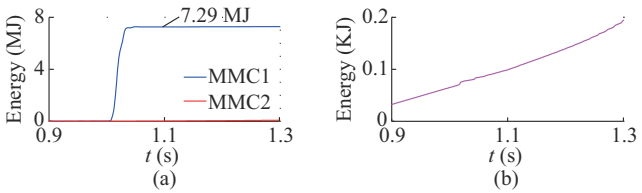

Fig. 15. Energy absorption for VSPG fault in internal MMC1. (a) MMC. (b) CAEC.

Note that, only the upper-arm SM capacitor voltages for the faulty MMC1 are displayed; rectifier and inverter denote the DC voltages measured at 800 kV DC bus port at the rectifier and inverter, respectively; and LCCI denotes the inverter LCC.

As shown in Fig. 14(c), if only the faulty MMC1 blocks, the surplus power will continuously charge both the MMC1 and MMC2, and ultimately the DC voltage is forced to increase near the open line voltage of the rectifier LCCs [32]. Worse still, the voltages of upper-arm SM capacitors will increase to 2.78 p.u., which is a fatal damage for the SMs. Thus, FR is an essential strategy to suppress the overvoltage.

Comparing the scenarios A11 and A12, the results of DC voltage, DC current, and active power are similar, whereas the upper-arm SM capacitor in phase c for scenario A12 still withstands about 1.59 p.u. of overvoltage. As shown in Fig. 15(b), the energy absorption of the CAEC is also very limited, which is induced by the leakage current. The reason is that the DC voltage at 400 kV DC bus increases slightly, and does not reach the reference voltage of MOA1, even though MOA2 has been bypassed. It is indicated that the CAEC reveals invalid effect under the VSPG faults. Such overvoltage is mainly induced by the negative half-cycles of valve-side non-fault phase voltages, which is also the reason that the active power injected to AC system from DC-side MMC1 is negative in Fig. 14(a), (b) and (c).

As depicted in Fig. 14(a), once the protection logic that the maximum SM capacitor voltage on any upper arm exceeds 1.3 p. u. is perceived, the corresponding upper-arm BESSs will be immediately activated to restrain the SM capacitor voltages near 1.3 p.u.. The maximum SM capacitor voltage in scenario A11 is 1.47 p. u., which is within the specified overvoltage tolerance (1.5 p. u.). As the healthy MMC2 is almost unaffected, the energy absorbed by MMC2 is minimal, as illustrated in Fig. 15(a). Notably, the MMC-BESS signifies excellent performance for the ability of overvoltage suppression.

2) GTPG Fault at Grid-side MMC

At $t=1$ s, a GTPG fault is applied at the grid-side MMC1, and is cleared after 0.1 s ($t=1.1$ s). Fault resistance is 0.01 Ω. The following three scenarios are simulated.

1) Scenario A21: the proposed FRT strategy with MMC-BESS. As shown in Fig. 12, I_{dcR}^{*2} is set to be 0.4 p.u., and u_{c}^{*2} is set to be 1.0 p.u.

2) Scenario A22: FRT strategy with the CAEC. As stated in [15], after the SM capacitor voltages reaches to 1.3 p.u., the switch K rapidly closes within 1 ms, sending a FR signal to the rectifier LCCs.

3) Scenario A23: no strategies. To analyze the impact of detection time, the detection time of both 1 ms and 5 ms is considered. The responses of the three scenarios for the GTPG fault with different detection time are shown in Figs. 16-19.

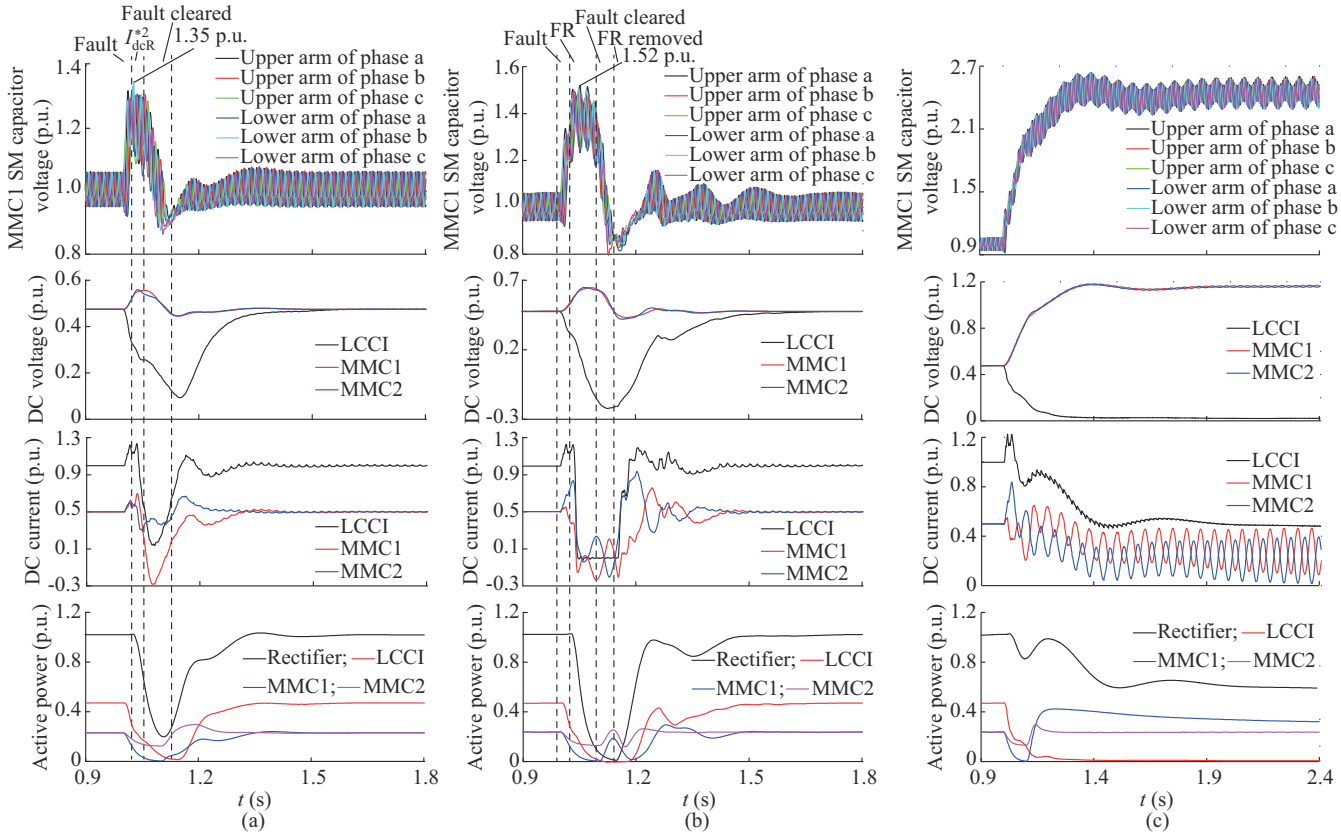

Fig. 16. Response for GTPG fault at grid-side MMC1 with 1-ms detection time. (a) Scenario A21. (b) Scenario A22. (c) Scenario A23.

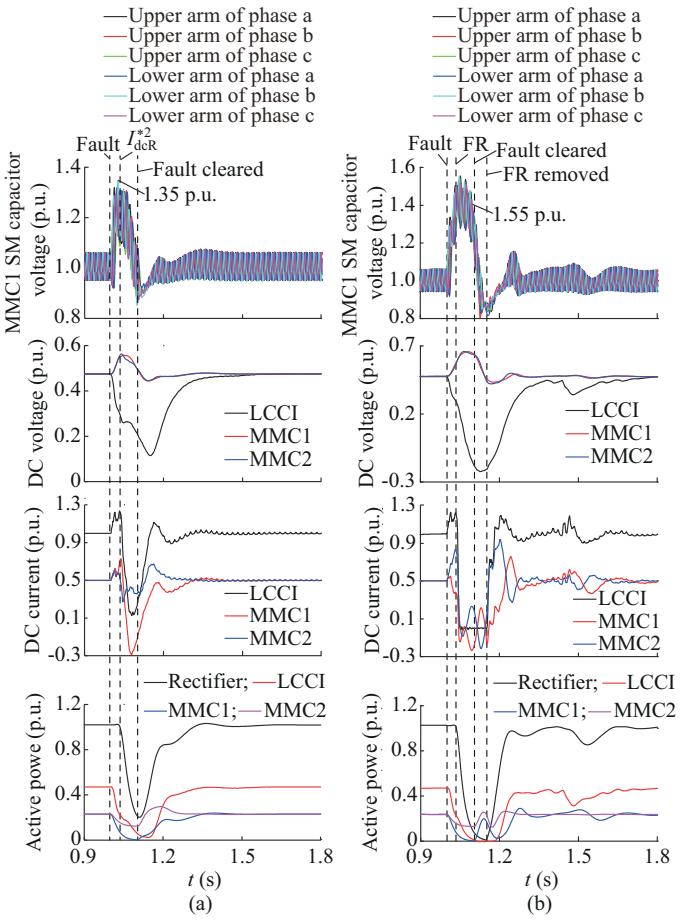

Fig. 17. Response for GTPG fault at grid-side MMC1 with 5-ms detection time. (a) Scenario A21. (b) scenario A22.

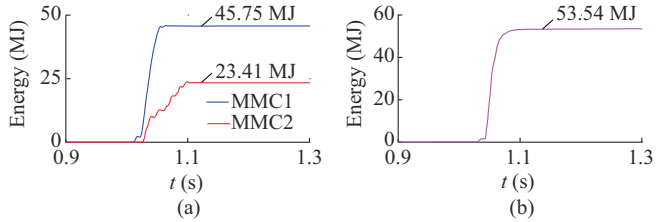

Fig. 18. Energy absorption for GTPG fault at grid-side MMC1 with 1-ms detection time. (a) MMC. (b) CAEC.

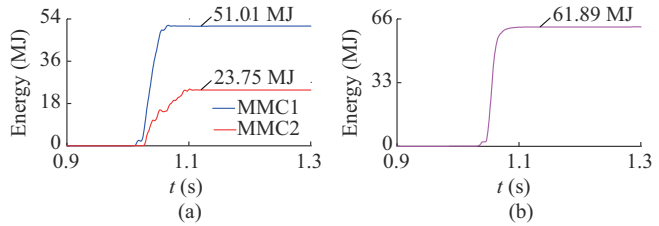

Fig. 19. Energy absorption for GTPG fault at grid-side MMC1 with 5-ms detection time. (a) MMC. (b) CAEC.

As shown in Figs. 16 and 17, after the grid-side AC fault, the CF inevitably occurs due to sudden decline of the AC voltage. Sequentially, the DC voltages drop swiftly, leading to prompt rises of the DC currents. The power deliveries of both MMC1 and LCC are absolutely restricted, though MMC2 is partly obstructed. If there is no other strategy, as visibly drawn in Fig. 16(c), the surplus DC power will compel the SMs of both MMC1 and MMC2 to overcharge near 2.7 p.u..

Figures 16(b) and 17(b) show that when the protection logic is detected, MOA2 is bypassed, and MOA1 is activated to absorb the superfluous power. With the help of FR and CAEC, the MMC DC voltage is limited to 0.65 p.u..

Nevertheless, the SM capacitor voltages are only bound to 1.52 p.u., since they could only be suppressed indirectly by dissipating the energy stacked at 400 kV DC bus. Besides, with 5-ms detection time, the fault recovery is longer and more terrible, and the CAEC absorbs more energy, as shown in Figs. 18(b) and 19(b). The reason is that the longer the fault detection is, the longer the time delay Δt_D is, and the more power the rectifier LCCs transmit. Thereby, the possibility of destroying the devices still exists. In addition, the current cut-off occurs unavoidably, resulting in longer and worse fault recovery.

Compared with the performance of the CAEC, once the maximum SM capacitor voltages exceed 1.3 p.u., the MMC-BESSs will be promptly activated to restrain SM capacitor voltages to 1.0 p.u., and the SM capacitor voltage is effectively restrained as the maximum 1.35 p.u.. As depicted in Figs. 16(b) and 17(b), the results are almost the same for different time delays, due to the powerful energy absorption capacity of MMC-BESS. Though, more energy is absorbed by the MMC-BESS for 5-ms detection time. The MMC-BESS reduces the SM capacitor voltages to a lower value, thus, the total energy absorbed by MMC1 and MMC2 exceeds that consumed by CAEC. Further, due to the absence of the current cut-off, the fault recovery is smoother and faster.

3) Summary

Based on the previous analysis, the proposed FRT strategies demonstrate better performance on overvoltage suppression, whereas the CAEC shows unsatisfactory effects. The longer the fault detection is, the more energy the devices dissipate.

B. Power Support

In order to effectively reveal the FRT improvement, the southern Jiangsu power grid is benchmarked on PSCAD/EMTDC. The network structure of the power grid is shown in Fig. 20, which is based on the planning data in the summer of 2025. The power grid comprises 53 buses of 500 kV, one bus of 1000 kV, and 58 branches of 500 kV. The total load of the power grid is about 43000 MW. The installed capacity is about 32000 MW, the base voltage is 525 kV, and the base capacity is 100 MVA. The whole bipolar BJ-HVDC system is inserted into the power grid, and the four converters at the inverter are connected to different 500 kV AC buses. Besides, the ±800 kV/7200 MW Jinping-Sunan LCC-HVDC (JS-HVDC) system is also built.

As the receiving-end AC faults have been studied in Section VI-A, only the sending-end GTPG fault and DC line fault are studied in this subsection. In the following subsections, due to the limited space, the generator phase angles of

G2, G3, and G5 and the active power flows of branches YS →CF, CSN→SB and ZJG→CY are measured. The arrows define the positive direction of the power flow. The base quantities for per-unitizing are 100 MW for the power flow, 8000 MW for the active power delivered by converters, and others are the same as described before. The power transmitted by converters are the sum of two poles.

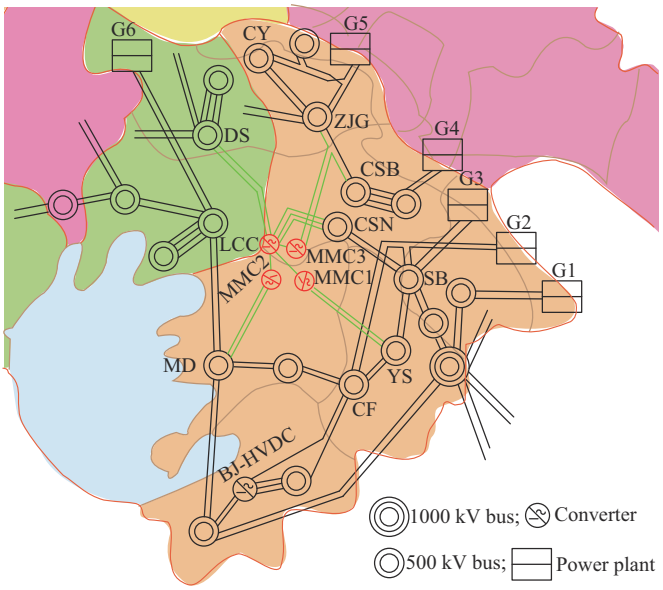

Fig. 20. Network structure of southern Jiangsu power grid.

1) AC Fault at Rectifier

A near-end fault on three phases with root meam square voltage dropping to 21% is simulated on the grid side of the rectifier LCCs after achieving steady state. The fault is applied at $t=0.2$ s and lasts for 0.2 s. Two scenarios are considered as follows.

1) Scenario B11: the proposed FRT strategy with MMC-BESS.

2) Scenario B12: conventional MMCs.

As two poles are symmetrical, only the behaviors of positive pole are exhibited as shown in Fig. 21. Under the sending-end AC fault, the BCC control of inverter LCC is activated to reduce its DC voltage to zero, while the MMC DC voltage hardly decreases due to the limitation of the voltage modulation ratio. Then, the DC voltage U_{dcR} drops to below U_{dcM}, resulting that the DC power drops to zero rapidly. Both the MMC2 and MMC3 output the active power, which is obedient to their power references, since they adopt constant active power control. MMC1 has to transmit the power reversely from AC system to afford the power extorted by MMC2 and MMC3. As a result, the power flows of branches YS→CF and CSN→SB alter significantly. As shown in Fig. 21(b), the loss of active power eventually leads to dramatic fluctuations in both DC and AC systems.

As indicated in Fig. 21(a), benefiting from the BESS, the active power losses of three MMCs are adequately compensated. Thus, the undulation of the power flows and generator power angles are remarkably mitigated, even though the power flow of branch CSN-SB connected to the inverter LCC still fluctuates greatly. Besides, the current references of the MMC2 and MMC3 are varied with the DC current of LCCI, leading to the absence of the current inversion of MMC1.

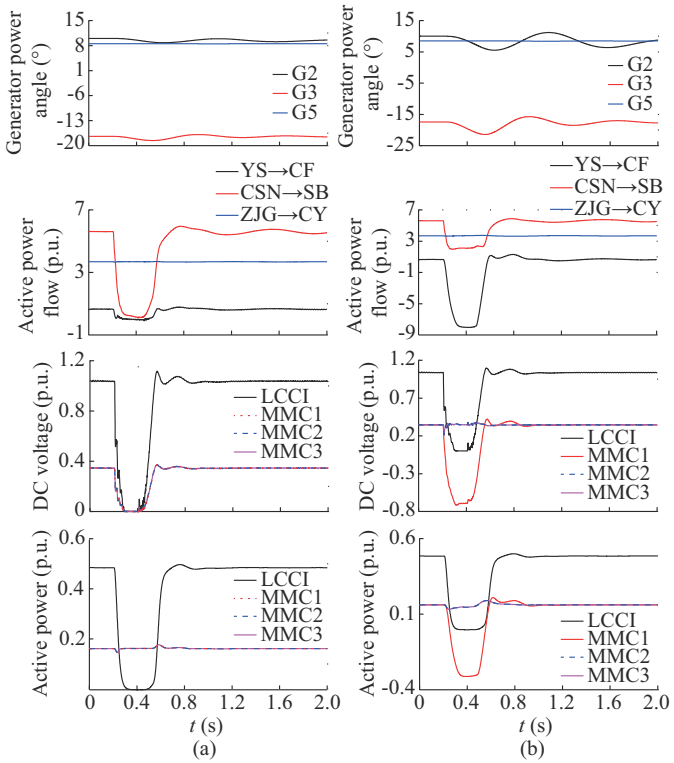

Fig. 21. Response for AC fault at rectifier. (a) Scenario B11. (b) Scenario B12.

2) DC Line Fault

In this subsection, at $t=0.2$ s, a pole-to-ground fault with fault resistance of 0.01 Ω is applied in the middle of the positive overhead DC line. Two scenarios are considered as follows.

1) Scenario B21: the proposed FRT strategy with MMC-BESS.

2) Scenario B22: conventional MMCs.

The DC fault handling strategy has been described in detail as in [11], and will be simplified later. When the DC current at the rectifier is larger than 1.5 p.u., the DC fault is detected, and then the FR is applied to the rectifier LCCs to cut off the fault current. After the fault current is cleared, the action of LCCs is held for another 0.2 s, so that the insulation of the fault point could be recovered [11]. Then, the system is shifted to the normal operation mode.

As shown in Fig. 22, after the fault occurs, the fault current induced by the rectifier LCCs rises rapidly. Due to the unidirectional continuity of the inverter LCC, the inverter cannot contribute to the fault current, and the inverter current promptly drops to zero. The responses for the DC line fault are similar to that for the AC fault at rectifier. Since the fault only occurs on the positive pole, half of the power is still delivered by DC system. Nevertheless, the active power loss of three MMCs can be fully compensated by the MMC-BESS.

3) Summary

According to the previous analysis, the MMC-BESS with the proposed FRT strategies could supply the power in a timely and reliable manner.

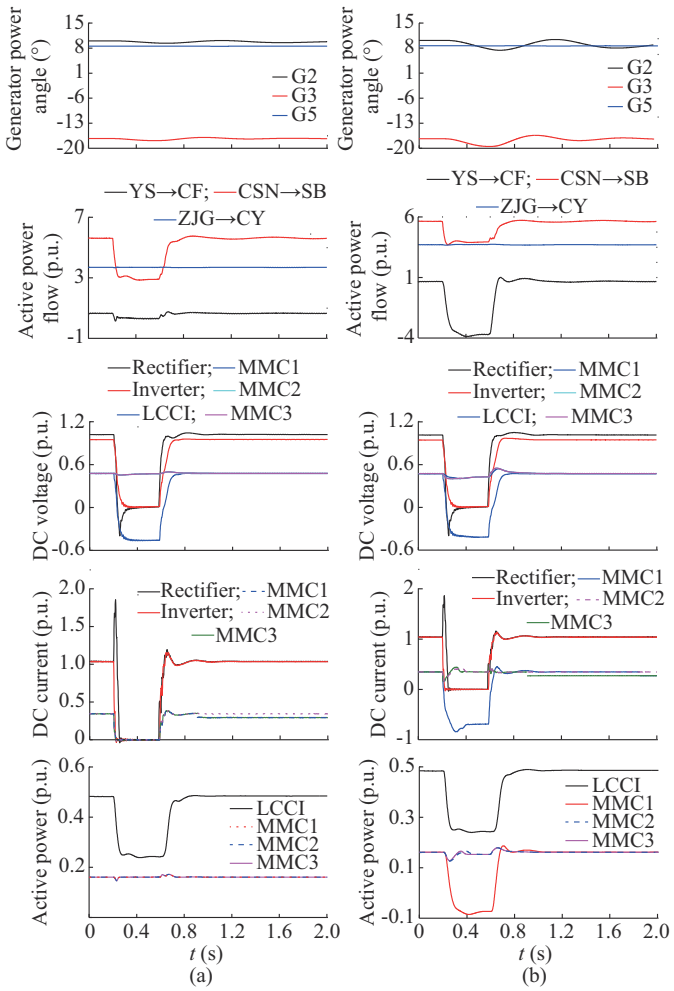

Fig. 22. Response for DC line fault. (a) Scenario B21. (b) Scenario B22.

VII. Conclusion

This paper demonstrates a novel alternative by employing the MMC-BESS to suppress serious overvoltage and supply emergency power. Firstly, the inducements of SM overvoltage are analyzed. Then, coordinated with MMC-BESS, new FRT strategies are proposed. Finally, several simulation scenarios are carried out to validate the feasibility and effectiveness. The conclusions are drawn as follows.

1) The analyses on the mechanisms of the SM overvoltage are strongly proven, which are mainly induced by the VSPG in internal MMC and the GTPG at grid-side MMC. Besides, the auxiliary energy consumption device is necessary to reliably relieve the overvoltage.

2) The effectiveness and superiority of the proposed FRT strategies based on MMC-BESS are forcefully validated via several simulation scenarios on PSCAD/EMTDC.

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