Small-signal Stability Analysis and Improvement with Phase-shift Phase-locked Loop Based on Back Electromotive Force Observer for VSC-HVDC in Weak Grids

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***Abstract*—Voltage source converter based high-voltage direct current (VSC-HVDC) transmission technology has been extensively employed in power systems with a high penetration of renewable energy resources. However, connecting a voltage source converter (VSC) to an AC weak grid may cause the converter system to become unstable. In this paper, a phase-shift phase-locked loop (PS-PLL) is proposed wherein a back electromotive force (BEMF) observer is added to the conventional phase-locked loop (PLL). The BEMF observer is used to observe the voltage of the infinite grid in the stationary *αβ* frame, which avoids the problem of inaccurate observations of the grid voltage in the *dq* frame that are caused by the output phase angle errors of the PLL. The VSC using the PS-PLL can operate as if it is facing a strong grid, thus enhancing the stability of the VSC-HVDC system. The proposed PS-PLL only needs to be properly modified on the basis of a traditional PLL, which makes it easy to implement. In addition, because it is difficult to obtain the exact impedance of the grid, the influence of short-circuit ratio (SCR) estimation errors on the performance of the PS-PLL is also studied. The effectiveness of the proposed PS-PLL is verified by the small-signal stability analysis and time-domain simulation.**

***Index Terms*—Phase-locked loop (PLL), small-signal model, stability improvement, voltage source converter based high-voltage direct current (VSC-HVDC), weak grid.**

I. Introduction

With the rapid development of wind power, photovoltaic and other renewable energy power generation technologies, voltage source converter based high-voltage direct current (VSC-HVDC) transmission has been widely applied in modern power systems and attracted the attention of researchers [1] - [3]. As the main active components in the VSC-HVDC system are power electronic devices, a potential oscillation problem may be induced and intensified due to their fast response [4], [5]. Several studies have revealed that the system stability is closely related to the dynamics of the phase-locked loop (PLL), especially when the AC system connected to VSC-HVDC is weak [6]-[10].

In voltage source converters (VSCs), the PLL is usually used to quickly and accurately obtain the grid voltage information such as phase angle and frequency to achieve synchronization with the AC grid [11]. Then the control system uses the output angle of the PLL to perform a *dq* transformation of the system voltage and current, thereby conducting vector control on the system. However, as analyzed in [7], when small-signal perturbations are added into the grid voltage, the controller *dq* frame is no longer aligned with the system *dq* frame because of the dynamic characteristics of the PLL and an angle deviation will appear between the two *dq* frames. When the grid impedance is high, the angle deviation introduced by the inaccurate phase lock will become unignorable and will make the control variables such as the voltage, current, and duty cycle in the controller have a certain deviation from the actual values. After being amplified by the inner- and outer-loop proportional-integral (PI) regulators, the voltage and current deviations from the actual values will affect the output voltage, current, and equivalent impedance of the converter. Eventually, it may cause oscillation and lead to system instability.

To address the stability problem introduced by a PLL in weak grids, researchers have proposed the corresponding feasible solutions. These solutions can be categorized into three types: ① optimizing the parameters of control system; ② improving the design of controller structure; ③ modifying the PLL structure. The first category focuses on the impacts of the PLL and other control parameters on the stability of the VSC system [7], [12]-[15]. References [12] and [13] effectively improved system stability by reducing the PLL con-

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trol bandwidth when the grid condition is fixed or known. Reference [14] proposed to improve the parameters of the current controller by considering the influence of the PLL so as to effectively reduce the negative influence of the PLL on the current control. Reference [15] proposed an improved vector current control method with an automatically adjustable outer-loop gain. However, these solutions are a trade-off between system stability and system dynamic response speed. The second category is to mitigate the impacts of the angle deviation between the two *dq* frames in the control channel by improving the design of the controller structure [16]-[18]. Reference [16] reshaped the *q*-axis impedance by inserting a notch filter into the PLL control loop. Reference [17] proposed an impedance controller directly linking the *q*-axis voltage to the *q*-axis current reference, thus improving the system stability by reshaping the *q*-axis impedance. Reference [18] proposed an improved vector control with a feed-forward branch, which promoted a faster reactive power response and thus enhanced the stability of the VSC-HVDC system. However, such solutions are more complicated to implement to a certain extent, and may not be applicable to different operation modes.

The former two categories partially mitigate the negative effect caused by the PLL. The third category pays attention to the PLL structure [19]-[21]. In [19], a symmetrical PLL was proposed, which can utilize the classical single-input single-output (SISO) impedance shaping to cancel the negative resistor behaviors caused by the PLL, thus enhancing the grid synchronization stability under weak grid conditions. In [20], an impedance-compensated PLL was proposed to increase the small-signal stability range towards the static power transfer capability limit. However, these solutions have a certain impact on the response speed and transient performance of the PLL. In addition, a method of referring the PLL measurement to an infinite artificial bus was proposed in [22], but the specific implementation method was not clearly explained.

Based on the aforementioned considerations, this paper proposes the phase-shift phase-locked loop (PS-PLL) based on the back electromotive force (BEMF) observer to improve system stability by approximately synchronizing with the infinite grid voltage. It allows a view that the VSC-HVDC system can operate as if it is facing a strong AC system even if the real AC system connected with the VSC-HVDC system is very weak. The proposed PS-PLL possesses good operation performance even when the observed grid voltage is inaccurate.

The rest of the paper is organized as follows. Section II describes the VSC-HVDC system and analyzes its steady-state operation characteristics. Sections III presents the small-signal model of the VSC-HVDC system and proposes the PS-PLL. Section IV analyzes the small-signal stability and illustrates the improvement of system stability by the PS-PLL. Section V verifies the effectiveness of the proposed PS-PLL through time-domain simulation results. Finally, the conclusions are given in Section VI.

II. Description of VSC-HVDC System and Analysis of Its Steady-state Operation Characteristics

Before analyzing the influence of the PLL on the stability of the VSC-HVDC system, the steady-state operation characteristics of the VSC-HVDC system under AC weak grids are first studied.

A. System Description

Figure 1 shows a schematic diagram of the classical VSC-HVDC system.

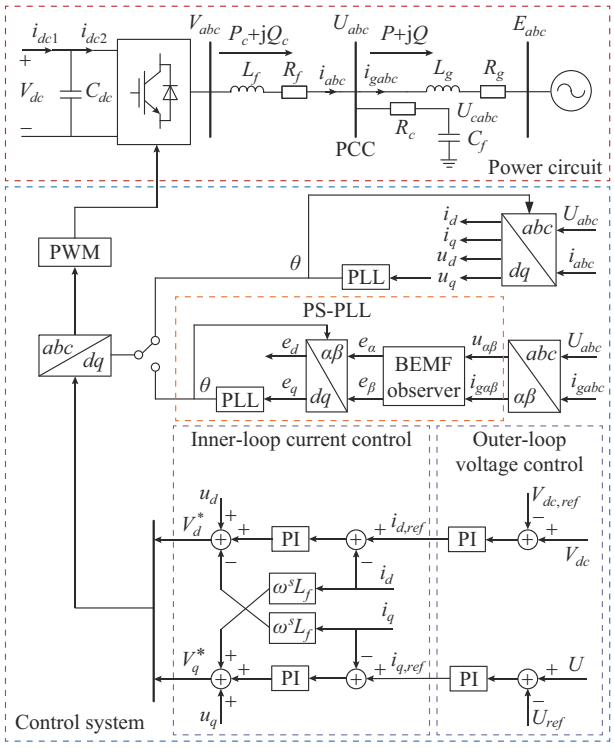

Fig. 1. Schematic diagram of classical VSC-HVDC system.

In Fig. 1, PWM stands for pluse width modulation; C_{dc} is the capacitance of the DC side; R_f and L_f are the equivalent resistance of the converter and the filter inductance of the filter, respectively; R_c and C_f are the damping resistance and capacitance of the filter, respectively; R_g and L_g are the equivalent resistance and inductance of the grid, respectively; E_{abc}, U_{cabc}, U_{abc}, and V_{abc} are the grid voltage, the voltage of the damping capacitance of the filter, the voltage of the point of common coupling (PCC), and the output voltage of the converter, respectively; i_{abc} is the current of the VSC flowing towards PCC; i_{gabc} is the current flowing from the PCC to the grid; V_{dc} is the DC-side voltage; i_{dc1} and i_{dc2} are the DC-side currents; P_c and Q_c are the output active and reactive power of the VSC flowing towards PCC, respectively; P and Q are the active and reactive power flowing from the PCC to the grid, respectively; u_d and u_q are the voltages of the PCC in the *dq* frame; i_d and i_q are the currents of the VSC flowing towards PCC in the *dq* frame; θ and ω^s are the synchronous phase angle and angle frequency of the grid, respectively; $u_{\alpha\beta}$ is the voltage of the PCC in the stationary $\alpha\beta$ frame; $i_{g\alpha\beta}$ is the current flowing from the PCC to the grid in the sta-

tionary $\alpha\beta$ frame; e_α and e_β are the grid voltages in the stationary $\alpha\beta$ frame obtained by the BEMF observer; e_d and e_q are the grid voltages in the dq frame obtained by the PS-PLL; $V_{dc,ref}$ is the DC-side reference voltage; U and U_{ref} are the magnitude of PCC voltage and its reference value, respectively; $i_{d,ref}$ and $i_{q,ref}$ are the reference currents of the VSC flowing towards PCC in the dq frame; and V_d^* and V_q^* are the reference output voltages of the converter in the dq frame.

The control system of the classical VSC-HVDC system in the dq frame is also shown in Fig. 1, which includes the outer-loop voltage control, inner-loop current control, and PLL. The PLL supplies a synchronous phase angle of the grid for the control system; the outer-loop voltage control produces current references in the dq frame for the inner-loop current control; and the inner-loop current control controls the actual active and reactive current tracking of the current reference value. The outer-loop voltage control consists of the DC voltage control and AC voltage control. In this paper, the average model is used in the frequency-domain analysis and the time-domain simulation to ignore the high-frequency dynamic process of the converter system including switching harmonics and small time delays.

B. Steady-state Operation Range Analysis

From Fig. 1, by using the grid voltage as the reference vector, it can be derived that [18]:

$$UE\sin\theta_{pcc}=P\omega^s L_g-QR_g \tag{1}$$

$$UE\cos\theta_{pcc}=U^2-PR_g-Q\omega^s L_g \tag{2}$$

where E is the magnitude of grid voltage; and θ_{pcc} is the phase angle of PCC voltage.

By exploiting $\sin^2\theta_{pcc}+\cos^2\theta_{pcc}=1$ and simplifying $(UE\sin\theta_{pcc})^2+(UE\cos\theta_{pcc})^2$, we can obtain:

$$\left(U^2\right)^2-\left(2PR_g+2Q\omega^s L_g+E^2\right)U^2+\left(PR_g+Q\omega^s L_g\right)^2+\left(P\omega^s L_g-QR_g\right)^2=0 \tag{3}$$

To ensure that there exist real roots in (3) for U, the following formula needs to be satisfied.

$$\Delta=\left(2PR_g+2Q\omega^s L_g+E^2\right)^2-4\left[\left(PR_g+Q\omega^s L_g\right)^2+\left(P\omega^s L_g-QR_g\right)^2\right]\geq 0 \tag{4}$$

Formula (4) is a constraint to ensure the existence of equilibrium in the VSC-HVDC system under a certain AC system operation condition.

However, for practical VSC-HVDC projects, some other constraints should also be included [23]. For the voltage constraint, it could be generalized based on the modulation index m as:

$$0\leq m=\frac{V_m}{V_{dc}/2}\leq 1 \tag{5}$$

where V_m is the amplitude of the converter output voltage, which can be obtained according to the Kirchhoff's voltage law.

For the current constraint, the main consideration is to keep the current requested by the control system within the rated current of the VSC. It could be generalized based on the VSC output voltage and power as:

$$abs\left(\frac{P_c+\mathrm{j}Q_c}{U\angle\theta_{pcc}}\right)\leq I_N \tag{6}$$

where I_N is the rated current on AC side of the VSC; and $abs(\cdot)$ is the function to take the absolute value.

Based on the constraints mentioned above, the steady-state operation range of the VSC-HVDC system can be obtained. In order to analyze the influence of different AC system strengths on the operation range of the VSC-HVDC system, the short-circuit ratio (SCR) is introduced, which can be expressed by (7) in per unit.

$$SCR=\frac{1}{\left|Z_{sys}\right|}=\frac{1}{\left|R_g+\omega^s L_g\right|} \tag{7}$$

where Z_{sys} is the equivalent impedance of the grid.

With variations of SCR, by solving $\Delta=0$ in (4), the minimum required reactive power can be obtained and is illustrated in Fig. 2. As shown in Fig. 2, the operation range of the VSC-HVDC system is closely related to SCRs. When the AC system is strong (e.g., $SCR=5$, 10), the VSC-HVDC system could always transmit a maximum active power of 1 p.u. without an extra reactive power demand. When the AC system is weak (e.g., $SCR=1$), because the VSC is not capable of providing excessive reactive power to the AC system due to its limited capacity, it is difficult for the VSC-HVDC system to transmit an active power of 1 p.u.. From Fig. 2, it can also be observed that when the value of the SCR is large, the minimum required reactive power changes little with active power. When the SCR is small, the minimum required reactive power changes greatly with active power, and the minimum required reactive power is high when the active power approaches the rated power.

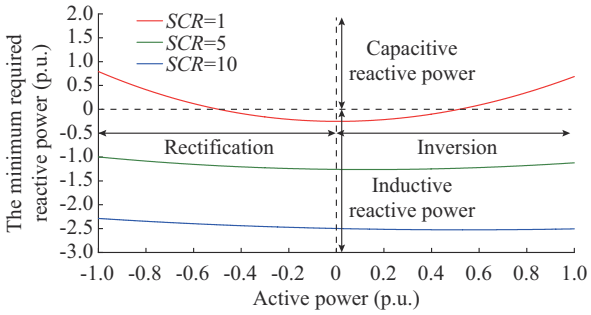

Fig. 2. Steady-state operation range of VSC-HVDC system with different SCRs.

On this basis, it is essential to further explore the small-signal stability of the VSC-HVDC system whose operation point is in the steady-state range. Firstly, the small-signal modeling of the VSC-HVDC system and eigenvalue analysis are required when analyzing the small-signal stability with different SCRs [6].

III. Small-signal Model of VSC-HVDC System and Proposed PS-PLL

A. Dynamic Modeling of VSC-HVDC System

Figure 1 shows the main circuit and control structure of a typical VSC-HVDC system from which the dynamic model can be derived.

1) AC System Equations

Using the equal-amplitude *dq* rotation transformation, the dynamic model of the AC system can be derived as:

$$L_f\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_d^s \\ i_q^s \end{bmatrix} = \begin{bmatrix} v_d^s \\ v_q^s \end{bmatrix} - \begin{bmatrix} u_d^s \\ u_q^s \end{bmatrix} - R_f\begin{bmatrix} i_d^s \\ i_q^s \end{bmatrix} - \omega^s L_f\begin{bmatrix} -i_q^s \\ i_d^s \end{bmatrix} \tag{8}$$

$$L_g\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_{gd}^s \\ i_{gq}^s \end{bmatrix} = \begin{bmatrix} u_d^s \\ u_q^s \end{bmatrix} - \begin{bmatrix} E_d^s \\ E_q^s \end{bmatrix} - R_g\begin{bmatrix} i_{gd}^s \\ i_{gq}^s \end{bmatrix} - \omega^s L_g\begin{bmatrix} -i_{gq}^s \\ i_{gd}^s \end{bmatrix} \tag{9}$$

$$C_f\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} u_{cd}^s \\ u_{cq}^s \end{bmatrix} = \begin{bmatrix} i_d^s \\ i_q^s \end{bmatrix} - \begin{bmatrix} i_{gd}^s \\ i_{gq}^s \end{bmatrix} - \omega^s C_f\begin{bmatrix} -u_{cq}^s \\ u_{cd}^s \end{bmatrix} \tag{10}$$

$$\begin{bmatrix} u_d^s \\ u_q^s \end{bmatrix} = \begin{bmatrix} u_{cd}^s \\ u_{cq}^s \end{bmatrix} + R_c\begin{bmatrix} i_d^s \\ i_q^s \end{bmatrix} - R_c\begin{bmatrix} i_{gd}^s \\ i_{gq}^s \end{bmatrix} \tag{11}$$

where u_{cd}^s and u_{cq}^s are the capacitor voltages of the AC filter in the *dq* frame; v_d^s and v_q^s are the output voltages of the converter in the *dq* frame; i_{gd}^s and i_{gq}^s are the grid currents in the *dq* frame flowing from the PCC to the grid; E_d^s and E_q^s are the grid voltages in the *dq* frame; and the superscript *s* represents the variables in the system *dq* frame.

2) DC-link Power Balance Equations

The DC-link power balance equations can be developed as:

$$\begin{cases} C_{dc}\dfrac{\mathrm{d}V_{dc}}{\mathrm{d}t} = i_{dc1} - i_{dc2} \\ i_{dc1} = \dfrac{P_{in}}{V_{dc}} \\ i_{dc2} = \dfrac{3\left(v_d^s i_d^s + v_q^s i_q^s\right)}{2V_{dc}} \approx \dfrac{3\left(u_d^s i_d^s + u_q^s i_q^s\right)}{2V_{dc}} \end{cases} \tag{12}$$

where P_{in} is the input power of the VSC on the DC side, and the loss of the converter is ignored here to facilitate later calculations.

3) PLL Control Equations

The block diagram of the PLL is depicted in Fig. 3, where the superscript *c* represents the variables in the controller *dq* frame; θ^c and ω^c are the synchronous phase angle and angle frequency of the grid obtained by the PLL, respectively; K_{ppll} and K_{ipll} are the PI control parameters of the PLL; and ω_0 is the rated angular frequency of the grid.

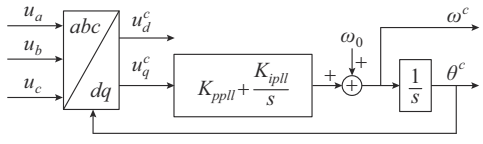

Fig. 3. Block diagram of PLL.

The dynamic equations of the PLL are illustrated as:

$$\begin{cases} \dfrac{\mathrm{d}x_{pll}}{\mathrm{d}t} = u_q^c \\ \dfrac{\mathrm{d}\theta^c}{\mathrm{d}t} = \omega^c = K_{ppll}u_q^c + K_{ipll}x_{pll} + \omega_0 \end{cases} \tag{13}$$

where x_{pll} is the state variable in the PLL.

4) Outer-loop Voltage Control Equations

The deviation between the DC/AC voltage and its reference value is expressed as:

$$\begin{cases} \dfrac{\mathrm{d}x_1}{\mathrm{d}t} = v_{dc} - v_{dc,ref} \\ \dfrac{\mathrm{d}x_2}{\mathrm{d}t} = u_{ac} - u_{ac,ref} \end{cases} \tag{14}$$

where x_1 and x_2 are the state variables in outer-loop voltage control; $v_{dc,ref}$ and $u_{ac,ref}$ are the DC-side reference voltage and the reference voltage at the PCC point, respectively; and u_{ac} is the voltage at the PCC point, which can be derived as:

$$u_{ac} = \sqrt{\left(u_d^c\right)^2 + \left(u_q^c\right)^2} \tag{15}$$

Then, the reference values of the current in the *dq* frame are developed as:

$$\begin{cases} i_{d,ref} = K_{pv_{dc}}\left(v_{dc} - v_{dc,ref}\right) + K_{iv_{dc}}x_1 \\ i_{q,ref} = K_{pu_{ac}}\left(u_{ac} - u_{ac,ref}\right) + K_{iu_{ac}}x_2 \end{cases} \tag{16}$$

where $K_{pv_{dc}}$, $K_{iv_{dc}}$ and $K_{pu_{ac}}$, $K_{iu_{ac}}$ are the PI control parameters for the outer-loop DC voltage control and AC voltage control, respectively.

5) Inner-loop Current Control Equations

The current deviation of the inner-loop current control can be written as:

$$\begin{cases} \dfrac{\mathrm{d}x_3}{\mathrm{d}t} = i_{d,ref} - i_d^c \\ \dfrac{\mathrm{d}x_4}{\mathrm{d}t} = i_{q,ref} - i_q^c \end{cases} \tag{17}$$

where x_3 and x_4 are the state variables in the inner-loop current control.

Then, the output voltages of the converter in the *dq* frame can be described as:

$$\begin{cases} v_d^c = K_{pi}\left(i_{d,ref} - i_d^c\right) + K_{ii}x_3 + u_d^c - \omega^c L_f i_q^c \\ v_q^c = K_{pi}\left(i_{q,ref} - i_q^c\right) + K_{ii}x_4 + u_q^c + \omega^c L_f i_d^c \end{cases} \tag{18}$$

where K_{pi} and K_{ii} are the PI control parameters for the inner-loop current control.

B. Relationship Between System and Controller dq Frames

As mentioned before, when small-signal perturbations exist, the controller *dq* frame will not align with the system *dq* frame due to the dynamic process of PLL, and an angle deviation named $\Delta\theta$ will appear between the two *dq* frames. The relationship between the variables in the system *dq* frame and controller *dq* frame is expressed as:

$$\begin{bmatrix} X_d^c+\Delta x_d^c \\ X_q^c+\Delta x_q^c \end{bmatrix} = \begin{bmatrix} \cos(\Delta\theta) & \sin(\Delta\theta) \\ -\sin(\Delta\theta) & \cos(\Delta\theta) \end{bmatrix} \begin{bmatrix} X_d^s+\Delta x_d^s \\ X_q^s+\Delta x_q^s \end{bmatrix} \approx \begin{bmatrix} 1 & \Delta\theta \\ -\Delta\theta & 1 \end{bmatrix} \begin{bmatrix} X_d^s+\Delta x_d^s \\ X_q^s+\Delta x_q^s \end{bmatrix} \tag{19}$$

where $\Delta\theta=\theta^c-\theta^s$; and X and Δx are the steady-state variables and the small-signal perturbation variables, respectively.

In the steady state, $X_d^s=X_d^c$ and $X_q^s=X_q^c$. By eliminating the steady-state variables and ignoring the high-order terms, the small-signal representations of two *dq* frames can be expressed as:

$$\begin{bmatrix} \Delta x_d^c \\ \Delta x_q^c \end{bmatrix} = \begin{bmatrix} X_q^s \\ -X_d^s \end{bmatrix} \Delta\theta + \begin{bmatrix} \Delta x_d^s \\ \Delta x_q^s \end{bmatrix} \tag{20}$$

C. PS-PLL

Previous studies have reached the conclusion that the stability of VSC-HVDC system will be enhanced by improving the design of the controller and the control parameters of PLL. However, it is difficult to eliminate the negative influences caused by the PLL by designing the structure of the controller and to balance the system response speed and stability by designing the control parameters. This difficulty motivates the research for a new solution that attempts to improve the system stability based on the nature of the problem. If the PLL can approximately synchronize with the infinite grid voltage, a converter connected with a stiff grid will be obtained. Consequently, the system would no longer face a weak grid and the angle deviation caused by the dynamic response of the PLL would not deteriorate the system stability.

In order to allow the converter to obtain the information of the infinite grid voltage, the BEMF observer technology in electric motors is adapted as [24] and [25]. Unlike the need of electric machines to utilize the transient impedance when calculating the BEMF, the PS-PLL will not need the transient impedances of fast electromagnetic processes under disturbance conditions. The grid operation is regarded as a quasi-steady-state process, and the change of the equivalent grid impedance is small. The rapid change of the grid impedance in the transient process is not the main concern. The proposed PS-PLL may allow the system to restore stability even if the system is unstable. The grid impedance can be regarded as a continuously varying steady-state impedance, and the PS-PLL only needs to regularly readjust the estimation of grid impedance according to the new steady state of the system.

According to the mathematical model of the transmission line in (8)-(11), under the conditions of known PCC voltage and current, the infinite grid voltage can be observed through the BEMF observer. Then the infinite grid voltage obtained by the BEMF observer is used as the input of the traditional PLL, and the infinite grid voltage information such as the phase angle and frequency can be obtained. Since the *dq* transformation requires the output phase angle of the PLL, the BEMF observer observes the infinite grid voltage in the *αβ* frame to avoid an inaccurate observation for the grid voltage in the *dq* frame caused by the output phase angle error of the PLL.

Reference [20] proposes an impedance-conditioned PLL that makes the PLL introduce an impedance-conditioning term, and then the VSC control system can be virtually synchronized to the infinite grid. This approach is similar to that proposed in this paper based on the principle of improving system stability. However, the impedance conditioning in [20] is obtained by subtracting the quasi-stationary voltage drop on the virtual impedance from the local voltage measurement of the PLL input, which ignores the differential term of inductance. Since the PLL is a dynamic component, ignoring the differential term is not conducive to the transient response speed of the PLL. Therefore, different from the impedance-conditioned PLL, the PS-PLL proposed in this paper considers the inductance differential term and replaces it with an integral link, avoiding the large error that may be caused by the actual uneven current differential.

It should also be noted that it is difficult to obtain the exact impedance of the grid. Thus, it may be impractical to accurately observe the grid voltage. In this paper, it will be demonstrated that an inaccurately estimated grid impedance can also improve the stability to a certain extent. Furthermore, the proposed PS-PLL can be combined with the method of estimating the equivalent grid impedance [26], [27], which will be our future research work.

The block diagram of the proposed PS-PLL is shown in Fig. 4. The BEMF observer uses a PI controller to control the AC component in a closed loop, instead of a proportion resonant (PR) controller. Although the PR controller can achieve an error-free adjustment, it may introduce additional high-order stability problems in the VSC-HVDC system. In addition, the closed-loop control system of the BEMF observer using the PI controller is stable, and the tracking error of the AC component can be reduced by increasing the parameters of the PI controller, so the BEMF observer also has good control performance.

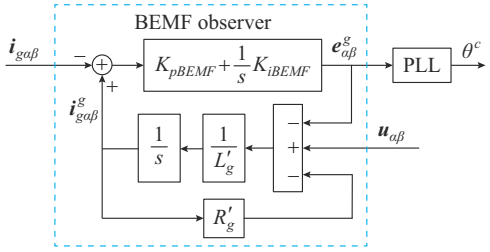

Fig. 4. Block diagram of proposed PS-PLL.

From Fig. 4, we can obtain:

$$\begin{cases} \left(\boldsymbol{i}^g_{g\alpha\beta}-\boldsymbol{i}_{g\alpha\beta}\right)\left(K_{pBEMF}+\dfrac{K_{iBEMF}}{s}\right)=\boldsymbol{e}^g_{\alpha\beta} \\ \left(\boldsymbol{u}_{\alpha\beta}-\boldsymbol{e}^g_{\alpha\beta}-R'_g\boldsymbol{i}^g_{g\alpha\beta}\right)\dfrac{1}{L'_g s}=\boldsymbol{i}^g_{g\alpha\beta} \end{cases} \tag{21}$$

where $\boldsymbol{u}_{\alpha\beta}$ and $\boldsymbol{i}_{g\alpha\beta}$ are the PCC voltage and current observed by the BEMF observer in the stationary *αβ* frame, respectively; $\boldsymbol{e}^g_{\alpha\beta}$ and $\boldsymbol{i}^g_{g\alpha\beta}$ are the grid voltage and current observed by the BEMF observer in the stationary *αβ* frame, respectively; R'_g and L'_g are the estimated grid resistance and inductance,

respectively; and K_{pBEMF} and K_{iBEMF} are the parameters of the PI controller for the BEMF observer.

Eliminating the intermediate variables $\boldsymbol{i}^g_{\alpha\beta}$, it can be derived that:

$$\boldsymbol{e}^g_{\alpha\beta}=\frac{K_{pBEMF}s+K_{iBEMF}}{L'_g s^2+\left(R'+K_{pBEMF}\right)s+K_{iBEMF}}\left[\boldsymbol{u}_{\alpha\beta}-\left(L'_g s+R'_g\right)\boldsymbol{i}_{g\alpha\beta}\right] \tag{22}$$

To facilitate the analysis and calculation later, the pole-zero cancellation method is used to simplify (22). We set:

$$\begin{cases}K_{pBEMF}=\omega_t L'_g\\ K_{iBEMF}=\omega_t R'_g\end{cases} \tag{23}$$

Substituting (23) into (22), we can obtain:

$$\boldsymbol{e}^g_{\alpha\beta}=\frac{\omega_t}{s+\omega_t}\left[\boldsymbol{u}_{\alpha\beta}-\left(L'_g s+R'_g\right)\boldsymbol{i}_{g\alpha\beta}\right] \tag{24}$$

where ω_t is the control bandwidth of the BEMF observer.

Then, by transforming the variables in (24) into the *dq* frame, the dynamic equations of the BEMF observer can be expressed as:

$$\begin{cases}\dfrac{\mathrm{d}e^g_d}{\mathrm{d}t}-\omega^c e^g_q+\omega_t e^g_d=\omega_t u^c_d-\omega_t L'_g\dfrac{\mathrm{d}i^c_{gd}}{\mathrm{d}t}+\omega_t\omega^c L'_g i^c_{gq}-\omega_t R'_g i^c_{gd}\\ \dfrac{\mathrm{d}e^g_q}{\mathrm{d}t}+\omega^c e^g_d+\omega_t e^g_q=\omega_t u^c_q-\omega_t L'_g\dfrac{\mathrm{d}i^c_{gq}}{\mathrm{d}t}-\omega_t\omega^c L'_g i^c_{gd}-\omega_t R'_g i^c_{gq}\end{cases} \tag{25}$$

Equations (13) and (24) give out the dynamic equations of the PS-PLL.

IV. Small-signal Stability Analysis and Improvement of System Stability by PS-PLL

A. Small-signal Model of VSC-HVDC System

A nonlinear state-space model of the VSC-HVDC system including the AC system, VSC main circuit, and VSC control system is developed. In Lyapunov linearization theory, the general nonlinear system shown in (25) can be linearized near the steady-state operation point x_0 to get the small-signal model (26).

$$\dot{\boldsymbol{x}}=\boldsymbol{f}(\boldsymbol{x})+\boldsymbol{u} \tag{26}$$

$$\Delta\dot{\boldsymbol{x}}=\boldsymbol{A}\Delta\boldsymbol{x} \tag{27}$$

where $\boldsymbol{f}(\boldsymbol{x})$ is the function of $\boldsymbol{x}$; $\boldsymbol{u}$ is the input vector; and $\boldsymbol{A}=\left.\dfrac{\partial\boldsymbol{f}(\boldsymbol{x}_0+\Delta\boldsymbol{x})}{\partial\boldsymbol{x}}\right|_{\boldsymbol{x}=\boldsymbol{x}_0}$.

Based on the state equations of the AC system, controller, and PLL, the state variables of the VSC system are:

$$\boldsymbol{x}=\left[i^s_d,i^s_q,u^s_{cd},u^s_{cq},i^s_{gd},i^s_{gq},v_{dc},\left(e^g_d,e^g_q\right),x_{pll},\theta,x_1,x_2,x_3,x_4\right]^{\mathrm{T}}$$

The VSC-HVDC system using a conventional PLL is equivalent to a 13th-order system, where the first 6 variables are actual circuit parameters in the system *dq* frame. After using the proposed PS-PLL, the system is equivalent to a 15th-order system.

B. Influence of SCR on Stability of VSC-HVDC System

1) Eigenvalue Locus Analysis of System Using Conventional PLL

The parameters of a VSC-HVDC system is shown in Table I. This paper mainly focuses on the influence mechanism of the PLL on the stability of the VSC-HVDC system. Therefore, a set of controller parameters is adjusted here. On one hand, it can demonstrate the influence of the PLL on the stability of the VSC-HVDC system under a weak grid. On the other hand, it can improve the control effect of other control links.

TABLE I
Parameters of VSC-HVDC System

Symbol	Description	Value
V_{dc}	DC-side rated voltage	1200 V
E	Rated voltage of AC system	690 V
P	Rated active power of AC system	1 MW
ω^s	Line frequency of AC system	100π rad/s
C_{dc}	DC-side capacitance	20 mF
R_g	Equivalent resistance of AC system	0.01 Ω
L_g	Equivalent inductance of AC system	0.3 mH
R_f	Equivalent resistance of VSC	0 Ω
L_f	Filter inductance	0.5 mH
R_c	Filter damping resistance	0.5 Ω
C_f	Filter capacitance	500 μF
K_{ppll}	Proportional gain of PLL	0.2
K_{ipll}	Integral gain of PLL	20
$K_{pv_{dc}}$	Proportional gain of DC voltage control	0.2
$K_{iv_{dc}}$	Integral gain DC voltage control	20
$K_{pu_{ac}}$	Proportional gain of AC voltage control	0.2
$K_{iu_{ac}}$	Integral gain of AC voltage control	20
K_{pi}	Proportional gain of current loop	2
K_{ii}	Integral gain of current loop	20

Using the parameters listed in Table I, the eigenvalue analysis method based on the small-signal model is utilized to assess the system stability. Figure 5 depicts the eigenvalue locus of the VSC-HVDC system using a conventional PLL when the SCR of the system changes from 5 to 1. The red arrows in Fig. 5 represent how the eigenvalues move when the SCR changes from 5 to 1. In order to observe the locus near the imaginary axis clearly, only parts of the eigenvalues are intercepted. From Fig. 5, it can be observed that a decreasing SCR drives a pair of dominant poles (λ_1,λ_2) toward the unstable region, while the other poles stay stable, and the system becomes unstable when the SCR becomes less than 1.38. Since the eigenvalue corresponding to the critical SCR is $0.062\pm\mathrm{j}21.195$, it can be inferred that the oscillation frequency is $\omega/(2\pi)=3.37$ Hz. Their modal participation factors are calculated, as shown in Table II. For poles λ_1 and λ_2, it can be observed from Table II that the state variables of the PLL (x_{pll} and θ) have the largest modal participation factors. Therefore, it can be concluded that the PLL mainly

leads to the positive eigenvalue or instability, which indicates that the improvement of PLL can improve the stability of the system under weak grid conditions.

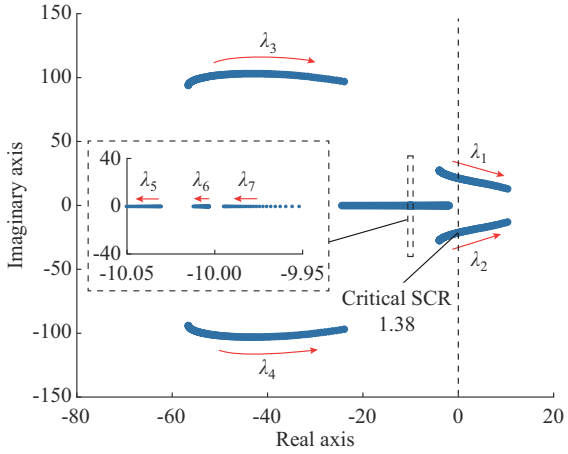

Fig. 5. Eigenvalue locus of VSC-HVDC system using conventional PLL when SCR changes from 5 to 1.

TABLE II
MODAL PARTICIPATION FACTORS

State variable	Modal participation factor when $\lambda_{1,2}=0.062\pm j21.195$	State variable	Modal participation factor when $\lambda_{1,2}=0.062\pm j21.195$
i_d^s	0	x_{pll}	0.4954
i_q^s	0	θ	0.4769
u_{cd}^s	0	x_1	0.0067
u_{cq}^s	0	x_2	0.0034
i_{gd}^s	0	x_3	0.0056
i_{gq}^s	0	x_4	0.0112
v_{dc}	0.0007		

2) Eigenvalue Locus Analysis of System Using PS-PLL

The eigenvalue locus of the VSC-HVDC system using the proposed PS-PLL without SCR estimation errors when the SCR changes from 5 to 1 is shown in Fig. 6.

It can be observed that all the eigenvalues are on the left half plane, which means that the VSC-HVDC system can operate stably using the proposed PS-PLL under the condition of an accurate grid impedance estimation. Therefore, by approximately synchronizing to an infinite grid voltage, the interaction between the controller and the angle deviation caused by the dynamic response of PLL is mitigated. In addition, the eigenvalue locus performs similarly to the situation using the PLL in a strong AC system.

C. Comparison of Stability Improvement

By keeping $U=1$ p.u., the Q-P curve when $SCR=1$ is illustrated by the blue line in Fig. 7. The red dotted line represents the corresponding reactive power of the VSC-HVDC system under different AC system operation conditions when $\Delta=0$, which also means the minimum reactive power required for the existence of equilibrium in the VSC-HVDC system when $SCR=1$. $\Delta=0$ represents the critical situation of the existence of equilibrium in the VSC-HVDC system.

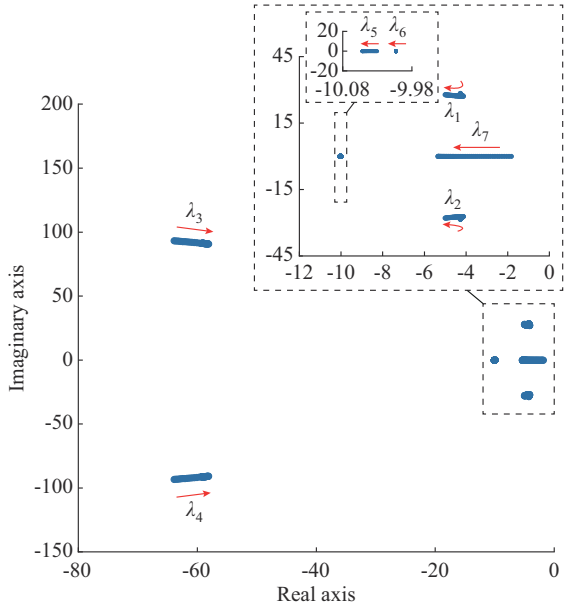

Fig. 6. Eigenvalue locus of VSC-HVDC system using proposed PS-PLL without SCR estimation errors when SCR changes from 5 to 1.

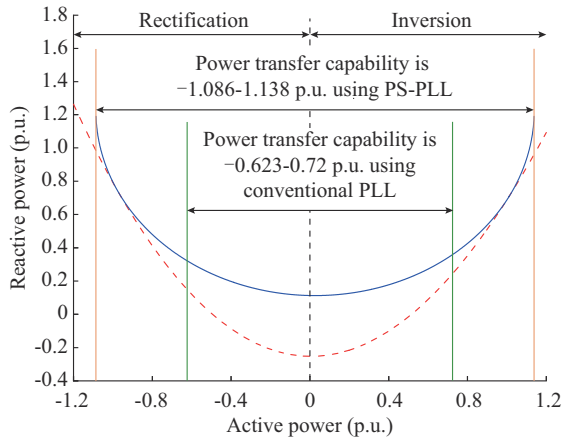

Fig. 7. Steady operation range of VSC-HVDC system with $U=1$ p.u. when $SCR=1$.

The active power area pointed by the green and orange arrows are the actual steady operation range of the VSC-HVDC system using the previously-developed small-signal model. It can be observed that the power transfer capability of the system using the PLL is −0.623 - 0.72 p.u.. However, the power transfer capability using the proposed PS-PLL without SCR estimation errors is −1.086 - 1.138 p.u., which effectively moves the steady operation range towards the theoretical steady operation range limitation of the system. This occurs inherently without modifying any PI controller gains of the PLL. The result indicates that approximately synchronizing with the infinite grid voltage in the PS-PLL implementation does significantly improve the stability of the system.

D. Influence of Estimation Errors of Grid Impedance

As previously mentioned, the accurate estimation of the grid impedance is difficult to obtain. Therefore, the influence

of the estimation errors of the grid impedance on the proposed PS-PLL is studied here. Figure 8 shows the eigenvalue locus of the VSC-HVDC system using the proposed PS-PLL with $SCR = 1$ when SCR estimation errors vary from −30% to 30%. It can be observed that no eigenvalue crosses the right half plane, which demonstrates that a partially inaccurate estimated grid impedance including both negative estimation errors and positive estimation errors can also improve the system stability. In addition, the eigenvalue closest to the right half plane corresponds to positive estimation errors; the system will be closer to the stability limit and will have a relatively poor dynamic response in comparison with negative estimation errors.

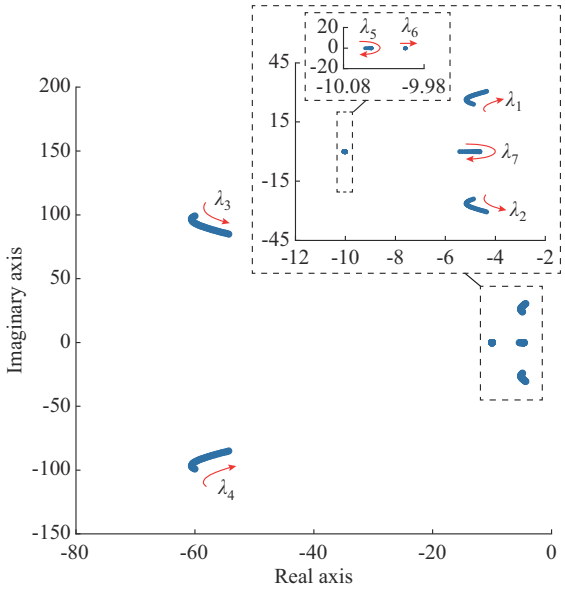

Fig. 8. Eigenvalue locus of VSC-HVDC system using proposed PS-PLL with $SCR = 1$ when SCR estimation errors vary from −30% to 30%.

V. Simulation Verification

In order to verify the effectiveness of the proposed PS-PLL, the simulation model of the VSC-HVDC system shown in Fig. 1 is developed in the MATLAB/Simulink environment. The relevant system and control parameter values can be found in Table I. The simulation results of the VSC-HVDC system using the conventional PLL and proposed PS-PLL without SCR estimation errors are shown in Fig. 9.

As shown in Fig. 9(a) and (b), when the SCR of the system changes from 5 to 1.38 at $t = 5$ s, the DC voltage and transmission power of the system using the conventional PLL exhibit oscillations. It can also be observed from Fig. 9(a) that the time for 10 oscillation cycles is 3.0002 s, which can infer that the simulated oscillation frequency is about 3.33 Hz. The results validate the theoretical analysis of Fig. 5. After the introduction of the proposed PS-PLL at simulation time $t = 10$ s, the system becomes stable. Figure 9(c) presents both the actual grid voltage and the grid voltage observed by the BEMF observer in the stationary $\alpha\beta$ frame. It can be observed that the BEMF observer displays good performance as the estimated SCR coincides with the real SCR. All the results show that the small-signal stability analysis is correct and the proposed PS-PLL based on BEMF observer has the ability to improve the stability of the system.

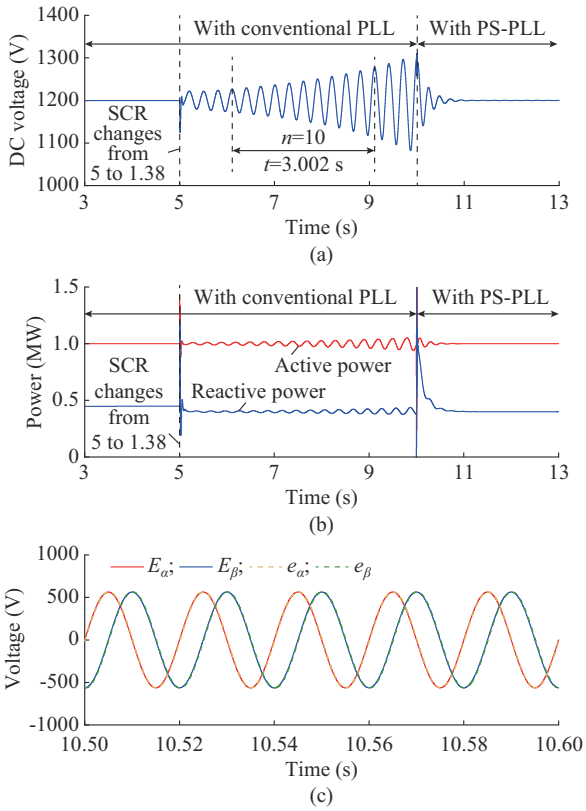

Fig. 9. Simulation results of VSC-HVDC system using conventional PLL and proposed PS-PLL without SCR estimation errors. (a) DC voltage. (b) Transmission power. (c) Actual and observed grid voltage in stationary $\alpha\beta$ frame.

To test the influence of an inaccurate SCR estimation on the performance of the PS-PLL, Fig. 10 and Fig. 11 show the simulation results of the VSC-HVDC system using the proposed PS-PLL with 30% SCR estimation errors and with −30% SCR estimation errors, respectively. It can be observed that the system can remain stable under both conditions. In addition, as shown in Fig. 10(b) and Fig. 11(b), after introducing the PS-PLL, the system using the PS-PLL with positive SCR estimation errors becomes stable after 1.6 s; however, the time required for the system using the PS-PLL with negative SCR estimation errors is 1.2 s. It can be concluded that the PS-PLL with positive estimation errors has a relatively poor dynamic response, which validates the analytical results of Fig. 8. It can be also observed from Fig. 10(c) and Fig. 11(c) that the BEMF observer can approximately observe the infinite grid voltage in the case of partial inaccurate SCR estimation, and the error is within an acceptable level. Therefore, although the proposed PS-PLL may not synchronize the infinite grid voltage exactly, the VSC-HVDC system can also operate as expected as if it is facing a strong grid. The results indicate that a partially inaccurate estimation of the SCR will not have too much influence on the performance of the PS-PLL, and it is more advantageous to estimate a smaller SCR the SCR of a system is uncertain.

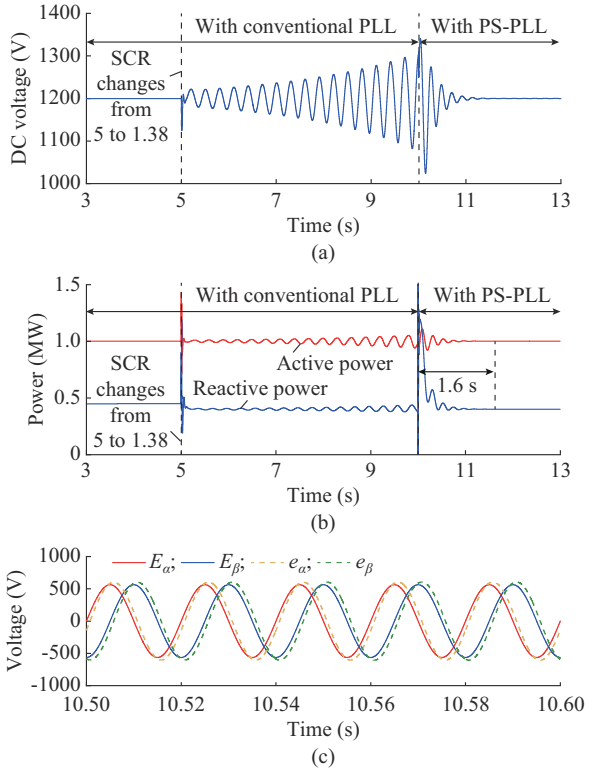

Fig. 10. Simulation results of VSC-HVDC system using conventional PLL and proposed PS-PLL with 30% SCR estimation errors. (a) DC voltage. (b) Transmission power. (c) Actual and observed grid voltage in stationary $\alpha\beta$ frame.

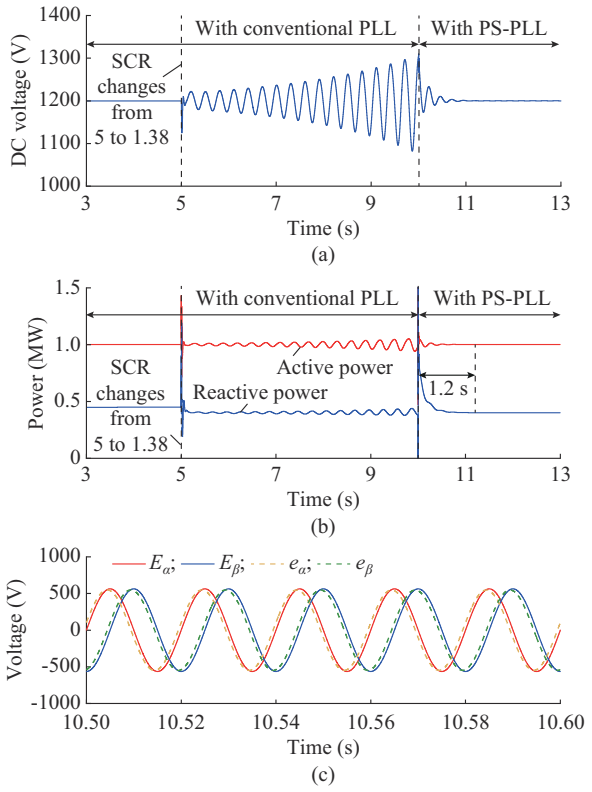

Fig. 11. Simulation results of VSC-HVDC system using conventional PLL and proposed PS-PLL with −30% SCR estimation errors. (a) DC voltage. (b) Transmission power. (c) Actual and observed grid voltage in stationary $\alpha\beta$ frame.

VI. Conclusion

In this paper, a PS-PLL based on a BEMF observer is proposed to address the oscillations caused by the PLL of a VSC-HVDC system under weak grid conditions. The proposed PS-PLL can approximately synchronize with the infinite grid voltage; thus, the VSC can operate as if it is facing a strong grid. It can be easily implemented and applied to various system operation conditions. Since the output phase angle error of the PLL may cause an inaccurate observation of the grid voltage in the dq frame, the BEMF observer observes the grid voltage in the $\alpha\beta$ frame. The small-signal stability analysis demonstrates that the proposed PS-PLL can significantly improve the stability of the system.

Furthermore, the PS-PLL possesses good operation performance under the condition of a partially inaccurate SCR estimation. However, the positive estimation errors of SCR give a relatively poor dynamic response. Hence, the negative estimation errors of the SCR are more advantageous when we estimate the SCR of a system. Simulation results verify the analytical results and the effectiveness of the proposed PS-PLL.

References

[1] J. M. Carrasco, L. G. Franquelo, J. T. Bialasiewicz *et al*., "Power-electronic systems for the grid integration of renewable energy sources: a survey," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 4, pp. 1002-1016, Jun. 2006.

[2] P. Bresesti, W. L. Kling, R. L. Hendriks *et al*., "HVDC connection of offshore wind farms to the transmission system," *IEEE Transactions on Energy Conversion*, vol. 22, no. 1, pp. 37-43, Mar. 2007.

[3] N. Flourentzou, V. G. Agelidis, and G. D. Demetriades, "VSC-based HVDC power transmission systems: an overview," *IEEE Transactions on Power Electronics*, vol. 24, no. 3, pp. 592-602, Mar. 2009.

[4] H. Liu and J. Sun, "Impedance-based stability analysis of VSC-based HVDC systems," in *Proceedings of 14th Workshop on Control and Modeling for Power Electronics*, Salt Lake City, USA, Oct. 2013, pp. 1-8.

[5] L. Shen, M. Barnes, R. Preece *et al*., "The effect of VSC-HVDC control on AC system electromechanical oscillations and DC system dynamics," *IEEE Transactions on Power Delivery*, vol. 31, no. 3, pp. 1085-1095, Jun. 2016.

[6] J. Zhou, H. Ding, S. Fan *et al*., "Impact of short circuit ratio and phase-locked-loop parameters on the small signal behavior of a VSC-HVDC converter," *IEEE Transactions on Power Delivery*, vol. 29, no. 5, pp. 2287-2296, Oct. 2014.

[7] B. Wen, D. Boroyevich, R. Burgos *et al*., "Analysis of d-q small-signal impedance of grid-tied inverters," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 675-687, Jan. 2016.

[8] D. Dong, B. Wen, D. Boroyevich *et al*., "Analysis of phase-locked loop low-frequency stability in three-phase grid-connected power converters considering impedance interactions," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 1, pp. 310-321, Jan. 2015.

[9] X. Zhang, D. Xia, Z. Fu *et al*., "An improved feedforward control method considering PLL dynamics to improve weak grid stability of grid-connected inverters," *IEEE Transactions on Industry Applications*, vol. 54, no. 5, pp. 5143-5151, Sept.-Oct. 2018.

[10] Y. Song and F. Blaabjerg, "Analysis of middle frequency resonance in DFIG system considering phase-locked loop," *IEEE Transactions on Power Electronics*, vol. 33, no. 1, pp. 343-356, Jan. 2018.

[11] J. Wang, J. Liang, F. Gao *et al*., "A method to improve the dynamic performance of moving average filter-based PLL," *IEEE Transactions on Power Electronics*, vol. 30, no. 10, pp. 5978-5990, Oct. 2015.

[12] B. Wen, D. Dong, D. Boroyevich *et al*., "Impedance-based analysis of grid-synchronization stability for three-phase paralleled converters," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 26-38, Jan. 2016.

[13] M. Cespedes and J. Sun, "Adaptive control of grid-connected inverters based on online grid impedance measurements," *IEEE Transactions*

on Sustainable Energy, vol. 5, no. 2, pp. 516-523, Apr. 2014.
[14] S. Zhou, X. Zou, D. Zhu *et al*., "An improved design of current controller for LCL-type grid-connected converter to reduce negative effect of PLL in weak grid," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 2, pp. 648-663, Jun. 2018.
[15] A. Egea-Alvarez, S. Fekriasl, F. Hassan *et al*., "Advanced vector control for voltage source converters connected to weak grids," *IEEE Transactions on Power Systems*, vol. 30, no. 6, pp. 3072-3081, Nov. 2015.
[16] K. M. Alawasa, Y. A. I. Mohamed, and W. Xu, "Active mitigation of subsynchronous interactions between PWM voltage-source converters and power networks," *IEEE Transactions on Power Electronics*, vol. 29, no. 1, pp. 121-134, Jan. 2014.
[17] J. Fang, X. Li, H. Li *et al*., "Stability improvement for three-phase grid-connected converters through impedance reshaping in quadrature-axis," *IEEE Transactions on Power Electronics*, vol. 33, no. 10, pp. 8365-8375, Oct. 2018.
[18] G. Wu, J. Liang, X. Zhou *et al*., "Analysis and design of vector control for VSC-HVDC connected to weak grids," *CSEE Journal of Power and Energy Systems*, vol. 3, no. 2, pp. 115-124, Jun. 2017.
[19] D. Yang, X. Wang, F. Liu *et al*., "Symmetrical PLL for SISO impedance modeling and enhanced stability in weak grids," *IEEE Transactions on Power Electronics*, vol. 35, no. 2, pp. 1473-1483, Feb. 2020.
[20] J. A. Suul, S. D'Arco, P. Rodríguez *et al*., "Impedance-compensated grid synchronisation for extending the stability range of weak grids with voltage source converters," *IET Generation, Transmission & Distribution*, vol. 10, no. 6, pp. 1315-1326, Apr. 2016.
[21] L. Huang, H. Xin, Z. Li *et al*., "Grid-synchronization stability analysis and loop shaping for PLL-based power converters with different reactive power control," *IEEE Transactions on Smart Grid*, vol. 11, no. 1, pp. 501-516, Jan. 2020.
[22] M. F. M. Arani and Y. A. I. Mohamed, "Analysis and performance enhancement of vector-controlled VSC in HVDC links connected to very weak grids," *IEEE Transactions on Power Systems*, vol. 32, no. 1, pp. 684-693, Jan. 2017
[23] Z. Zhang, Z. Xu, W. Jiang *et al*., "Operating area for modular multilevel converter based high-voltage direct current systems," *IET Renewable Power Generation*, vol. 10, no. 6, pp. 776-787, Feb. 2016.
[24] H. Kim, M. C. Harke, and R. D. Lorenz. "Sensorless control of interior permanent-magnet machine drives with zero-phase lag position estimation," *IEEE Transactions on Industry Applications*, vol. 39, no. 6, pp. 1726-1733, Nov.-Dec. 2003.
[25] F. Lin, Y. Hung, J. Chen *et al*., "Sensorless IPMSM drive system using saliency back-EMF-based intelligent torque observer with MTPA control," *IEEE Transactions on Industrial Informatics*, vol. 10, no. 2, pp. 1226-1241, May 2014.
[26] J. Fang, J. Yu, Y. Zhang *et al*., "An estimation-based solution to weak-grid-induced small-signal stability problems of power converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 4, pp. 4558-4572, Aug. 2021.
[27] J. Fang, H. Deng, and S. M. Goetz, "Grid impedance estimation through grid-forming power converters," *IEEE Transactions on Power Electronics*, vol. 36, no. 2, pp. 2094-2104, Feb. 2021.

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