Reclosing Current Limiting for DC Line Faults in VSC-HVDC Systems

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***Abstract*—The problem of reclosing current limiting in voltage source converter based high-voltage direct current (VSC-HVDC) systems is becoming more and more serious. A soft reclosing scheme for DC permanent faults is presented in this paper. Because the converter voltages of stations at both terminals of the disconnected faulty line may be different, the choice of which terminal to reclose first will affect the reclosing overcurrent. A method for selecting the terminal to reclose first is investigated to achieve a minimum peak overcurrent during the reclosing process. In order to ensure that the hybrid DC circuit breaker (HDCCB) adapts to the needs of the reclosing process better, the traditional HDCCB is improved by adding a soft reclosing module (SRM). The energy dissipated in the arresters is significantly reduced when using the improved HDCCB. The improved HDCCB will be able to reclose multiple times safely and thus increase the possibility of successful reclosing. Moreover, the recovery time after the HDCCB is successfully reclosed is very short with the improved HDCCB and its control principles. Simulation results show that this proposed scheme is capable of limiting the reclosing overcurrent when the fault still exists.**

***Index Terms*—Soft reclosing, current limiting, voltage source converter based high-voltage direct current (VSC-HVDC), DC fault.**

I. Introduction

VOLTAGE source converter based high-voltage direct current (VSC-HVDC) systems are developing very fast nowadays, and multi-terminal VSC-HVDC (VSC-MTDC) systems are very attractive owing to their advantages such as the reduction in investment and the increase in power transmission stability [1]. Although the advantages of VSC-HVDC systems are significant, the protection system faces enormous challenges [2], [3]. A VSC-HVDC system is vulnerable to DC line faults because any DC line fault will result in a steep increase in the fault current due to the small impedance of the DC system [4]-[6]. Power transmission is usually based on the overhead lines in a VSC-MTDC system [7]. Therefore, the reliability of the VSC-MTDC system may be affected by frequent temporary faults in overhead lines.

To satisfy the requirements of the VSC-HVDC protection system, the use of a DC circuit breaker (DCCB) to interrupt the fault current is now considered to be the most effective and reliable protection scheme [8]-[12]. Hybrid DCCBs (HDCCBs) comprising joint mechanical switches and semiconductor devices have combined rapidity and economy, giving them good application prospects [13], [14]. Previous research on HDCCBs mainly focused on the fault-current interruption process, fault-current limiting methods, and topology optimization [15]-[19]. There are also some meaningful studies on the reclosing operation process [20]. When an HDCCB is reclosed to the system, there is a certain probability that the fault still exists; therefore, the HDCCB will be opened again, and this is the open-close-close (O-C-C) process. Owing to the existence of a fault, the fault current rapidly increases during the open-close-open (O-C-O) process, thus affecting the safety and stability of the system.

It is significant to limit the overcurrent during the fault recovery process to achieve a soft restart for the faulty line. References [21]-[23] discuss several reclosing strategies for HDCCBs based on traveling wave theory. By detecting certain characteristic waveforms on the line before reclosing, it is possible to identify whether the fault is clear and decide whether to reclose. However, these methods require complex control, and the indicators that distinguish the two types of faults are not completely reliable. Reference [24] improves the active and reactive control method of the converter to minimize the impact of DC faults on the AC system, but the current on the DC side is still considerable during the O-C-O process. In [25] and [26], a sequential autoreclosing method for HDCCBs is proposed to achieve a soft reclosing process by limiting the reclosing current. However, the principles for choosing which terminal to reclose is not discussed, and the surge arresters in the HDCCB may become overloaded. Moreover, the recovery time of this method is quite long. In [27], a resistive fault current limiter, which is currently widely used, is studied. A soft reclosing module (SRM) model based on a resistive current-limiting scheme is proposed in this study. In [28], a soft reclosing scheme is presented to limit the reclosing current. Starting from the current-limiting model presented in [28], this study extends the detailed and comprehensive analysis of this model. A

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method for choosing which terminal to reclose first is presented, the energy dissipation stress of the O-C-O process is analyzed, and most importantly, a soft reclosing scheme is proposed.

The remainder of this paper is organized as follows. Section II describes the operation principles of HDCCBs before reclosing and the impact of disconnection of HDCCBs. A soft reclosing scheme suitable for both two-terminal VSC-HVDC and VSC-MTDC systems is proposed in Section III. The reclosing process of the improved HDCCB with SRM is discussed in Section IV. The effectiveness of the soft reclosing scheme and improved HDCCB proposed in this paper is verified by simulation studies in Section V. Section VI concludes this paper.

II. Operation Principles of HDCCBs Before Reclosing and Impact of Disconnection of HDCCBs

In this section, the structure and operation principles of the traditional and improved HDCCBs before reclosing are presented. Then, the impact of the disconnection of HDCCBs is analyzed.

A. Structure and Operation Principles of Traditional and Improved HDCCBs Before Reclosing

The structures of the traditional and improved HDCCBs before reclosing are shown in Fig. 1.

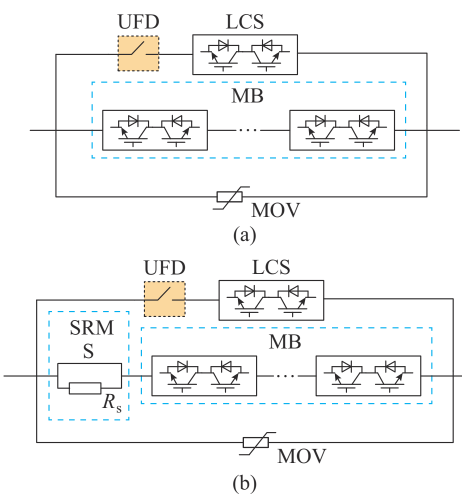

Fig. 1. Structures of traditional and improved HDCCBs before reclosing. (a) Traditional HDCCB. (b) Improved HDCCB.

The traditional HDCCB is improved by adding an SRM to the main breaker (MB). Before reclosing, the mechanical switch S in Fig. 1(b) is closed, the reclosing current-limiting resistor R_s is bypassed, and the operation principles of traditional and improved HDCCBs are the same. The main branch is composed of an ultrafast fault disconnector (UFD) and a load commutation switch (LCS). The commutation branch is composed of many semiconductor devices connected in series called the MB. During normal operation, current flows through the main branch. When a fault is detected, the LCS will be opened, and the fault current is commutated from the LCS to the MB. After the fault current is fully commutated to the MB, the UFD will be triggered to open, and the opening time is approximately 2 ms. When the UFD is able to withstand the system voltage, the MB will be opened, and the energy is absorbed by a metal oxide varistor (MOV).

B. Impact of Disconnection of HDCCBs

VSC-HVDC transmission systems can be divided into two-terminal VSC-HVDC and VSC-MTDC systems according to the number of converter stations. The impacts of disconnection of HDCCBs on these two types of systems are different. Note that all of the systems analyzed in this study are under a master-slave control strategy.

1) Two-terminal VSC-HVDC System

In a two-terminal VSC-HVDC system, one station is in DC voltage control, and the other is in active power control. After the DC line is lost, these two stations will be separated, and the station that controls the active power will lose control of its DC voltage. To illustrate this case, Fig. 2 shows the structure of a two-terminal system in which station 1 is feeding power and station 2 is receiving power.

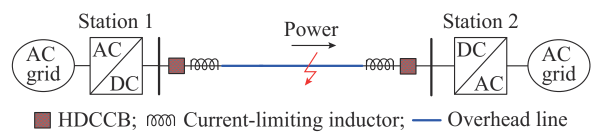

Fig. 2. Structure of two-terminal VSC-HVDC system.

Figure 3 shows a diagram of active power control in the VSC-HVDC system, where P_{ref} and P_{AC} are the reference and actual values of the active power, respectively; PI_{max} and PI_{min} are the maximum and minimum output-limiting values of the proportional-integral (PI) controller; V_{AC} is the AC-side voltage; U_{dlim} and K_{dlim} are the input and protection control coefficients of the voltage limiter, respectively; and I_{ref} is the reference current delivered to the inner-current control loop.

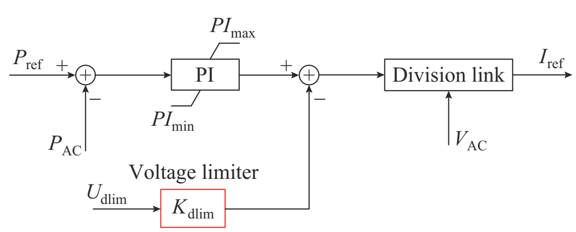

Fig. 3. Diagram of active power controller in a VSC-HVDC system.

The voltage limiter will be activated to limit the converter voltage once it exceeds a predetermined upper-lower boundary for security consideration. On the basis of the operation principle of the voltage limiter, U_{dlim} is expressed as:

$$U_{dlim} = \begin{cases} U_d - U_{up} & U_d > U_{up} \\ U_d - U_{low} & U_d < U_{low} \\ 0 & U_{low} \le U_d \le U_{up} \end{cases} \tag{1}$$

where U_d is the converter voltage; and U_{up} and U_{low} are the upper and lower boundaries of the predetermined converter voltage, respectively.

If station 1 controls the active power and station 2 controls the DC voltage, the converter voltage of station 1 will be determined only by the control system at station 1 after the DC line is lost. After fault isolation, the control system in Fig. 3 will continue working and delivering a positive reference current I_{ref} to the inner-loop current controller. In such cases, the AC-side current continues to charge the DC capacitor in the converter after fault isolation, and the converter voltage of station 1 will continue to increase until the voltage limiter in the control system is activated. Once the voltage limiter is activated, it participates in the control process of the converter voltage with the PI controller, and the maximum converter voltage $U_{d,max}$ can be calculated using (2). Similarly, if station 2 controls the active power, there will be an undervoltage on the DC side of station 2 after the HDCCB is disconnected, and the minimum converter voltage $U_{d,min}$ is also given in (2).

$$\begin{cases} U_{d,max} = \dfrac{PI_{max}}{K_{dlim}} + U_{up} \\ U_{d,min} = \dfrac{PI_{min}}{K_{dlim}} + U_{low} \end{cases} \tag{2}$$

2) VSC-MTDC System

There are several connection types of VSC-MTDC systems including circular, radial, and meshed connections. The five-terminal VSC-HVDC system developed in [29], which contains both circular and radial connections, is adopted in this study. Figure 4 shows the structure of this system, where stations 1, 2, and 5 form a circular connection, and stations 3 and 4 adopt radial connections.

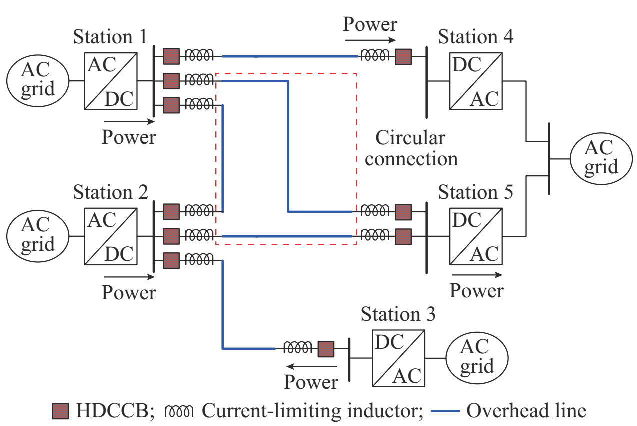

Fig. 4. Structure of five-terminal VSC-HVDC system.

For the stations in circular or meshed connection, power can still be transmitted by other lines even if one line is lost, and the converter stations are also connected together via the remaining DC lines. Therefore, the DC-side voltage of all converters will remain near the rated value.

However, in a radial connection, the converter at the end of the fault line will be isolated from the whole network. The station isolated from the network will lose the control of DC voltage if it is in the active power control mode, similar to a two-terminal system. Therefore, station 3 will appear overvoltage after line 3-2 is lost if it is in the active power control mode. On the contrary, there will be an undervoltage at station 4 after line 1-4 is lost if station 4 controls the active power. In principle, only one station controls the DC voltage, and the other stations control the active power in a VSC-MTDC system [30].

III. Soft Reclosing Scheme

The control principles of HDCCBs during the reclosing process are described in this section. A method for selecting which terminal to reclose first is investigated to achieve a minimum reclosing current during the O-C-O process. Converters are not blocked during the fault isolation and reclosing processes.

A. Control Principles for Reclosing Process

Figure 5 shows the current variation and control principles of HDCCBs during the reclosing process.

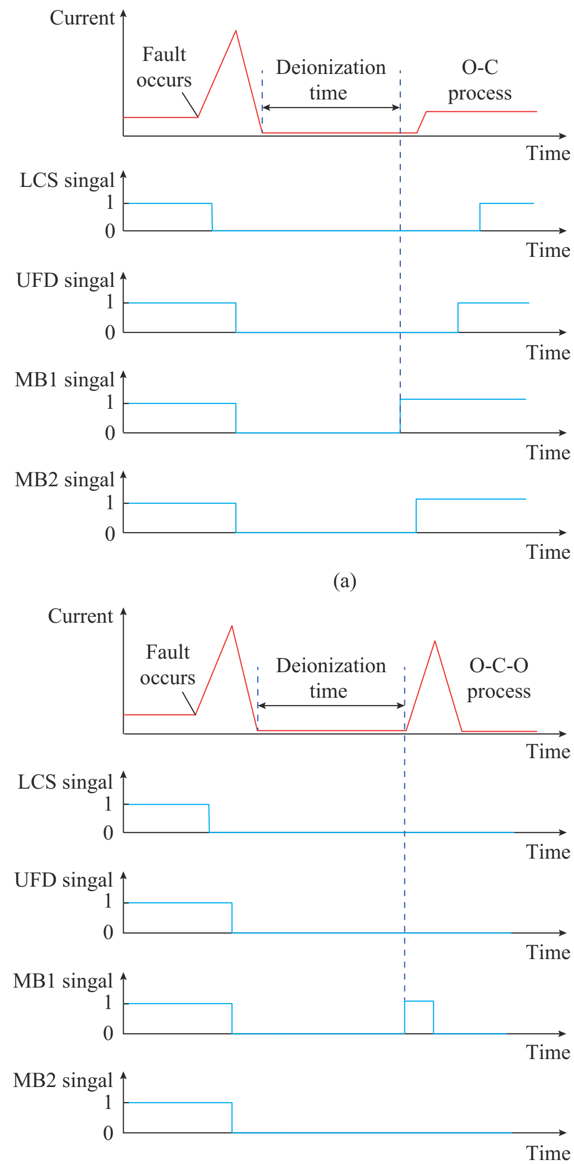

Fig. 5. Current variation and control principles of HDCCBs during reclosing process. (a) O-C process. (b) O-C-O process.

After waiting for the deionization time in Fig. 5(a), one terminal will attempt to reclose the line first, and the reclosing process is triggered by closing MB1 of this terminal.

The open-close (O-C) process occurs when a fault has been cleared, MB2 at another terminal is closed for fast restarting, and the LCS and UFD of both ends are closed after the system is stable. Then, current is transferred to the main branch. If the fault still exists, the converter will be connected to the fault again, and the current will rapidly increase. As shown in Fig. 5(b), MB1 will be triggered to open immediately, and the DC system will undergo an O-C-O process. The main purpose of this study is to limit the peak value of O-C-O overcurrent to reduce the impact of the O-C-O process.

B. Method for Selecting Which Terminal to Reclose First

A method for calculating the O-C-O current is presented in this subsection, along with the equivalent model of a modular multilevel converter (MMC). On the basis of the calculated O-C-O current, the terminal that will reclose with a smaller reclosing current is chosen as the terminal to reclose first.

The reclosing current is mainly caused by submodule (SM) capacitor discharging during the first 5 ms of the reclosing process [31]. An equivalent model for an MMC is shown in Fig. 6, where U_N is the normal operation voltage; R_0 and L_0 are the equivalent resistance and inductance of the bridge arm, respectively; and R_c, L_c, and C_c are the equivalent circuit parameters, which can be obtained by:

$$\begin{cases} R_c = \dfrac{2(R_0+R_{on})}{3} \\ L_c = \dfrac{2L_0}{3} \\ C_c = \dfrac{6C_0}{N_{SM}} \end{cases} \tag{3}$$

where R_{on} is the on-state resistance of all SMs; N_{SM} is the number of SMs in each arm; and C_0 is the capacitance of SM.

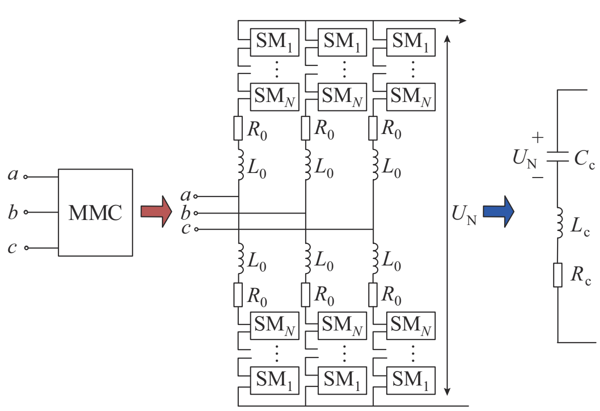

Fig. 6. Equivalent model for an MMC.

As shown in Fig. 7, a second-order differential equation for the reclosing current i_r can be written as (4) according to Kirchhoff's voltage law (KVL).

$$(2L_L+2L_l+L_c)C_c\frac{d^2 i_r}{dt^2}+(2R_l+R_c+R_f+R_s)C_c\frac{di_r}{dt}+i_r=0 \tag{4}$$

where L_l and R_l are the line inductance and resistance, respectively; L_L is the current-limiting inductance; and R_f is the equivalent fault resistance.

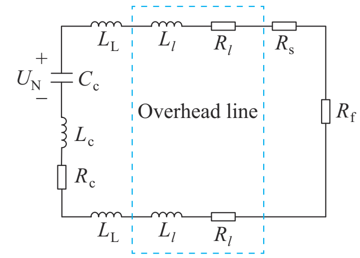

Fig. 7. Equivalent circuit for reclosing when fault still exists.

The boundary condition is given as:

$$\begin{cases} i_r\big|_{t=0}=0 \\ \dfrac{di_r}{dt}\Big|_{t=0} = \dfrac{U_N}{L_c+2L_L+2L_l} \end{cases} \tag{5}$$

The line inductance and resistance and the DC voltages will be different for the two terminals of the faulty line if the fault does not occur at the middle of the faulty line.

The adoption of a method for precalculating the reclosing current in order to choose a terminal to reclose with a smaller overcurrent can effectively limit the overcurrent during the O-C-O process. Note that this method for calculating the reclosing current can be adapted to a VSC-MTDC system. The detailed calculation process for a VSC-MTDC system can be found in [31], [32].

C. Energy Dissipation Stress of MOV

The MB in the HDCCB will be triggered to open once the existence of a fault is determined; then, the energy stored in the DC system will be dissipated through the MOV. The equivalent circuit during the energy dissipation process is shown in Fig. 8, where U_{MOV} is the protective voltage of the MOV; I_{max} is the peak value of the reclosing current; and U_c is the voltage of the converter capacitor after the MB of the HDCCB is disconnected.

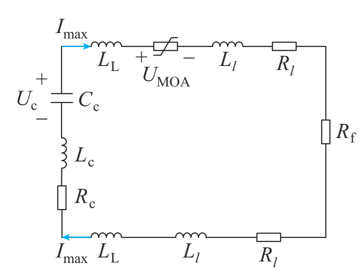

Fig. 8. Equivalent circuit during energy dissipation process.

From Fig. 8, the equation for calculating the residual current i_{MOV} during the energy dissipation process is shown in (6), and the solution for the current is expressed in (7). Thus, the energy dissipated through the MOV (E_{MOV}) can be calculated using (8), where $R = R_c + 2R_l + R_f$ and $L = L_c + 2L_L + 2L_l$.

$$\begin{cases} L\dfrac{\mathrm{d}i_{\mathrm{MOV}}}{\mathrm{d}t}+i_{\mathrm{MOV}}R+U_{\mathrm{MOV}}=U_{\mathrm{c}} \\ i_{\mathrm{MOV}}\big|_{t=0}=I_{\max} \end{cases} \tag{6}$$

$$i_{\mathrm{MOV}}=\frac{1}{R}\left[U_{\mathrm{c}}-U_{\mathrm{MOV}}-(U_{\mathrm{c}}-U_{\mathrm{MOV}}-I_{\max}R)\mathrm{e}^{-Rt/L}\right] \tag{7}$$

$$E_{\mathrm{MOV}}=\int U_{\mathrm{MOV}}i_{\mathrm{MOV}}\mathrm{d}t \tag{8}$$

Considering that the MOV may break apart if it is overloaded, the proposed method for selecting which terminal to reclose first can choose a terminal to reclose with the minimum $I_{\max}$ during the O-C-O process to reduce the energy dissipation stress of the MOV.

IV. Reclosing Process of Improved HDCCB with SRM

Owing to the small impedance of the DC system, an overcurrent still exists during the O-C-O process even though the method for selecting the terminal to reclose first is applied. Therefore, to limit the overcurrent thoroughly during the O-C-O process, when the HDCCB begins to reclose, the mechanical switch S will be opened, the MB will be closed, and the current will flow through the resistor R_s and MB. The topology of the improved HDCCB during reclosing is shown in Fig. 9. As the equivalent impedance of the commutation branch increases, the overcurrent during the reclosing process is limited even though the fault is permanent.

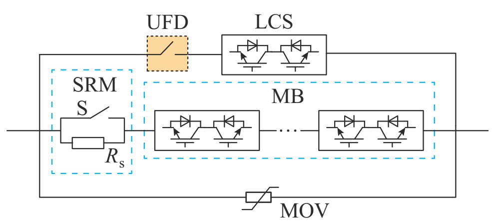

Fig. 9. Topology of improved HDCCB during reclosing.

Because the reclosing current needs to be less than the normal operating current but cannot be too small to affect the detection of the line fault, R_s is selected as:

$$R_{\mathrm{s}}=\frac{U_{\mathrm{N}}}{\alpha I_{\mathrm{N}}}-R_{\mathrm{f}}-R_{l} \tag{9}$$

where I_N is the normal operating current; and α is the safety factor in the range of 0.5-1.0.

On the basis of the method proposed in Section III, the terminal selected to reclose first is named T1, and the other terminal is named T2 in this paper. Figure 10 shows an equivalent circuit diagram of the system before reclosing.

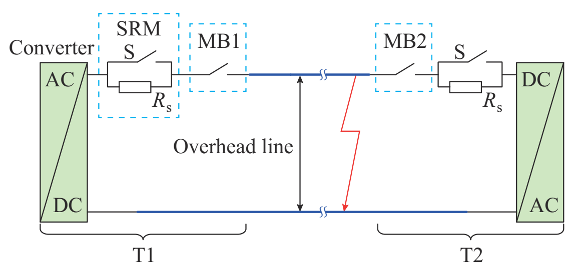

Fig. 10. Equivalent circuit diagram of system before reclosing.

A. Opening Process

In this process, S is always closed when using the improved HDCCB. There is no difference between the traditional and improved HDCCBs for the operation procedure during the opening process.

B. Reclosing Process

The operation procedure for the reclosing process when using improved HDCCBs is shown in Fig. 11, where $N_{\max}$ is the maximum number of reclosing times.

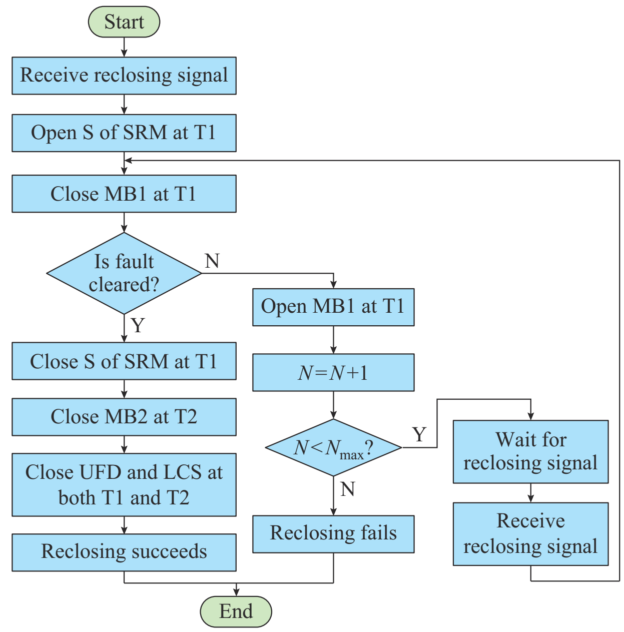

Fig. 11. Operation procedure for reclosing process when using improved HDCCBs.

The O-C-O process in a traditional solution may cause damage to the DC system again and greatly increase the energy dissipated through the MOV. However, the energy dissipation stress of the MOV in the improved HDCCB will not be increased because the reclosing current during the O-C-O process is greatly limited. R_s will be bypassed during the O-C process if the fault is cleared; therefore, the restart of the system will not be affected in this improved solution. Moreover, the control systems of the converters are not changed, and there is no need to restart the control system after successful reclosing of the HDCCB. Thus, the recovery time will be relatively shortened.

The total energy dissipated through R_s (E_R) can be calculated as:

$$E_{\mathrm{R}}=\frac{U_{\mathrm{N}}^{2}}{R_{\mathrm{s}}}\Delta t_{\mathrm{r}}N_{\max} \tag{10}$$

where Δt_r is the time needed to determine whether the fault is cleared during the reclosing process

As shown in (10), the energy dissipated through R_s during the O-C-O process is determined by the resistance and DC system voltage. Therefore, the design limit for $N_{\max}$ is limited by the resistance and energy-dissipating ability of the chosen resistor.

A faulty line voltage is chosen as the fault feature in this study. If the fault has already been cleared before the reclosing process, the voltage of the faulty line will increase to the rated value of the DC system. If the voltage of the faulty line fails to recover after the last attempt, the fault is considered to be permanent.

V. Simulation Results

To verify the effectiveness of the proposed soft reclosing scheme and improved HDCCB, simulations of both two-termainal and five-terminal VSC-HVDC systems are carried out using PSCAD/EMTDC.

A. Two-terminal VSC-HVDC System

Figure 12 shows the topology of a two-terminal VSC-HVDC system, where station 1 controls the active power and station 2 controls the DC voltage. The parameters of the DC system and control system are listed in Tables I and II, respectively.

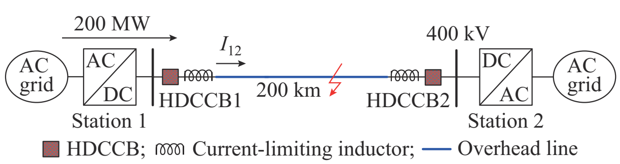

Fig. 12. Topology of two-terminal VSC-HVDC system.

TABLE I
Parameters of DC System

Parameter	Value
Rated DC voltage (kV)	400
Protective voltage of MOV (kV)	780
Upper limit of converter voltage (kV)	450
Lower limit of converter voltage (kV)	350
Number of SMs in each arm N_{SM}	250
Arm inductance (mH)	29
On-state resistance of each SM (mΩ)	0.908
Current-limiting inductance (mH)	50
Resistance of overhead line (Ω/km)	0.015
Inductance of overhead line (mH/km)	0.82

TABLE II
Parameters of Control System

Parameter	Value
Upper boundary of voltage limiter $U_{d,max}$ (p.u.)	1.05
Lower boundary of voltage limiter $U_{d,min}$ (p.u.)	0.95
Upper limit of PI controller output PI_{max} (p.u.)	1.1
Lower limit of PI controller output PI_{min} (p.u.)	−1.1
Protection coefficient of voltage limiter K_{dlim} (p.u.)	14

1) Impact of Control System

In the simulation, a permanent pole-to-pole short-circuit fault occurs at the middle of DC line at 1.0 s. Then, the two HDDCBs at both ends detect the fault and disconnect to interrupt the fault current at 1.005 s. Figure 13 shows the output of the control system and the converter voltage of station 1 after fault isolation. Consistent with the theoretical analysis in Section II, the control system will continue working and deliver a positive reference current I_{ref} to the inner-loop current controller after the DC fault current is interrupted. Thus, the AC system will follow this positive reference current and deliver active power P_{AC} to the converter. The converter will thus be charged, and the voltage will keep increasing and activate the voltage limiter, as shown in Fig. 13. After the voltage limiter is activated, it limits the converter voltage to its maximum value. The maximum converter voltage of station 1 is 1.129 p.u., which is exactly the same as the theoretical value calculated using (2).

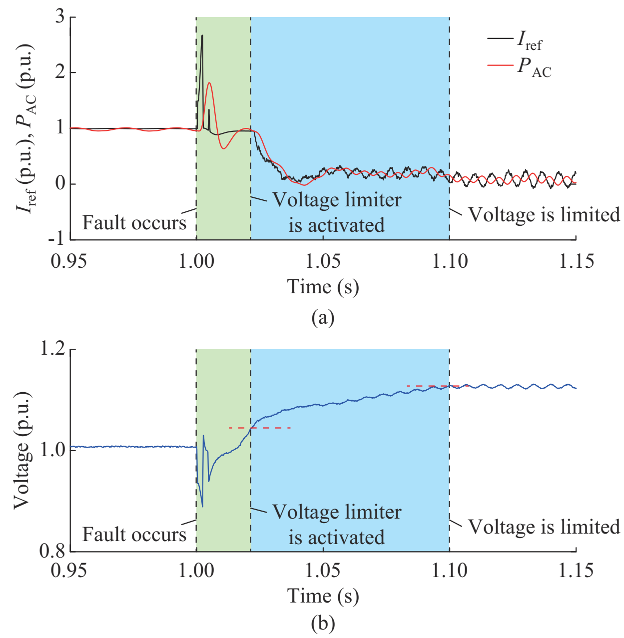

Fig. 13. Output of control system and converter voltage of station 1 after fault isolation. (a) Output of control system. (b) Converter voltage.

2) Impact of Disconnection of HDCCB

After waiting for the deionization time, HDCCB1 recloses at 1.3 s. Figure 14 shows the reclosing currents from the theoretical calculation and simulation during the reclosing process.

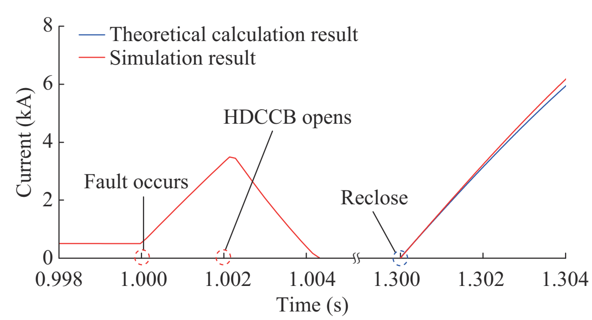

Fig. 14. Reclosing currents from theoretical calculation and simulation during reclosing process.

It can be observed in Fig. 14 that the proposed method for calculating the O-C-O current is sufficiently accurate during the first 5 ms. Considering that the time needed to identify the existence of a fault is approximately 2 ms, the error is almost negligible.

Simulations are carried out under multiple conditions at different fault locations to verify the effectiveness of the proposed method for selecting which terminal to reclose first. The value of the fault location, which ranges from 0 to 1, represents the distance between the fault location and station 1 after normalization. If the value of the fault location is equal to 0.5, the fault occurs at the middle of the DC line. Figure 15 shows the current during the O-C-O process when selecting a different terminal to reclose first. It can be observed that the current will be different when changing different terminals that reclose first. Even when a fault occurs at the middle of the DC line, the reclosing currents of the two terminals are different.

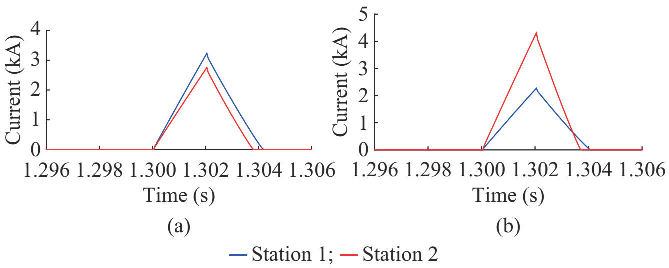

Fig. 15. Currents for different reclosing terminals during O-C-O process. (a) Value of fault location is 0.5. (b) Value of fault location is 0.83.

As stated before, the method for selecting which terminal to reclose first aims to achieve a minimum peak current during the O-C-O process. Figure 16 shows the simulation results I_{rS} and theoretical calculation results I_{rT} of the peak current during the O-C-O process when the fault location changes and different terminals are reclosed. These results show that the proposed method is accurate and sufficiently efficient to choose an appropriate terminal to reclose with a smaller overcurrent.

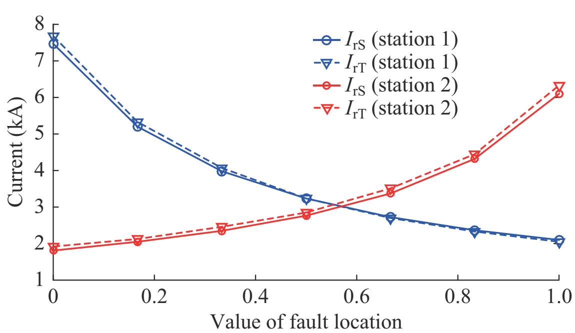

Fig. 16. Simulation and theoretical calculation results of peak current during O-C-O process when fault location changes and different terminals are reclosed.

3) *Soft Reclosing Module*

From the simulation results above, it can be observed that an overcurrent still exists during the O-C-O process even when the proposed method is adopted. To limit the overcurrent thoroughly during the O-C-O process, the improved HDCCB with an SRM is applied to the two-terminal system. R_s of the SRM is chosen as 1500 Ω ($\alpha=0.67$), and N_{max} is 3 in this simulation work.

Figure 17 shows the change in the fault current during the opening process of traditional and improved HDCCBs. As shown in Fig. 17, the opening process of the HDCCB will not be affected by the addition of the SRM to the HDCCB. Figure 18 shows a comparison of currents during the O-C-O process of the traditional and improved HDCCBs. The results show that the unwanted overcurrent during the O-C-O process is effectively limited when applying the improved HDCCB.

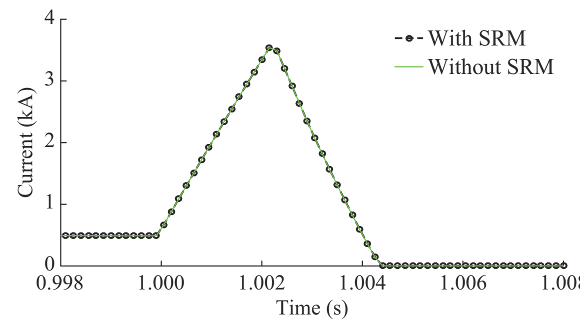

Fig. 17. Change in fault current during opening process of traditional and improved HDCCBs.

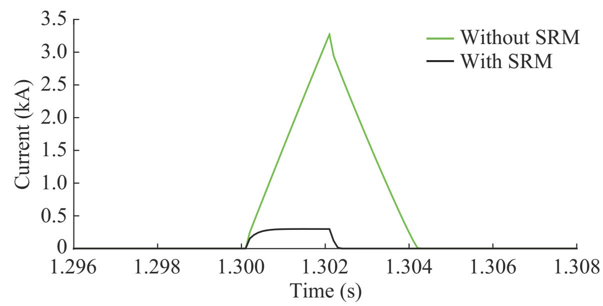

Fig. 18. Currents during O-C-O process of traditional and improved HDCCBs.

Figure 19 shows the energy dissipation stress of the MOV in the traditional and improved HDCCBs.

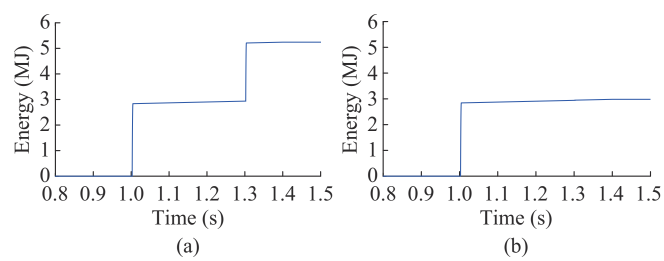

Fig. 19. Energy dissipation stress of MOV in traditional and improved HDCCBs. (a) Traditional HDCCB. (b) Improved HDCCB.

It can be observed from Fig. 19(a) that the energy dissipation stress of the MOV is increased by about 2.21 MJ during the O-C-O process for the traditional HDCCB. By using the theoretical analysis in Section III, the energy dissipated through the MOV should be increased by approximately 2.17 MJ, and the error is acceptable. As shown in Fig. 19(b), the energy dissipation stress of the MOV is hardly increased. According to Fig. 18 and the parameters of the simulation system used in this study, an energy of approximately 0.21 MJ is dissipated through R_s during the entire reclosing process for the improved HDCCB.

To prevent overloading of the MOV, reclosing the traditional HDCCB multiple times is not recommended, as the energy dissipation stress of the MOV will be increased by 73.6% during each O-C-O process. However, the improved HDCCB is capable of reclosing more than once because both the theoretical calculation and simulation results show that the MOV will not be overloaded and the energy consumed in R_s is acceptable during the O-C-O process.

Moreover, the impact of the O-C-O process on the AC system of the traditional and improved HDCCBs is compared in Fig. 20. As can be observed, the impact of the O-C-O process on the AC system, which occurs at 1.3 s, is greatly decreased for the improved HDCCB.

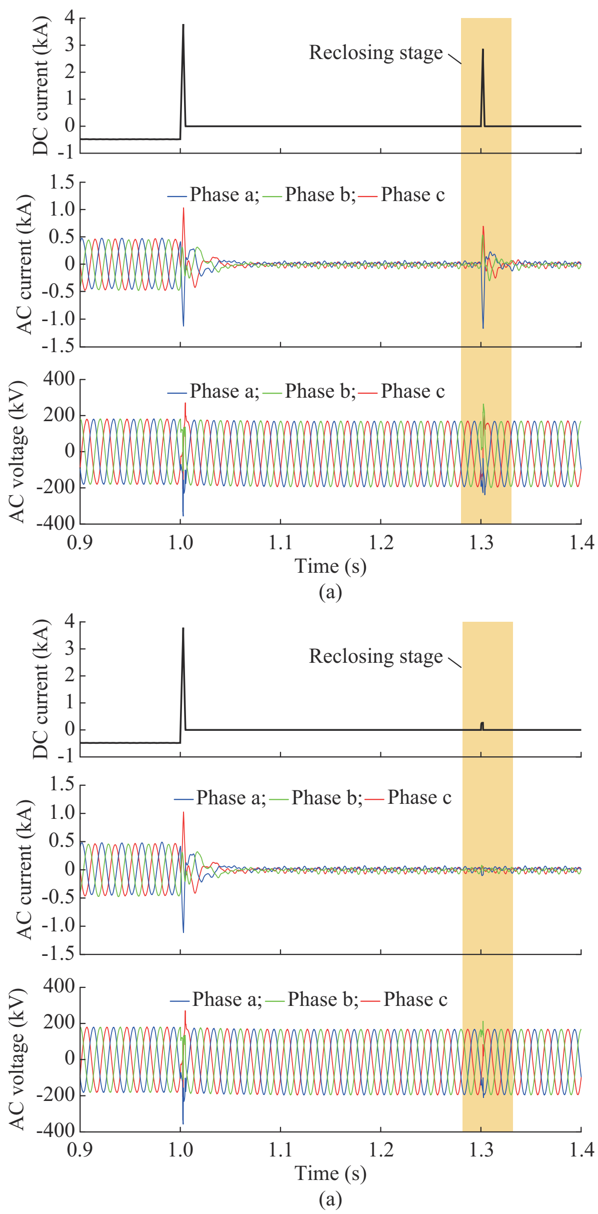

Fig. 20. Impact of O-C-O process on AC system of traditional and improved HDCCBs. (a) Traditional HDCCB. (b) Improved HDCCB.

B. Multi-terminal System

Figure 21 shows the topology of a five-terminal VSC-HVDC system with system parameters such as the rated power and DC line length. Station 5 controls the DC voltage, and all other stations are in the active power control mode.

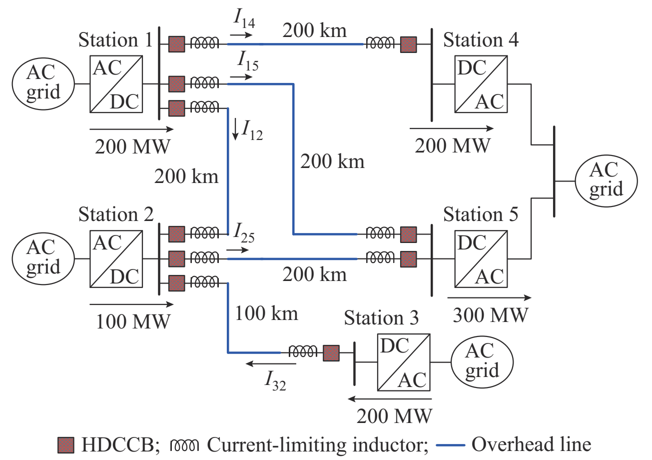

Fig. 21. Topology of five-terminal VSC-HVDC system with system parameters.

Figure 22 shows the DC voltages of stations 1 and 4 when a temporary fault is applied to the middle of line 1-4 at 1.0 s and the protection system successfully isolates the fault at 1.005 s. Consistent with the theoretical analysis in Section III, undervoltage occurs in station 4 after fault isolation. The converter voltage is 0.87 p.u., which is exactly the same as the theoretical value calculated from (2).

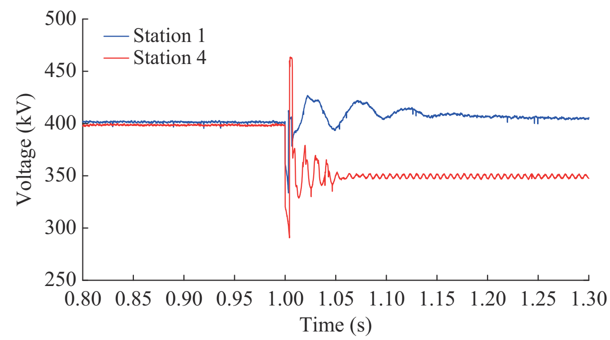

Fig. 22. DC voltages of stations 1 and 4.

The main objective of the improved HDCCB is to limit the overcurrent if the fault is not cleared, thus eliminating the impact of the O-C-O process. Figures 23 and 24 show comparisons of the overcurrent and power disturbances of the traditional and improved HDCCBs when a permanent fault occurs at the middle of line 2-5 and the system recloses at 1.3 s after fault isolation. As shown in Fig. 23, the reclosing current during the O-C-O process for the improved HDCCB is much smaller compared with that of the traditional HDCCB. The power disturbance during the O-C-O process when using a traditional HDCCB is 656.7 MW, as shown in Fig. 24. However, it decreases to 30.5 MW after adopting the improved HDCCB. It is obvious that the overcurrent and power disturbance during the O-C-O process are significantly reduced by adopting the improved HDCCB; thus, the DC system is able to reclose multiple times safely. Figure 24 shows that the HDCCB recloses during the fault twice and recloses successfully on the third attempt.

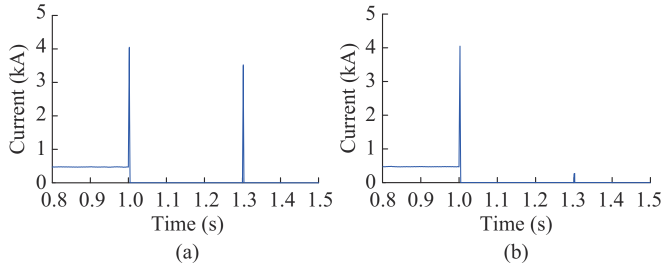

Fig. 23. Comparison of overcurrents of traditional and improved HDCCBs during O-C-O process. **(a)** Traditional HDCCB. **(b)** Improved HDCCB.

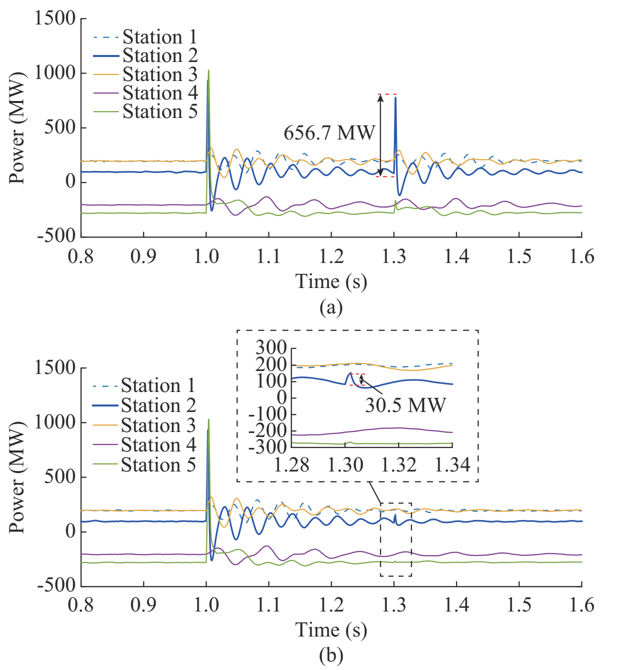

Fig. 24. Comparison of power disturbances of traditional and improved HDCCBs during O-C-O process. (a) Traditional HDCCB. (b) Improved HDCCB.

The sequential autoreclosing method proposed in [26] can limit the reclosing current during the O-C-O process. However, by applying a sequential autoreclosing method, the control systems of converters are changed before reclosing and need to be restarted. Thus, the recovery time after successful reclosing of the HDCCB is much longer than that of the proposed method, as shown in Figs. 25 and 26. Moreover, the sequential autoreclosing method proposed in [26] uses an MOV to limit the reclosing current, which will increase the energy dissipation stress of the MOV by approximately 24.5% during each O-C-O process. However, as discussed above, the energy dissipation stress of the MOV will not be increased using the proposed method.

VI. Conclusion

In this study, a reclosing process for permanent faults is investigated. When reclosing a permanent fault, the peak current differs in the fault location. The proposed method for selecting which terminal to reclose first can accurately choose an appropriate terminal to reclose to restrain the overcurrent during the O-C-O process.

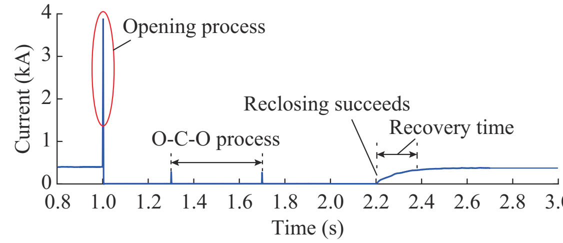

Fig. 25. Reclosing process applying proposed method.

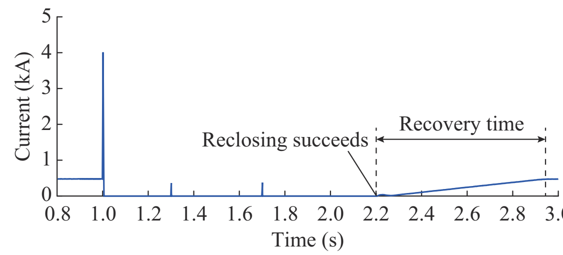

Fig. 26. Reclosing process applying method proposed in [26].

To thoroughly limit the overcurrent during the O-C-O process, the traditional HDCCB is improved by adding an SRM. The improved scheme and model proposed in this paper have the following advantages: ① the normal operation of the HDCCB will not be affected; ② the overcurrent and power disturbances during the reclosing process can be thoroughly limited; ③ the energy dissipation stress of the MOV will be reduced, which can mitigate the design and manufacturing difficulties of the MOV; ④ the impact of the reclosing process on the AC system is decreased; ⑤ the HDCCB is capable of reclosing multiple times safely; and ⑥ the recovery time after successful reclosing of the HDCCB is very short.

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