Improved Coordinated Control Approach for Evolved CCC-HVDC System to Enhance Mitigation Effect of Commutation Failure

Chunyi Guo, Bo Liu, and Chengyong Zhao

***Abstract*—The evolved capacitor commutated converter (ECCC), embedded with anti-parallel thyristors based dual-directional full-bridge modules (APT-DFBMs), can effectively reduce commutation failure (CF) risks of line-commutated converter-based high voltage direct current (HVDC) and improve the dynamic responses of capacitor-commutated converter-based HVDC. This paper proposes an improved coordinated control strategy for ECCC with the following improvements: ① under normal operation state, series-connected capacitors can accelerate the commutation process, thereby reducing the overlap angle and increasing the successful commutation margin; ② under AC fault conditions, the ability of ECCC to mitigate the CF issue no longer relies on the fast fault detection, since the capacitors inside the APT-DFBMs can consistently contribute to the commutation process and further reduce the CF probability; ③ the inserted capacitors can output certain amount of reactive power, increase the power factor, and reduce the required reactive power compensation capacity. Firstly, the proposed coordinated control approach is presented in detail, and the extra commutation voltage to mitigate the CFs provided by the proposed control approach and an existing approach is compared. Secondly, the mechanism of the improved control approach to accelerate commutation process and improve the power factor is analyzed theoretically. Finally, the detailed electromagnetic transient (EMT) simulation in PSCAD/EMTDC is conducted to validate the effectiveness of the proposed coordinated control. The results show that the proposed approach can present a further substantial improvement for ECCC, especially enhancing the CF mitigation effect.**

***Index Terms*—Evolved capacitor commutated converter (ECCC), coordinated control, commutation failure, power factor.**

I. Introduction

LINE commutated converter-based high voltage direct current (LCC-HVDC) transmission has been successfully applied in long-distance bulk-power transmission and asynchronous power grid interconnection. However, the LCC-HVDC technology has its inherent issues owing to the utilization of thyristors. The most common issue is the commutation failure (CF) occurring under voltage depression at inverter AC bus [1]-[3]. Moreover, with the increase of transmission distance, the ultra-high voltage direct current (UHVDC) systems with significantly large capacity are considered in the construction of particular projects [4], [5]. The growth in power transmission level increases the threats of CFs to the power grid, because the CFs can cause temporary suspension of transmission power, overheating of converter valves, and a sudden power shift to the adjacent high voltage alternate current (HVAC) lines [6]-[8].

By adding additional capacitive modules, a few enhanced converter topologies are proposed to mitigate CFs [1], [9]-[12]. Capacitor commutated converter (CCC), which is utilized in practical engineering, can offer an improved power factor and lower CF probability [9]. However, the capacitor voltage is usually uncontrollable during fault period, which may cause overvoltage and deteriorate the recovery performance. The controlled series capacitor converter (CSCC) is studied in [10]. Although the capacitor voltage can be adjusted by the embedded thyristor controlled series compensation (TCSC), the harmonic characteristics of the topology are complex, and there are resonance risks owing to the existence of inductors and capacitors in the CSCC scheme. In [11], an LCC-HVDC system with controllable capacitors is proposed. However, its application with larger power ratings, e.g., UHVDC systems, would be limited owing to the parameter mismatching of thyristor and insulated gate bipolar transistor (IGBT). The LCC system using thyristor-based controllable capacitors (TBCCs) with more complex control is studied in [12]. Nevertheless, better CF mitigation ability is obtained.

In [1], an evolved capacitor commutated converter (ECCC) embedded with anti-parallel thyristors based dual-directional full-bridge module (APT-DFBM) is presented. Under AC fault conditions, the charged capacitors can be inserted to provide an additional commutation-voltage support to mitigate the CF. As shown in [1], the ECCC-HVDC can effectively mitigate the CF risks compared with CCC-HVDC and LCC-HVDC schemes. Furthermore, through the change of APT-DFBM operation modes, the capacitor voltage can be limited to an allowable range, and the over-charging situa-

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C. Guo (corresponding author), B. Liu, and C. Zhao are with State Key Laboratory of Alternate Electrical Power System with Renewable Energy Sources (North China Electric Power University), Beijing, China (e-mail: chunyiguo@gmail.com; liubo_1995@126.com; chengyongzhao@ncepu.edu.cn).

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tion can be avoided even without surge arresters. Thus, the ECCC-HVDC can effectively mitigate the CF risks and improve the dynamic responses of the CCC-HVDC.

Although the ECCC performs well in CF suppression and fault recovery, it can still be further improved. With the original control approach in [1], the capacitor is bypassed when the system operates normally, and when the AC fault occurs, the capacitor is inserted to assist commutation process after a time delay of fault detection. In particular, the mitigation effect on CF of ECCC-HVDC is affected by the fault detection delay. Thus, it relies on the fast and accurate detection of AC faults. On one hand, the implementation of the accurate fault detection device will bring additional costs. On the other hand, if the required fault detection time is relatively long, the capacitor will not be able to provide auxiliary commutation support in time, and thus the mitigation effect of the CF will be significantly weakened.

According to the above analysis, it will have a great significance to eliminate the dependence of ECCC on the fast fault detection. To further reduce the CF risks and improve the system performance, based on the ECCC in [1], an improved coordinated control approach is proposed in this paper. During the normal operation and fault period, by coordinating the different working modes of APT-FBSMs, the following advantages can be achieved: ① under normal operation state, series-connected capacitors can accelerate the commutation process and increase the commutation margin successfully; ② under AC fault conditions, the ability of ECCC to mitigate CFs no longer relies on the fast fault detection because the capacitors of the APT-DFBMs can contribute to the commutation process; ③ the inserted capacitors can output certain amount of reactive power, increase power factor, and then reduce the required reactive power compensation capacity.

The remainder of this paper is organized as follows. In Section II, the ECCC topology and the operation principles of APT-DFBMs are described. In Section III, the improved coordinated control approach is proposed. The comparison between the added voltage-time commutation areas with original control approach and the proposed control approach is also conducted. In Section IV, the proposed control mechanism to accelerate the commutation process and improve the power factor is analyzed. In Section V, the effectiveness of the proposed coordinated control approach is investigated. Finally, conclusions are drawn in Section VI.

II. System Configuration & Operation Principles

A. ECCC Configuration

Figure 1(a) shows the ECCC topology in [1], where VT1-VT6 are thyristor valves; L_S is the reactor; and e_a, e_b and e_c are the valve-side phase voltages of the converter. Several APT-DFBMs are connected between the valve-side of the converter and the secondary side of the converter transformer. The structure of APT-DFBM is shown in Fig. 1(b), where four sets of dual-directional APTs are used to enhance the control flexibility of inserted capacitors and provide an additional voltage-time commutation area; C is a capacitor; u_c is the capacitor voltage; S termination is connected to the converter valve; and S' termination is connected to the converter transformer. Each thyristor element VTij ($i = 1, 2, 3, 4$ and $j = 1, 2$) can be composed of several series-connected thyristors.

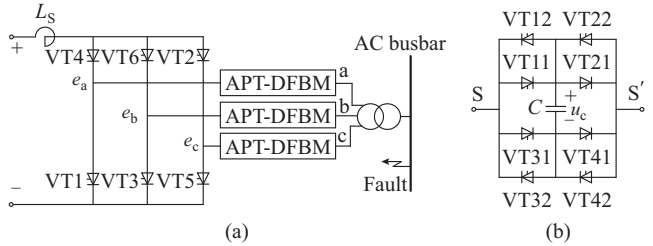

Fig. 1. ECCC topology. (a) ECCC configuration (6 pulses). (b) APT-DFBM.

B. Operation Modes of APT-DFBM

Figure 2 shows eight different working modes of APT-DFBM, where the dark portion represents the current flow path, and the arrow represents the current flow direction. When the APT-DFBM is working in modes 1-4, the capacitor is bypassed, and the capacitor is inserted in modes 5-8. The working mode of APT-DFBM depends on on-going or off-going period of the arm in each phase. Since modes 1 and 2, modes 3 and 4, modes 5 and 6, and modes 7 and 8 are mutually equivalent, this analysis takes modes 1, 3, 5 and 7 as examples.

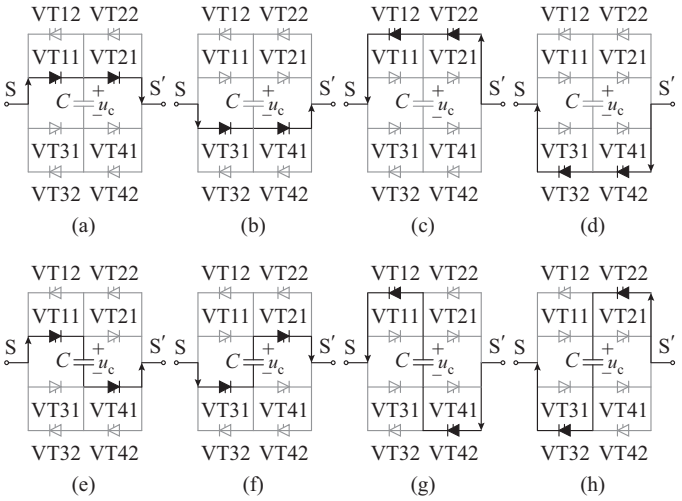

Fig. 2. Operation modes of APT-DFBM. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6. (g) Mode 7. (h) Mode 8.

III. Improved Coordinated Control Strategy for ECCC

This section analyzes the working principle and drawbacks of the original control approach of the ECCC in [1]. Then, an improved coordinated control approach is proposed to further reduce the probability of CFs and improve the system performances. The schematic diagram of the proposed improved coordinated control approach and the comparison with the original control approach is shown in Fig. 3.

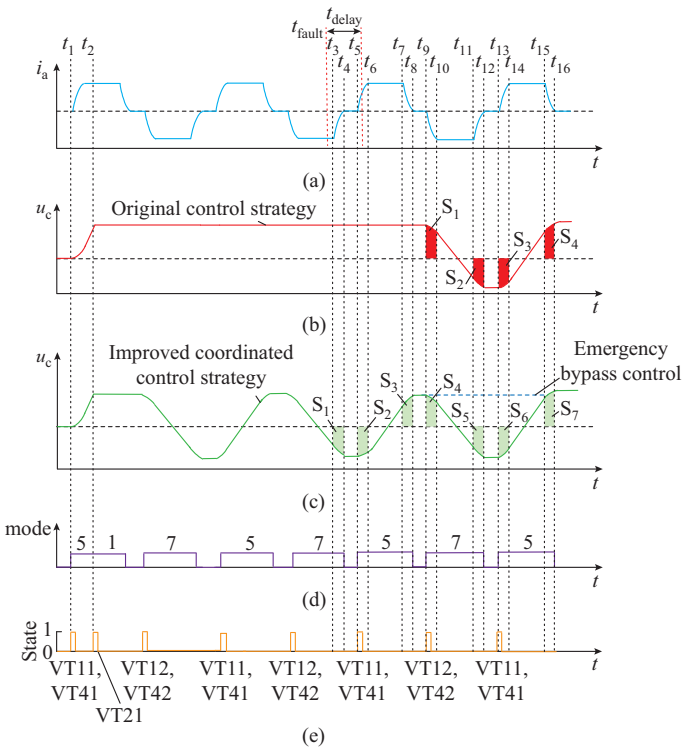

Fig. 3. Schematic diagram of proposed improved coordinated control approach in phase A. (a) AC current. (b) Capacitor voltage with original control approach. (c) Capacitor voltage with proposed improved coordinated control approach. (d) Operation mode. (e) State of VT*ij*.

A. Drawbacks of Original Control Strategy

For the original control approach of the ECCC, the capacitor of the APT-DFBM is bypassed under the steady-state condition. When a fault occurs, a capacitor is inserted to provide an additional voltage-time area to mitigate the CF. With the additional commutation voltage support provided by the APT-DFBMs, the successful commutation can be easily attained. Moreover, the ECCC has an emergency bypass control for self-protection. The capacitor voltage can be limited to an allowable range by the emergency bypass control, and the over-charging situation can be avoided even without the surge arresters. Therefore, the ECCC can effectively reduce the CF risks of LCC-HVDC, enhance the control flexibility, and thus improve the dynamic responses of CCC-HVDC.

Although the ECCC performs well in CF suppression and fault recovery, its performance can still be further improved. With the original control approach, the auxiliary commutation control is activated by a fault detection, thus the capacitor will be inserted after a delay time of fault detection.

Figure 3(a) takes phase A current i_a as an example, assuming that the fault occurs at $t=t_{fault}$ and is cleared at $t=t_{16}$. Figure 3(b) shows the capacitor voltage waveform with the original control approach. The reference direction of the capacitor voltage is shown in Fig. 2(a). During fault detection period, the capacitor is not yet inserted, thus the APT-DFBM cannot mitigate the CF during the delay time. After a while, as shown in Fig. 3(b), at $t=t_9$, VT1 will experience on-going period and VT5 will experience off-going period. The sub-module of phase A operates at mode 7, and it outputs a positive voltage and provides an extra voltage-time area S_1 (red shadow area in Fig. 3(b)) to accelerate the on-going process of VT1. Meanwhile, the APT-DFBM of phase C outputs a negative voltage to accelerate the off-going process of VT5. Similarly, additional voltage-time areas S_2-S_4 (red shadow areas in Fig. 3(b)) will be output sequentially by APT-DFBMs to assist commutation process and mitigate CF of the system.

From the above analysis, during the period of [t_{fault}, t_9], the ECCC cannot provide the additional voltage-time area to mitigate the CF in time. Therefore, with the original control approach, the mitigation effect on the CF is affected by the fault detection time. Supposing the required fault detection time is relatively long, the capacitors will not be able to provide auxiliary commutation support in time, and the mitigation effect of the CF will be greatly weakened to extent of not suppressing the CF.

B. Improved Coordinated Control Strategy

Based on the above analysis, an improved coordinated control approach is proposed. The main difference between the improved coordinated control approach and the original control approach in [1] is that the capacitors of the APT-DFBMs are inserted with the improved coordinated control approach under both normal operation and fault conditions.

Figure 3(c) shows the capacitor voltage waveform with the improved coordinated control approach. After $t=t_2$, the ECCC-HVDC operates under the steady-state condition. Under this condition, the APT-DFBM of phase A operates in mode 7 and mode 5 when the lower and upper arms of phase A are conducting, respectively. The capacitor experiences charging and discharging processes in cycles. With the improved coordinated control approach, the capacitor is inserted, which can enhance the commutation process, reduce the overlap angle, and increase the margin for successful commutation. Furthermore, the inserted capacitor can output reactive power, increase the power factor, and reduce the required reactive power compensation capacity.

Moreover, the improved coordinated control approach can further reduce the probability of CF compared with the original control approach. The comparison of capacitor voltage waveforms with the original and improved control strategies are shown in Fig. 3(b) and (c). With the improved coordinated control approach, as shown in Fig. 3(c), VT1 will experience off-going period at $t=t_3$. During this period, the APT-DFBM in phase A outputs a negative voltage and provides an extra voltage-time area S_1 (green shadow area in Fig. 3(c)) to accelerate the off-going process of VT1. At $t=t_5$, VT4 starts to experience on-going period, and the APT-DFBM of phase A outputs a negative voltage and provides an extra voltage-time area S_2 (green shadow area in Fig. 3 (c)) in mode 5 to accelerate the on-going process of VT4. Similarly, additional voltage-time areas S_3-S_7 (green shadow areas in Fig. 3(c)) will be output sequentially by APT-DFBMs to assist commutation process and mitigate the CF of the system. The detailed flow chart of the improved coordinated control approach is shown in Fig. 4. The emergency bypass control of the improved coordinated control approach is similar to that of the original control approach in [1].

Thus, the capacitor voltage can also be limited to an allowable range.

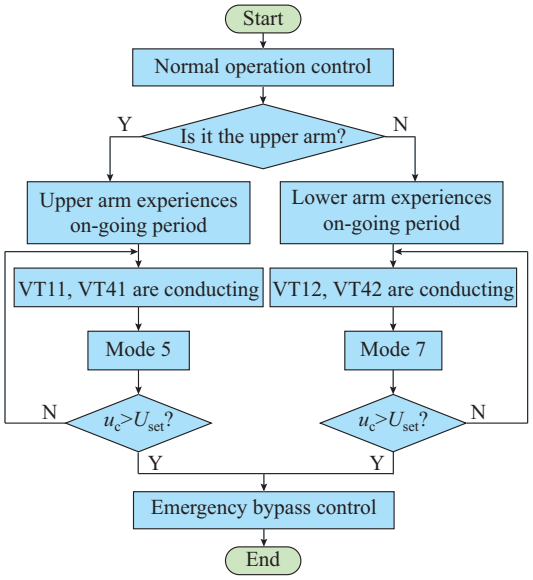

Fig. 4. Flow chart of improved coordinated control approach.

Note that the CF mitigation effect with the improved coordinated control approach is also related to the fault time, especially during the initial period after the fault occurs. For example, if the fault occurs when the capacitor is in the charging state and the capacitor voltage does not reach the maximum value, the provided extra voltage-time commutation area during this period will be limited and thus the inhibition on the CF may be weakened to some extent. More elaborations are provided in Section V.

From the comparison between Fig. 3(b) and (c), the additional voltage-time areas provided by the original control approach are S_1-S_4 (red shadow areas in Fig. 3(b)) and the areas provided by the proposed improved coordinated control approach are S_1-S_7 (green shadow areas in Fig. 3(c)). Thus, the improved coordinated control approach can provide more additional voltage-time commutation areas to mitigate CFs, especially during the initial period after the fault occurs. Therefore, the improved coordinated control approach can further reduce the CF probability.

IV. Theoretical Analysis of Proposed Control Strategy

This section analyzes the improved coordinated control approach from the theoretical aspects. The improved coordinated control approach has two major benefits. First, the series-connected capacitors can accelerate the commutation process, increase the margin for successful commutation and further reduce the probability of CF under both normal operation and fault conditions. Second, the inserted capacitors can output reactive power, increase the power factor, and reduce the reactive power compensation capacity.

A. Commutation Process Analysis to Further Mitigate CFs

With the original control approach, the capacitors are bypassed when the system operates normally. The commutation process of the ECCC-HVDC under steady-state condition is similar to that of the LCC-HVDC. Taking the commutation period from VT4 to VT6 as an example, the commutation process can be written as:

$$L_r\frac{di_6}{dt}-L_r\frac{di_4}{dt}=\sqrt{2}\,V_L\sin\omega t \tag{1}$$

$$i_6+i_4=I_d \tag{2}$$

where i_6 and i_4 are the currents flowing through VT6 and VT4, respectively; V_L is the root mean square (RMS) value of the commutation voltage; L_r is the commutation inductor; ω is the system angular frequency; and I_d is DC current.

With the initial condition $i_4(\alpha)=I_d$, i_4 can be obtained as:

$$i_4=I_d-\frac{V_L}{\sqrt{2}\,\omega L_r}(\cos\alpha-\cos\omega t) \tag{3}$$

where α is the firing angle.

When $\omega t=\alpha+\mu$, the commutation process terminates. By substituting i_4=0 into (3), the overlap angle μ with the original control approach can be obtained as:

$$\mu=-\alpha+\arccos\left(\cos\alpha-\frac{\sqrt{2}\,\omega L_r I_d}{V_L}\right) \tag{4}$$

With the proposed improved coordinated control approach, the capacitors are inserted. The equivalent commutation circuit from VT4 to VT6 is shown in Fig. 5, where u_{ca}, u_{cb} and u_{cc} are the capacitor voltages of the three phases, i_5 is the current flowing through VT5, and V_d is DC voltage.

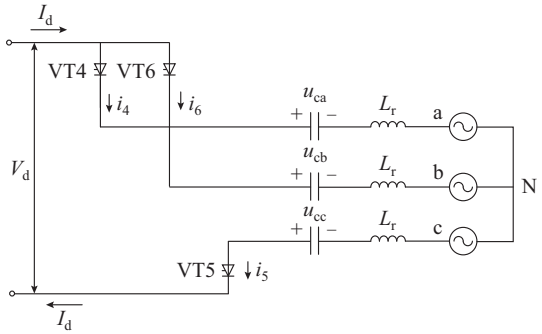

Fig. 5. Equivalent commutation circuit from VT4 to VT6.

During the normal operation period of the system, the instantaneous line-to-neutral source voltages are:

$$\begin{cases} e_a=E_m\cos\left(\omega t+\alpha+\dfrac{\pi}{3}\right) \\ e_b=E_m\cos\left(\omega t+\alpha-\dfrac{\pi}{3}\right) \\ e_c=E_m\cos(\omega t+\alpha-\pi) \end{cases} \tag{5}$$

where E_m is the phase voltage amplitude. The commutation loop of Fig. 5 can be written as:

$$i_4+i_6=i_5=I_d \tag{6}$$

$$i_4=C\frac{du_{ca}}{dt} \tag{7}$$

$$i_6=-C\frac{du_{cb}}{dt} \tag{8}$$

$$e_{\mathrm{b}}+L_{\mathrm{r}}\frac{\mathrm{d}i_6}{\mathrm{d}t}-u_{\mathrm{cb}}=e_{\mathrm{a}}+L_{\mathrm{r}}\frac{\mathrm{d}i_4}{\mathrm{d}t}+u_{\mathrm{ca}} \tag{9}$$

When t=0, the initial condition is:

$$C\frac{\mathrm{d}u_{\mathrm{ca}}}{\mathrm{d}t}\bigg|_{t=0}=I_{\mathrm{d}} \tag{10}$$

By solving (5)-(10), i_4 can be obtained as:

$$\begin{aligned}i_4=\frac{\omega C}{2}\Bigg[&\frac{-U_{\mathrm{cb}}(0)}{\sqrt{X_{\mathrm{r}}\omega C}}\sin\frac{\omega t}{\sqrt{X_{\mathrm{r}}\omega C}}-\frac{U_{\mathrm{ca}}(0)}{\sqrt{X_{\mathrm{r}}\omega C}}\sin\frac{\omega t}{\sqrt{X_{\mathrm{r}}\omega C}}+\\&\frac{I_{\mathrm{d}}}{\omega C}\left(\cos\frac{\omega t}{\sqrt{X_{\mathrm{r}}\omega C}}+1\right)-\sqrt{2}\,V_{\mathrm{L}}\left(\frac{-\sin\alpha}{\sqrt{X_{\mathrm{r}}\omega C}}\sin\frac{\omega t}{\sqrt{X_{\mathrm{r}}\omega C}}+\right.\\&\left.\cos\alpha\cos\frac{\omega t}{\sqrt{X_{\mathrm{r}}\omega C}}-\cos(\omega t+\alpha)\right)\frac{1}{X_{\mathrm{r}}\omega C-1}\Bigg]\end{aligned} \tag{11}$$

where X_{r} is the equivalent commutation reactor; and $U_{\mathrm{ca}}(0)$ and $U_{\mathrm{cb}}(0)$ are the initial charge voltages of the capacitors.

When $t=\mu/\omega$, the commutation process terminates. By substituting $i_4=0$ into (11), let $C_1=\mu/X_{\mathrm{r}}$, the relationship between the overlap angle μ and capacitor value C with the improved coordination control approach can be obtained as:

$$\begin{aligned}\mu=-\alpha+\arccos\Bigg\{&\frac{X_{\mathrm{r}}\omega C-1}{\sqrt{2}\,V_{\mathrm{L}}}\Bigg[\frac{U_{\mathrm{cb}}(0)}{\sqrt{X_{\mathrm{r}}\omega C}}\sin\frac{C_1\sqrt{X_{\mathrm{r}}}}{\sqrt{\omega C}}+\\&\frac{U_{\mathrm{ca}}(0)}{\sqrt{X_{\mathrm{r}}\omega C}}\sin\frac{C_1\sqrt{X_{\mathrm{r}}}}{\sqrt{\omega C}}-\frac{I_{\mathrm{d}}}{\omega C}\left(\cos\frac{C_1\sqrt{X_{\mathrm{r}}}}{\sqrt{\omega C}}+1\right)\Bigg]-\\&\frac{\sin\alpha}{\sqrt{X_{\mathrm{r}}\omega C}}\sin\frac{C_1\sqrt{X_{\mathrm{r}}}}{\sqrt{\omega C}}+\cos\alpha\cos\frac{C_1\sqrt{X_{\mathrm{r}}}}{\sqrt{\omega C}}\Bigg\}\end{aligned} \tag{12}$$

By comparing (12) and (4), it can be seen that the overlap angle μ can be reduced owing to the effect of the inserted capacitor C and capacitor voltage with the improved coordination control approach. Therefore, the inserted capacitor can accelerate the commutation process. Assuming that the advanced firing angle β is the same as that of original control approach, the extinction angle γ can be increased, and thus the successful commutation margin can be enlarged.

B. Analysis of Improving Power Factor

The increased capacitor voltage of VT4 during the on-going period is:

$$\Delta V=\frac{1}{C}\int_0^{\frac{\mu}{\omega}}\left(I_{\mathrm{d}}-i_4\right)\mathrm{d}t \tag{13}$$

The increased capacitor voltage of VT4 during the off-going period is:

$$\Delta V'=\frac{1}{C}\int_{\frac{2\pi}{3\omega}}^{\frac{2\pi}{3\omega}+\frac{\mu}{\omega}}i_4\,\mathrm{d}t \tag{14}$$

The DC voltage during the commutation period is:

$$V_{\mathrm{dcom}}=\frac{1}{2}\left(e_{\mathrm{a}}+u_{\mathrm{ca}}+e_{\mathrm{c}}+u_{\mathrm{cc}}\right)-\left(e_{\mathrm{b}}-u_{\mathrm{cb}}\right) \tag{15}$$

The DC voltage during the conductive period is:

$$V_{\mathrm{dcon}}=\left(e_{\mathrm{a}}+u_{\mathrm{ca}}\right)-\left(e_{\mathrm{b}}-u_{\mathrm{cb}}\right) \tag{16}$$

The average DC voltage over a cycle is:

$$V_{\mathrm{d}}=\frac{3}{\pi}\left(\int_0^{\frac{\mu}{\omega}}V_{\mathrm{dcom}}\,\mathrm{d}t+\int_{\frac{\mu}{\omega}}^{\frac{\pi}{3\omega}}V_{\mathrm{dcon}}\,\mathrm{d}t\right) \tag{17}$$

Thus, the DC voltage V_{d} can be obtained as:

$$V_{\mathrm{d}}=\frac{3\sqrt{3}\,E_{\mathrm{m}}}{\pi}\frac{\cos\alpha+\cos(\alpha+\mu)}{2}+\frac{\pi}{3}\left[(\Delta V'-\Delta V)\left(\frac{\pi}{3}-\frac{\mu}{4}\right)\right] \tag{18}$$

Assuming that the active power delivered by the DC system is equal to that delivered by the AC system, then

$$V_{\mathrm{d}}I_{\mathrm{d}}=\sqrt{3}\,V_{\mathrm{L}}I_{\mathrm{L1}}\cos\varphi \tag{19}$$

where I_{L1} is the RMS value of the fundamental frequency current, and $\cos\varphi$ is the power factor. I_{L1} can be written as:

$$I_{\mathrm{L1}}=\frac{\sqrt{6}}{\pi}I_{\mathrm{d}} \tag{20}$$

Finally, by substituting (18) and (20) into (19), the power factor can be calculated as:

$$\begin{aligned}\cos\varphi=\frac{\pi}{3\sqrt{2}\,V_{\mathrm{L}}}\Bigg[&\frac{3\sqrt{3}\,E_{\mathrm{m}}}{2\pi}\left(\cos\alpha+\cos(\alpha+\mu)\right)+\\&\frac{\pi}{3}(\Delta V'-\Delta V)\left(\frac{\pi}{3}-\frac{\mu}{4}\right)\Bigg]\end{aligned} \tag{21}$$

From (21), by inserting the capacitors, the overlap angle is reduced, and the power factor of the system is improved with the improved coordinated control approach. Moreover, the capacitors can output reactive power, thus reducing the reactive power compensation capacity required by the system.

V. Simulation Studies

A. Scenarios

In this subsection, the improved coordinated control approach is investigated by comparing the system performances in the following six scenarios.

Scenario 1: LCC-HVDC (CIGRE benchmark model).

Scenario 2: ECCC-HVDC, with the original control approach considering fault detection time $t_{\mathrm{fd}}=2$ ms.

Scenario 3: ECCC-HVDC, with the original control approach considering $t_{\mathrm{fd}}=3$ ms.

Scenario 4: ECCC-HVDC, with the original control approach considering $t_{\mathrm{fd}}=4$ ms.

Scenario 5: ECCC-HVDC, with the improved coordinated control approach.

Scenario 6: CCC-HVDC.

The parameters of scenario 1 [13] are shown in Table I. In scenarios 2-5, the HVDC systems adopt the ECCC configuration of Fig. 1 as inverters, and have the same rectifiers and DC links as those in scenario 1. The parameters of ECCC and the APT-DFBM in scenarios 2-5 are consistent with those in [1], where U_{set} is 22 kV and the capacitor size C is 400 μF in one APT-DFBM. Scenarios 2-4 adopt the original control approach with different values of fault detection time t_{fd}.

TABLE I
PARAMETERS OF LCC-HVDC SYSTEM

Location	AC system voltage (kV)	Direct voltage (kV)	Direct current (kA)	Transformer ratio	Leakage inductance (p.u.)
Rectifier side	345	505	2	345 kV/ 213.5 kV	0.18
Inverter side	230	495	2	230 kV/ 209.2 kV	0.18

B. Investigation of Improving Power Factor

When the systems operate normally, the results of the reactive power consumption and the overlap angle of inverter in scenarios 1-5 are measured and shown in Table II.

TABLE II
REACTIVE POWER CONSUMPTION AND OVERLAP ANGLE OF INVERTER

Scenario	Reactive power consumption (Mvar)	Overlap angle (°)
Scenario 1	547	22.99
Scenarios 2-4	550	22.99
Scenario 5	516	19.78

As shown in Table II, compared with scenarios 1-4, scenario 5 has the minimum reactive power consumption. With the improved coordinated control approach, the capacitor can output certain reactive power at nominal operation state, which can increase the power factor and reduce the capacity of the reactive power compensators. However, in scenarios 2-4, the capacitors are bypassed under normal operation state, and cannot output reactive power. Thus, more reactive power compensators are required. Therefore, the improved coordinated control approach can improve the power factor of the system and reduce the reactive power consumption of the converter. In addition, the overlap angle of scenario 5 is the smallest compared with scenarios 1-4. With the improved coordinated control approach, the capacitor directly participates in commutation process, which can accelerate the commutation process, reduce the overlap angle and increase the margin for successful commutation. However, in scenarios 2-4, the commutation process and overlap angle are similar to the LCC-HVDC owing to the capacitor not inserted under the normal operation. Therefore, the proposed method can reduce overlap angle and increase the commutation margin, thus, increasing power factor and reducing the reactive power compensation.

C. Investigation of CF Mitigation in Single-infeed HVDC System

1) Single-phase-to-ground Fault

1) Dynamic performance comparison

In this subsection, the transient performances under fault conditions and the ability of the proposed method to mitigate the CF are investigated. The simulation results are provided in 2 cases.

Case 1: a minor fault occurs in the AC system (single-phase-to-ground fault with 0.55 H inductance).

This fault with 0.55 H inductance occurs at t=2.0 s and continues for 50 ms. The dynamic performances in scenarios 1, 2, 5 and 6 are shown in Fig. 6.

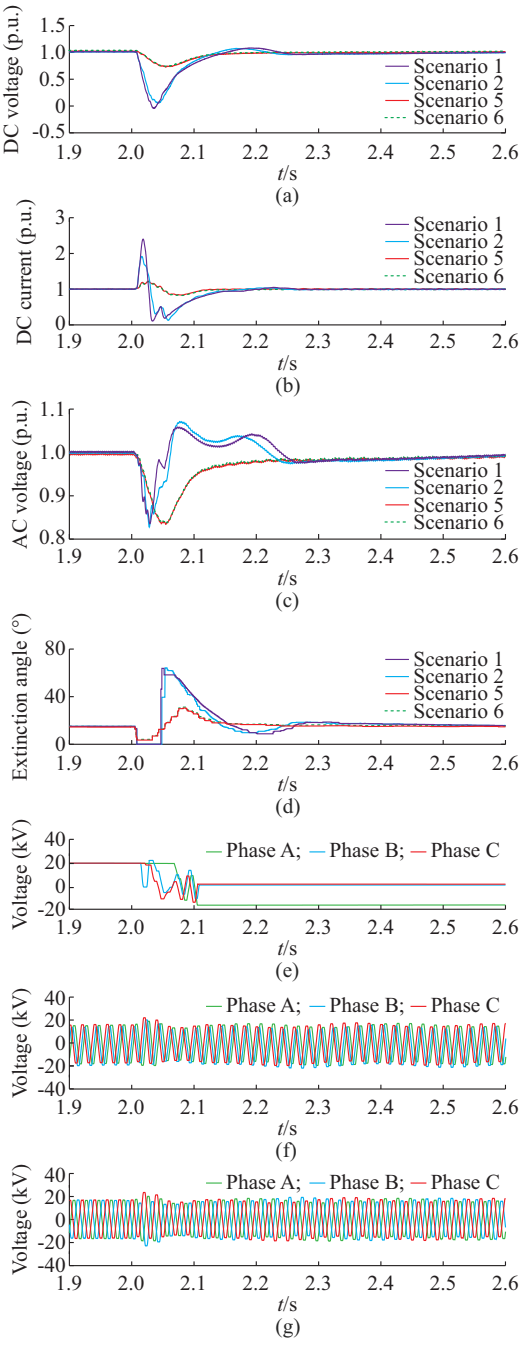

Fig. 6. Transient response comparison in Case 1. (a) DC voltage. (b) DC current. (c) AC voltage. (d) Extinction angle. (e) Capacitor voltage of scenario 2. (f) Capacitor voltage of scenario 5. (g) Capacitor voltage of scenario 6.

In Fig. 6, the LCC inverters in scenarios 1 and 2 experience CFs after the fault occurs. However, the LCC inverters in scenarios 5 and 6 mitigate the CFs successfully. In Fig. 6(a), the DC voltages in scenarios 1 and 2 drop to 0 and 0.1 p.u., respectively, while those in scenarios 5 and 6 drop to 0.75 p.u.. In Fig. 6(b), the DC currents in scenarios 1 and 2 rise to 2.5 p.u. and 1.9 p.u., respectively, while those in scenarios 5 and 6 rise to 1.2 p.u.. From Fig. 6(e) to (g), the maximum capacitor voltages in scenarios 2, 5 and 6 are all approximately 20 kV, and there are no overvoltage issues. Therefore, under a minor fault condition, the utilization of the proposed im-

proved coordinated control approach can suppress CF, accelerate the recovery process and improve the dynamic performances under the given fault conditions. Simultaneously, the capacitor voltage can be limited within the suitable range with the improved coordination control approach.

Case 2: a serious fault occurs in the AC system (solid single-phase-to-ground fault).

This fault occurs at $t=2.0$ s and continues for 50 ms. The dynamic performances under scenarios 1, 2, 5 and 6 are shown in Fig. 7.

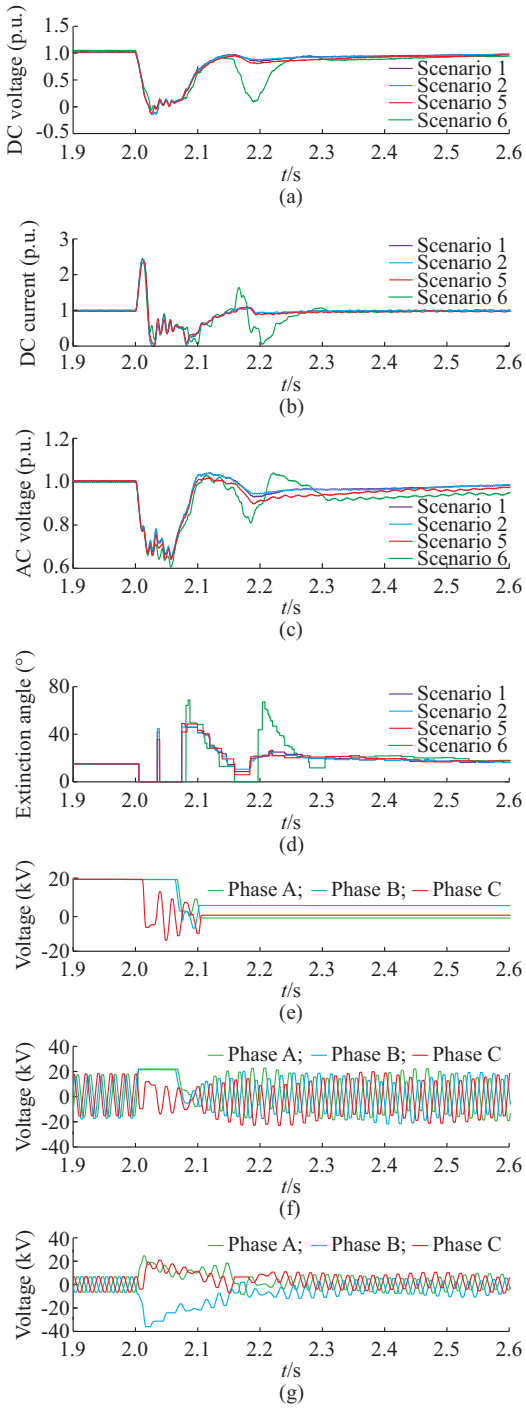

Fig. 7. Transient response comparison in Case 2. (a) DC voltage. (b) DC current. (c) AC voltage. (d) Extinction angle. (e) Capacitor voltage of scenario 2. (f) Capacitor voltage of scenario 5. (g) Capacitor voltage of scenario 6.

In Fig. 7, all four HVDC links experience CFs when a significantly severe fault occurs. After the fault is cleared, scenarios 1, 2 and 5 can be successfully restored to the normal operation state. However, scenario 6 experiences CF again at $t=2.15$ s. As for scenario 6, the capacitors experience uncontrolled charging and discharging processes, and the maximum voltage of the capacitor is 80 kV, which is likely to damage the capacitor. For scenario 5, the emergency bypass control is activated and the maximum capacitor voltage is close to an acceptable value of 20 kV from Fig. 3(e). Under the solid single-phase-to-ground fault, the capacitor voltage of CCC-HVDC is uncontrollable during the fault recovery progress, which causes overvoltage and deteriorates the recovery performance. However, with the proposed approach, the capacitor of APT-DFBMs can be flexibly controlled, and the capacitor will be bypassed after CF occurs, thus ensuring that overvoltage does not occur, and avoiding adverse effects on the recovery process of the system. Therefore, compared with CCC, the ECCC adopting the improved coordinated control approach retains the ability to resist CF, avoids overvoltage of capacitor, and has a good fault recovery ability.

2) CF probability comparison

To further investigate the effects of the proposed control approach, the CF probabilities [20] of five scenarios are studied. The CF probability of a given fault is calculated as the fraction of faults that result in CF of a certain amount N_{total} applied at different points on wave within a cycle. In this study, N_{total} is 100, and the interval time between two adjacent fault points is 20 ms/100, namely 200 μs. The AC systems of scenarios 1-5 are the same as those of scenario 1, and one APT-DFBM is embedded in each phase at the inverters in scenarios 2-5. Figure 8 shows the CF probability curves of scenarios 1-5 with single-phase-to-ground fault.

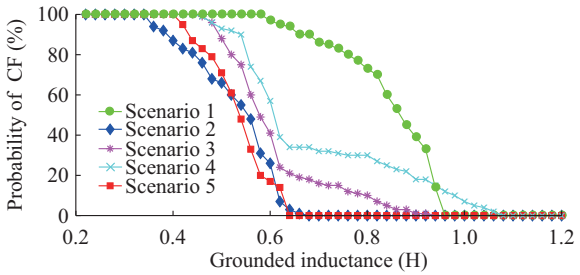

Fig. 8. Probability of CF in scenarios 1-5 with one APT-DFBM under single-phase to ground fault.

In Fig. 8, with the decrease of the grounded inductance, the faults become more serious and all CF probabilities of scenarios 1-5 increase gradually as expected. High CF probability indicates that the CF is likely to occur at the same fault level. In Fig. 8, the CF probability curve of scenario 5 is lower than those of scenarios 1, 3 and 4. Compared with scenario 2, the CF probability of scenario 5 is slightly higher when the fault inductance is in the range of [0.36, 0.52]H. The reasons are as follows: ① as for scenario 2, 2 ms is considered to detect the fault, then the maximum capacitor voltages of APT-DFBMs are provided directly during the initial period after the fault occurs; ② as for scenario 5, at a certain fault occurring time, the capacitors of APT-DFBMs

could be in the charging state, and the capacitor voltage does not reach the maximum value. Therefore, the provided extra voltage-time commutation area during this period is limited, and thus the inhibition on CF may be slightly weakened to some extent. However, the fast fault detection (less than 2 ms) is necessary for scenario 2. Generally, compared with scenarios 1-4, the proposed coordinated control approach of scenario 5 can further reduce the probability of CFs.

2) Three-phase-to-ground Fault

Figure 9 shows the CF probability curves of scenarios 1-5 under a three-phase-to-ground fault, where scenarios 2-5 are embedded with one APT-DFBM in each phase.

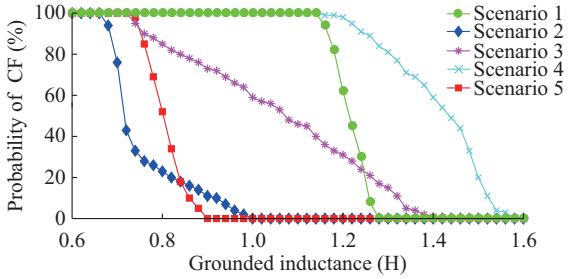

Fig. 9. Probability of CF in scenarios 1-5 with one APT-DFBM under three-phase-to-ground fault.

From Fig. 9, with the decrease of the grounded inductance, the faults become further serious, and CF probability of scenarios 1-5 all increases gradually as expected. The CF probability curve of scenario 5 is significantly lower than those of scenarios 1, 3 and 4. However, compared with scenario 2, the CF probability of scenario 5 is higher when the fault inductance is in the range of [0.68, 0.82]H. Similar to the analysis of Fig. 8, the reason is that the capacitors of APT-DFBMs can be in the charging state and the capacitor voltage does not reach the maximum value at a certain fault occurring time. Therefore, the provided extra voltage-time commutation area during this period is limited, and thus the inhibition on CF may be slightly weakened to some extent. However, the proposed coordinated control approach of scenario 5 can generally further reduce the probability of CFs.

D. Investigation of CF Mitigation in Dual-infeed HVDC System

To further evaluate the effectiveness of the improved coordinated control approach to mitigate CFs, a dual-infeed system is developed in PSCAD/EMTDC as shown in Fig. 10, where U_{d1N} and U_{d2N} are the DC voltages of HVDC1 and HVDC2, respectively; I_{d1N} and I_{d2N} are the DC currents of HVDC1 and HVDC2, respectively; P_{d1N} and P_{d2N} are the DC power of HVDC1 and HVDC2, respectively; U_1 and U_2 are the AC voltages of HVDC1 and HVDC2, respectively; Z_{tie} is the impedance of transmission line; E_1 and E_2 are the equivalent sources for AC systems of HVDC1 and HVDC2, respectively; Z_{s1}, Z_{s2}, Z_{c1}, Z_{c2} are the equivalent impedances for AC systems and filters of HVDC1 and HVDC2, respectively; and z_f is the fault impedance. Here, HVDC1 adopts the ECCC-HVDC in scenarios 1-5 as previously described in Section V-A, HVDC2 adopts LCC-HVDC system, the transmission line between two HVDC links is 50 km, and the parameter of the transmission line is $(0.028+\mathrm{j}0.271)\,\Omega$/km [21]. The inductive fault is applied on the AC busbar of HVDC1, and the CF probability curves of HVDC1 and HVDC2 under single- and three-phase faults are shown in Figs. 11 and 12, respectively.

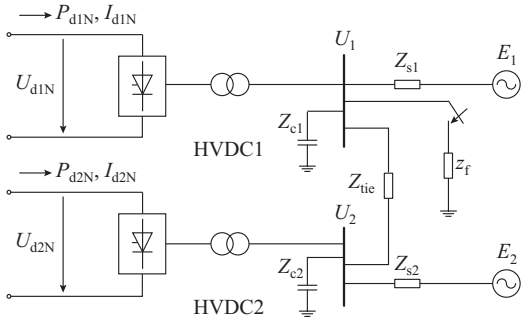

Fig. 10. Dual-infeed HVDC system.

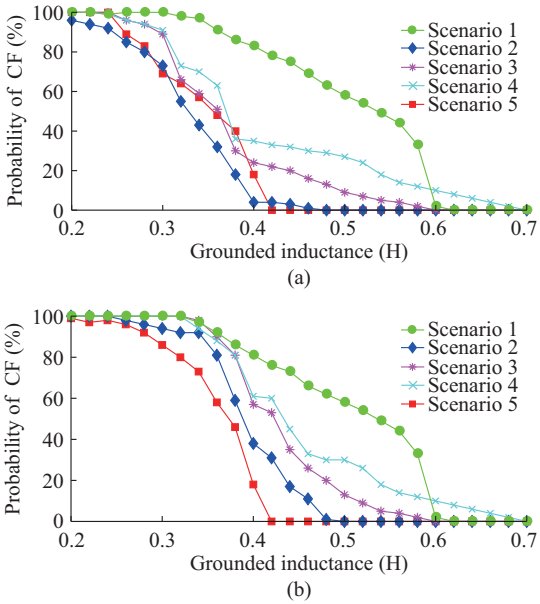

Fig. 11. Probability of CF in dual-infeed HVDC with single-phase fault. (a) HVDC1. (b) HVDC2.

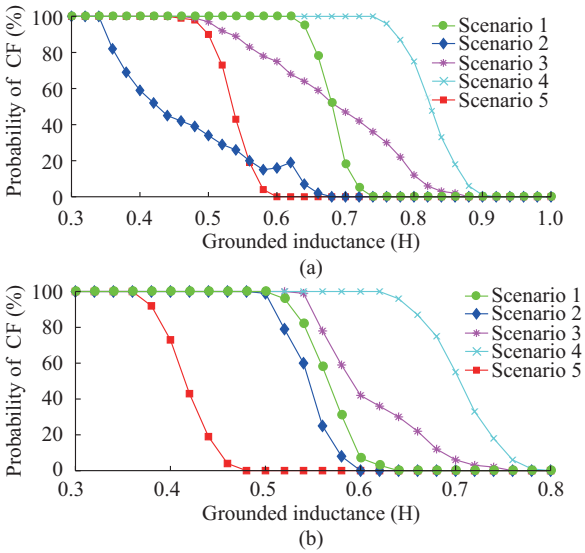

Fig. 12. Probability of CF in dual-infeed HVDC with three-phase fault. (a) HVDC1. (b) HVDC2.

From Figs. 11(a) and 12(a), as for HVDC1 system, the CF probability curve of scenario 5 is lower than those of scenarios 1, 3 and 4; thus, scenario 5 has a lower CF probability. Compared with scenario 2, the CF probability of scenario 5 is higher under certain fault inductance. This is because the capacitors in the APT-DFBMs of scenario 5 can be in the charging state and the capacitor voltage does not reach the maximum value at a certain fault occurring time, as from the previously analysis of Figs. 8 and 9. For HVDC2 system, as shown in Figs. 11(b) and 12(b), the CF probability curve of scenario 5 is significantly lower than that of scenarios 1-4. Therefore, it can be concluded that the proposed improved coordinated control approach can reduce the probability of CF for both local HVDC link and the adjacent HVDC link in dual-infeed HVDC system.

VI. Conclusion

This paper presents a further substantial improvement by proposing an improved coordinated control approach for ECCC-HVDC systems embedded with APT-DFBMs. The essential difference between the improved coordinated control approach and the original control approach in [1] is that the capacitors of the APT-DFBMs are consistently inserted with the improved coordinated control approach under both normal operation and fault conditions. The detailed EMT simulations are conducted based on PSCAD/EMTEC for both single-infeed HVDC and dual-infeed HVDC systems to evaluate the effectiveness of the proposed coordinated control approach. The following conclusions can be obtained.

1) Since the capacitors in the APT-DFBMs consistently contribute to the commutation process with the proposed approach, the ability of ECCC-HVDC system to mitigate the CF issue no longer relies on the fast fault detection, and the CF probability is further reduced.

2) At a certain fault occurring time, the capacitors of APT-DFBMs can be in a charging state and the capacitor voltage does not reach the maximum value, and thus, the CF inhibition ability can be slightly weakened to some extent.

3) The proposed approach can reduce the probability of CF for both local HVDC link and the adjacent HVDC link in dual-infeed HVDC system.

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Chunyi Guo received the B.S. and Ph.D. degrees in power system and automation from North China Electric Power University (NCEPU), Beijing, China, in 2007 and 2012, respectively. He is currently an Associate Professor at NCEPU. His research interests include high voltage direct current (HVDC) and power electronics.

Bo Liu received the B.S. degree from Hebei University of Technology (HEBUT), Tianjin, China, in 2013. Currently, he is pursuing his M.S. degree in power system and automation from North China Electric Power University (NCEPU), Beijing, China. His research interests include HVDC and power electronics.

Chengyong Zhao received the B.S., M.S., and Ph.D. degrees in power system and automation from North China Electrical Power University (NCEPU), Beijing, China, in 1988, 1993, and 2001, respectively. Currently, he is the Deputy Director of the Flexible Transmission and Distribution Institute, Electrical and Electronic Engineering School, NCEPU. His research interests include HVDC, flexible AC transmission systems, and power quality.