Continuous Commutation Failure Suppression Method Based on Self-adaptive Auto-disturbance Rejection Proportional-integral Controller for HVDC Transmission System

Tonghua Wu, Yuping Zheng, Qipu Liu, Guoqiang Sun, Xiaohong Wang, and Xindong Li

***Abstract*—Once an asymmetrical fault occurs on the AC side of the receiving-end of a high-voltage direct current (HVDC) transmission system, the current reference will be affected by the control regulation on the DC inverter side and the commutation voltage asymmetry. In this case, the advance firing angle will fluctuate periodically, causing security threats to the system. If the fault cannot be cleared in time, the effect may be even more serious. However, the traditional proportional-integral (PI) controller cannot effectively suppress the periodic components in the input error signal, which is an important cause of continuous commutation failure. Thus, the system requires more time to recover from the fault. Motivated by this, a self-adaptive auto-disturbance rejection PI controller is proposed in this study. The controller has the advantages of fast response speed and strong anti-interference ability of the auto-disturbance rejection controller. On one hand, it can automatically adjust PI, and the parameters can maintain the system's adaptive ability. On the other hand, the discretization process satisfies the computer simulation requirements. By applying the proposed controller to a system under constant current control and extinction angle control, the dynamic response speed can be improved and the robust performance of the system can be ensured when dealing with a wide range of perturbations. Finally, simulation results show that the proposed algorithm can effectively suppress the continuous commutation failure of DC transmission systems.**

***Index Terms*—High-voltage direct current (HVDC) transmission, continuous commutation failure, periodic fluctuation, self-adaptive auto-disturbance rejection proportional-integral (PI) controller, computer simulation.**

I. Introduction

UNDER the national development strategy of "power transmission from West to East, mutual supply between North and South and nationwide interconnection", high-voltage direct current (HVDC) transmission featured by cross-regional ability, large capacity, and asynchronous grid interconnection, is playing an important role in the grid development of China [1], [2]. However, the semi-controlled device commutated thyristor cannot be turned off through the gate electrode, which relies on grid voltage to help recover the blocking capability. Therefore, commutation failure (CF) is a pivotal factor that hinders the development of DC transmission. As the DC transmission capacity increases, the corresponding short-term power interruptions and other problems can seriously threaten the safe and stable operation of the AC system [3].

The occurrence of CF is related to many factors such as the AC bus voltage, commutation reactance, DC current, converter transformer ratio, and advance trigger angle. Among these, the main reason for CF is that the AC bus voltage drops owing to a ground fault. Generally, the first CF is inevitable. For short-term failure, recovery is normally possible after the fault clearance [4]. If the fault cannot be cleared in time, continuous CF may occur during the DC system recovery period. Continuous CF will lead to the blocking and interruption of power transmission in the DC system, which can result in AC power flow transfer and protection malfunctions.

Reference [5] analyzes the recordings of a DC fault in Tianguang HVDC transmission system of China, which indicates that abundant second-order harmonics will appear in the DC system when continuous CF occurs in a single-phase-to-ground fault. This has been verified by the simulation of the inverter-side failure in an AC system by a real-time digital simulator (RTDS). This study uses this feature to construct 100 Hz protection for the DC system and applies it in practice.

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Reference [6] conducts an elaborate analysis of a fault when the main transformer is charging at an ultrahigh voltage, which causes a magnetizing inrush current and voltage distortion at the inverter-side commutation bus, and leads to periodic CF in the DC system. The recordings show that the magnetizing inrush current causes the converter bus voltage to exhibit abundant second-order harmonics with a long decay period. The influence on the converter bus voltage is similar to the asymmetric fault of the inverter-side AC system. Periodic CF will occur if the fault cannot be cleared in time. The most common fault is a single-phase-to-ground fault in the AC power grid. Therefore, it is necessary to analyze the mechanism of continuous CF caused by an asymmetric fault in the inverter-side AC system and propose a corresponding control strategy.

Existing research has mainly focused on forecasting and topology improvements rather than the analysis of continuous CF and the corresponding control strategy [3], [7]-[9]. However, DC control has a significant impact and can be adjusted sufficiently during this period. Compared with suppressing a single CF, it is more beneficial to suppress continuous CF for improving system stability, which is easier to realize. Reference [10] adds a virtual resistance module to the control system. In the recovery period after a CF, the virtual resistance module can suppress the surge of the DC current, which has a certain effect on suppressing continuous CF. However, the virtual resistance current limiter introduces harmonic current into the control block and thus generates large fluctuations in the current order, which restricts applications under asymmetric faults. Reference [11] shows that the DC current surge and temporary drop in commutation voltage after a fault lead to a gap in the commutation voltage time area. Therefore, a DC current regulation command is designed in [11]. However, this method requires an integration delay of virtual commutation time Δt, which causes the command not to be responded in time and influences the following suppression of CF.

Reference [12] conducts an analysis using a voltage-dependent current order limiter (VDCL). It is considered that the severe disturbance in the input DC voltage can cause fluctuations in the trigger angle command, resulting in continuous CF. It is also considered that an AC bus voltage with a relatively slow change characteristic is more suitable as an input. However, it ignores the mechanism of fluctuations in electrical quantities. The control strategy mentioned above does not improve the continuous CF problem from the perspective of this mechanism.

There are several methods for suppressing continuous CFs at present such as suppression methods based on full-control devices [13]. Reference [14] introduces a flexible DC transmission system that uses full-control devices to fundamentally solve the problem of CF, but the cost is high and the voltage level and transmission capacity are limited.

An HVDC transmission system exhibits nonlinearity and multivariable strong coupling when disturbed, whereas a traditional PI control framework provides a typical linear control. Therefore, it requires to redesign the controller to improve the performance during transient process.

Auto-disturbance rejection control (ADRC) is a novel control technology that does not depend on a mathematically accurate model of the controlled plant, and manages to automatically detect and compensate for internal and external disturbances. It can achieve good control results even when the control object encounters uncertain disturbances or changes in parameters. This kind of control, owing to its higher adaptability and robustness, is partly applied in the switch and excitation of thermal power units.

Reference [15] proposes a low-frequency oscillation suppression method for a traction network based on ADRC. ADRC can overcome the contradiction between rapidity and overshoot in the PI controller. This allows for the estimation of the disturbance in time and nonlinear dynamic compensation, which results in better performance than that of the PI controller.

Reference [16] applies ADRC to a DC transmission system for the first time, which uses the extended state observer to extract the disturbance signal, and compensates for the input to obtain a good control effect. However, the effects of discrete systems on the high-frequency flutter and communication delays in the differential tracker are not considered in [16], nor is the relation to CF. Therefore, this paper deals with the need for discretization simulations, redesigns the ADRC, and introduces the *fal* function to realize the parameter self-tuning process.

We propose a self-adaptive auto-disturbance rejection proportional integral controller (SAADR-PI) to improve the constant current and constant extinction angle control on the rectifier and inverter sides, respectively.

The remainder of this paper is organized as follows. Section II discusses the mechanisms of single CF and continuous CF, and it is pointed out that the main factors leading to continuous CF are harmonic components in the trigger angle. In Section III, based on the deficiency of the linear PI controller, an SAADR-PI control strategy is proposed to enhance the accuracy of the tracking command value during the transient process. In Section IV, the performance of the proposed strategy is validated through several simulations in RTDS. The results verify the effectiveness of the mechanism analysis of continuous CF and the control strategy proposed in this paper. Finally, Section V concludes this paper.

II. CF Mechanism and Influencing Factors

A. Single CF and Continuous CF

The Graetz bridge is the most basic structure that constitutes an HVDC converter. As indicated in Fig. 1, it includes six thyristors and triggers in the order of T1-T6. This enables the system to operate in rectification or inverter mode by adjusting the firing angles. Because of the leakage reactance of the converter transformer and the impedance of the AC system, there is an overlap time μ in the commutation. In addition, when two adjacent converter valves in the same bridge arm group are commutated, the valve that has just been turned off needs to withstand a reverse voltage for a period of time to restore the blocking capability. This period of time is called deionization, and the corresponding angle is the margin angle γ.

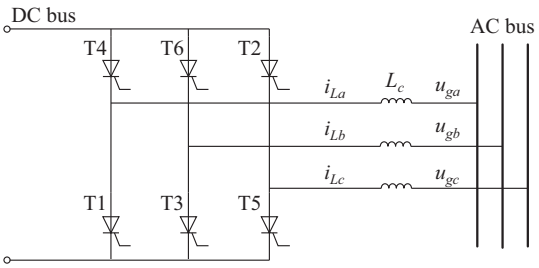

Fig. 1. HVDC inverter-side Graetz bridge topology.

Figure A1 in Appendix A shows the voltage and current waveforms of the Graetz bridge in the rectifier and inverter modes. Taking the commutation of inverter-side T1 to T3 as an example, Fig. A1 shows that T1, T2, and T3 are simultaneously conducted during the commutation overlap time μ_i, and T2 and T3 are simultaneously conducted during γ_i. If the commutation process is not complete or the commutation process is complete but the valve blocking capability is not restored, the valve forward voltage becomes positive, and the valve that is expected to be turned off will be conducted once again. This is called CF [17].

CF can be divided into single and continuous CF. A single CF implies that only one CF occurs in DC transmission. The first CF after an AC system fault on the inverter side occurs very quickly, and the DC system operates under hysteresis control. The operation begins only if the AC fault is detected. As the operation time is limited, even if preventive control measures are taken, it is difficult to avoid the first CF in DC transmission.

Continuous CF in DC transmission implies that there are one or more CFs in the DC system after the first CF. After the first CF, the DC system control block has sufficient time to adjust and recover from the fault. Therefore, the occurrence of continuous CF is related to the functioning of the DC system control block [18]. A single CF has a short duration, and its impact on the AC system is limited. A continuous CF has a long duration, during which electrical quantities such as the DC current, DC voltage, and commutated bus voltage change drastically, causing adverse impacts that are harmful to the safety and stability of the AC/DC system. Thus, it is necessary to study and improve it.

B. DC Control Block

The control block of the DC system adopts a hierarchical control, namely, the system control level, pole control level, and valve control level. The lower the level is, the faster the response of the control will be. The response speed of the valve control is measured in milliseconds. Most research and improvements are aimed at the structure of the pole control level.

This study aims at the control framework in the CIGRE benchmark model [19]. As indicated in Fig. A2 in Appendix A, U_{dc} is the inverter-side DC voltage; γ_{inv} is the inverter-side extinction angle; $I_{d,order}$ is the DC current reference value given by the main control; and $\beta_{inv,\mathrm{CC}}$ and $\beta_{inv,\mathrm{CEA}}$ are the inverter-side advance trigger angle command outputs from the constant current control and constant extinction angle control, respectively.

The measurement is often replaced by a first-order inertia section, where the inertia time constant T reflects the response speed of the measuring device, and the gain G converts the actual values of DC voltage and current into a per-unit value. Figure A2 shows that the rectifier side adopts a constant current controller, and that the inverter side combines a constant current controller and constant extinction angle controller. In addition, the inverter side is equipped with a DC-current bias control, which enables smooth switching from constant extinction angle control to constant current control.

In general, $I_{d,order}$ is set as 1 p.u.. After a fault occurs, γ quickly falls and enables constant extinction angle control. To avoid the first CF, the output of constant extinction angle control will increase the advance trigger angle β_{inv}. The speed of the trigger angle increases depending on the traditional linear PI controller parameters. Considering the CIGRE HVDC benchmark model parameters, it takes 110 ms for β_{inv} to increase to 90° [19]. This time is too slow for fault transient control, which makes it difficult to avoid the first CF.

C. Effect of Second-order Harmonic on Continuous CF

After the first CF occurs, one or multiple CFs may occur again during the recovery process owing to the drastic change in the output angle command under DC control. DC transmission may develop from a single CF to a continuous CF. Reference [20] points out that the negative-sequence voltage and the positive-sequence third-order harmonic component of the AC system will cause the secondary component to fluctuate, which will then cause the DC current command value to fluctuate drastically. This is the key reason for continuous CF.

Figure A3 in Appendix A shows the simulation results of the CIGRE benchmark model on the RTDS platform. The single-phase ground fault on the AC side occurs at 2 s, and the fluctuation of the electrical quantity can be observed during the two consecutive CFs. The figure shows that the delay trigger angle, extinction angle, and DC current all have second-order harmonic components. In the practical application of AC/DC hybrid power grid engineering, 100 Hz protection is also an important part of DC system protection [21]. Therefore, harmonic filtering on the DC side is a pivotal factor in solving the control during a fault.

III. Suppression Measures of Continuous CF

According to the above analysis of continuous CF, the strategy to suppress this problem should start with the following two aspects: first, to solve the second-order harmonic component in the collected electrical quantity; and second, to enhance the tracking accuracy of the trigger angle command and reduce the delay effect. To this end, the following control strategy is proposed to deal with continuous CF.

After the DC system detects a fault, the control strategy starts. After DC low-pass filtering, a second-order band-stop filter with a center frequency of 100 Hz is added to filter out the second-order harmonic component of the DC current signal for reducing the second-order harmonic component of

the advance trigger angle command β_{inv}.

Given that the linear PI controllers cannot achieve good performance for nonlinear systems such as HVDC, a novel controller is designed based on the idea of the ADRC theory to replace the original PI controller and improve the tracking accuracy of the trigger angle command under internal and external disturbances. The steps will be introduced in detail as below.

A. Mathematical Model of Line Commutated Converter HVDC

The dynamic equation of the line commutated converter (LCC) HVDC transmission system can be expressed as:

$$\begin{cases} L_{dr\Sigma}\dfrac{\mathrm{d}I_{dr}}{\mathrm{d}t} = -R_d I_{dr} + \dfrac{3\sqrt{2}}{\pi}V_{ar}\cos\alpha - \dfrac{3}{\pi}X_r I_{dr} - V_c \\ L_{di\Sigma}\dfrac{\mathrm{d}I_{di}}{\mathrm{d}t} = -R_d I_{di} + \dfrac{3\sqrt{2}}{\pi}V_{ai}\cos\beta - \dfrac{3}{\pi}X_i I_{di} + V_c \\ C_{dc}\dfrac{\mathrm{d}V_c}{\mathrm{d}t} = I_{dr} - I_{di} \end{cases} \tag{1}$$

where $L_{dr\Sigma}$ and $L_{di\Sigma}$ are the rectifier-side and inverter-side total impedances, respectively; C_{dc} is the DC capacitor; R_d is the DC resistance; V_c is the voltage of the DC capacitor; and X_r, V_{ar}, and I_{dr} are the commutation reactance, AC bus voltage, and DC current on the rectifier side, respectively. Correspondingly, X_i, V_{ai}, and I_{di} represent those on the inverter side. α is the rectifier-side delay firing angle; and β is the inverter-side advance firing angle. Considering the trigger delay of the control section, we obtain:

$$\begin{cases} \dfrac{\mathrm{d}\alpha}{\mathrm{d}t} = \dfrac{1}{T_\alpha}\left(-\alpha + \alpha_0 + u_\alpha\right) \\ \dfrac{\mathrm{d}\beta}{\mathrm{d}t} = \dfrac{1}{T_\beta}\left(-\beta + \beta_0 + u_\beta\right) \end{cases} \tag{2}$$

where T_α is the constant time of delay firing angle α; T_β is the constant time of advance firing angle β; α_0 and β_0 are the reference delay firing angle and the reference advance firing angle, respectively; and u_α and u_β are the control laws of the rectifier-side delay firing angle and the inverter-side advance firing angle, respectively.

For the control targets of the rectifier side and the inverter side, the constant current control is the tracking current command, and (3) is guaranteed:

$$y_r = I_{dr} - I_{d,order} = 0 \tag{3}$$

The inverter-side constant extinction angle γ should guarantee the following output:

$$y_i = \gamma - \gamma_0 = \arccos\left(\cos\beta + \frac{\sqrt{2}\,X_i I_{di}}{V_{ai}}\right) - \gamma_0 = 0 \tag{4}$$

where γ_0 is the reference inverter-side extinction angle.

By deriving (1) on both sides, we obtain:

$$\frac{\mathrm{d}^2 I_{dr}}{\mathrm{d}t^2} = \frac{1}{L_{dr\Sigma}}\left[-\left(R_d + \frac{3}{\pi}X_r\right)\frac{\mathrm{d}I_{dr}}{\mathrm{d}t} - \frac{\mathrm{d}V_c}{\mathrm{d}t} + \frac{3\sqrt{2}}{\pi}\left(\frac{\mathrm{d}V_{ar}}{\mathrm{d}t}\cos\alpha - V_{ar}\frac{\mathrm{d}\alpha}{\mathrm{d}t}\sin\alpha\right)\right] \tag{5}$$

Then, by substituting (2) into (1), the standard form of input/output is derived as:

$$I_{dr}^{(2)} = f\left(I_{dr}, I_{dr}^{(1)}, w_r\right) + b_r u_\alpha \tag{6}$$

where w_r is the disturbance variable in the rectifier-side state function. The function and parameter in (6) are as follows:

$$f\left(I_{dr}, I_{dr}^{(1)}, w_r\right) = \frac{1}{L_{dr\Sigma}}\left\{-\left(R_d + \frac{3}{\pi}X_r\right)\frac{\mathrm{d}I_{dr}}{\mathrm{d}t} - \frac{\mathrm{d}V_c}{\mathrm{d}t} + \frac{3\sqrt{2}}{\pi}\left[\frac{\mathrm{d}V_{ar}}{\mathrm{d}t}\cos\alpha - \frac{V_{ar}}{T_\alpha}\left(-\alpha + \alpha_0\right)\sin\alpha\right]\right\} \tag{7}$$

$$b_r = -\frac{3\sqrt{2}}{\pi T_\alpha L_{dr\Sigma}}V_{ar}\sin\alpha \tag{8}$$

Equation (6) satisfies the ADRC standard form and can be controlled with a second-order ADRC. Similarly, by deriving the inverter-side constant extinction angle control, we can obtain:

$$\frac{\mathrm{d}\gamma}{\mathrm{d}t} = -\frac{1}{\sqrt{1-\left(\cos\beta + \sqrt{2}\,X_i I_{di}/V_{ai}\right)^2}} \cdot \left[-\frac{\mathrm{d}\beta}{\mathrm{d}t}\sin\beta + \frac{\sqrt{2}\,X_i\left(\dot{I}_{di}V_{ai} - I_{di}\dot{V}_{ai}\right)}{V_{ai}^2}\right] \tag{9}$$

By combining (2), the standard form of input or output is expressed as:

$$I_{di}^{(1)} = f\left(I_{di}, w_i\right) + b_i u_\beta \tag{10}$$

where w_i is the disturbance variable on the inverter-side state function; and b_i is given as:

$$b_i = -\frac{\sin\beta}{T_\beta\sqrt{1-\left(\cos\beta + \dfrac{\sqrt{2}\,X_i I_{di}}{V_{ai}}\right)^2}} \tag{11}$$

Similarly, a first-order ADRC can be used as a control.

B. Design of SAADR-PI Controller

The ADRC consists of three parts: tracking differentiator (TD), extended state observer (ESO), and nonlinear state error feedback (NLSEF). The ADRC compensates for the disturbance to the system by accurately estimating the total disturbance. Simplifying the system equivalent to a series integral structure by estimation and compensation, the control law of the controlled plant can be easily designed. The advantages include independence of the precise mathematical model of the controlled object, strong anti-disturbance ability, and good adaptability. A typical block diagram of an ADRC controller is shown in Fig. 2.

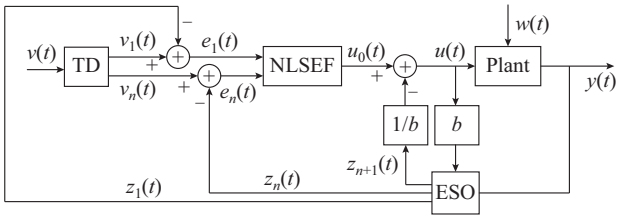

Fig. 2. Auto-disturbance rejection algorithm control block diagram.

In Fig. 2, $v(t)$ is the input signal; $z(t)$ is the observer output signal; $e(t)$ is the error signal; $u(t)$ is the control signal;

$w(t)$ is the disturbance signal; and $y(t)$ is the output signal. Since the tracking differentiator is implemented in a simulation system, a discrete algorithm must be used. This paper proposes optimal control synthesis function of the discrete form of the tracking differentiator. Discretization is also used in the rest of the system design.

Taking the second-order system $\ddot{x}=f\left(x,\dot{x},w\left(t\right)\right)+bu\left(t\right)$ as an example, the specific algorithm has three parts:

1) Setting $v(k)$ as the input signal at sampling instant k, the transition process can be arranged and the input can be extracted as (12).

$$\begin{cases} v_1(k+1)=v_1(k)+hv_2(k) \\ v_2(k+1)=v_2(k)+hfhan\left(v_1(k)-v(k),v_2(k),r,h_0\right) \end{cases} \tag{12}$$

where $v_1(k)$, $v_1(k+1)$ are the arranged transition processes at sampling instant k and $k+1$, respectively, which are differentiable smooth signals; $v_2(k)$ and $v_2(k+1)$ represent $\mathrm{d}v_1(k)/\mathrm{d}t$ and $\mathrm{d}v_1(k+1)/\mathrm{d}t$, respectively; h is the integration step length; and h_0 is the parameter that determines the filtering effect when the input signal is contaminated by noise. The function $fhan(v_1,v_2,r,h)$ is expressed as:

$$\begin{cases} d=rh \\ d_0=rh^2 \\ y=v_1+hv_2 \\ a_0=\sqrt{d^2+8r\left|y\right|} \end{cases} \tag{13}$$

$$a=\begin{cases} v_2+\dfrac{\left(a_0-d\right)}{2}\mathrm{sgn}\left(y\right) & \left|y\right|>d_0 \\ v_2+\dfrac{y}{h} & \left|y\right|\le d_0 \end{cases} \tag{14}$$

$$fhan=-\begin{cases} r\,\mathrm{sgn}\left(a\right) & \left|a\right|>d \\ r\dfrac{a}{d} & \left|a\right|\le d \end{cases} \tag{15}$$

where r and h are the adjustment parameters.

2) The observation of system states and extended states (total disturbances) by input u and output y can be expressed as:

$$\begin{cases} e(k)=z_1(k)-y(k) \\ z_1(k+1)=z_1(k)+h\left(z_2(k)-\beta_{01}fal\left(e(k),\alpha_{01},\delta_0\right)\right) \\ z_2(k+1)=z_2(k)+h\left(z_3(k)-\beta_{02}fal\left(e(k),\alpha_{02},\delta_0\right)+b_0u\right) \\ z_3(k+1)=z_3(k)-h\beta_{03}fal\left(e(k),\alpha_{03},\delta_0\right) \end{cases} \tag{16}$$

where α_{01}, α_{02}, β_{01}, β_{02}, and β_{03} are the adjustment parameters; and b_0 is the estimated value of b. The function $fal(\cdot)$ can be expressed as:

$$fal\left(e,a,\delta\right)=\begin{cases} \dfrac{e}{\delta^{1-\alpha}} & \left|e\right|\le\delta,\delta>0 \\ \left|e\right|^{\alpha}\mathrm{sgn}\left(e\right) & \left|e\right|>\delta>0 \end{cases} \tag{17}$$

where α is a constant related to the tracking effect, which is inversely proportional to the tracking effect, whereas the filtering effect is degraded when α decreases; and δ_0 is a constant that affects the filtering effect and is proportional to the filtering effect, whereas its increase causes a tracking delay. When the signal error is large, the function $fal(\cdot)$ produces a small feedback gain. This satisfies the requirements of system stability and rapidity.

3) Finally, the state error feedback control law is designed as:

$$\begin{cases} e_1=v_1(k)-z_1(k) \\ e_2=v_2(k)-z_2(k) \\ u_0=k_P fal\left(e_1,\alpha_1,\delta\right)+k_D fal\left(e_2,\alpha_2,\delta\right) \\ u=u_0-z_3(k)/b_0 \end{cases} \tag{18}$$

where e_1 and e_2 are the errors between the arranged transition process v_1 and system output estimate z and the differential of this error, respectively. The nonlinear control of the series integral plant is realized by selecting the nonlinear parameters α_1, α_2, δ, and parameters k_P and k_D reasonably.

C. DC System Control Based on SAADR-PI

The SAADR-PI controller inherits the advantages of fast response speed and strong anti-interference ability of the ADRC controller. Moreover, it can automatically adjust the PI parameters through the function $fal(\cdot)$ to maintain the adaptive ability of the system. By applying it to the current and turn-off angle control strategy, the dynamic response speed and the robust performance of the system can both be improved.

This paper applies an SAADR-PI controller to the rectifier-side constant current and the inverter-side constant extinction angle control strategy to replace the traditional linear PI controller. The DC system closed-loop control block diagram is shown in Fig. 3. The green frame on the left in Fig. 3 is a second-order band-stop filter with a center frequency of 100 Hz to filter out the second-order harmonic component in the DC current and extinction angle measurement. The red frame on the right is the algorithm mentioned above. The constant current control realized by a PI controller on the inverter side is not improved because the inverter side is rarely in the constant current control state. It will only start when the rectifier-side AC bus voltage drops significantly, and hence, it is completely different from the situation discussed in this paper.

The parameters of the tracking differentiator are adjusted according to the requirements of the transition process. The larger the speed factor r is, the faster the tracking speed will be [22]. Adjusting the parameters of the extended state observer enables the controller to estimate the combined effect of the parameter input and external disturbances as quickly and accurately as possible. β_{01} and β_{02} are the feedback gains of the state error. The larger the values are, the smaller the lag of the disturbance estimation and the faster the convergence will be.

The parameter α in the function $fal(\cdot)$ determines the degree of nonlinearity. The following principles are based on engineering application experience. In a proportional link, $0<\alpha_1<1$ is set to achieve the goal of "large gain for small error, small gain for large error". The differential link requires that the differential gain is small (large) when the differential error is small (large), so we set $\alpha_2>1$. Thus, the differential effect will be smaller when it is close to the steady

state, which will help improve the performance of the control system [23], [24].

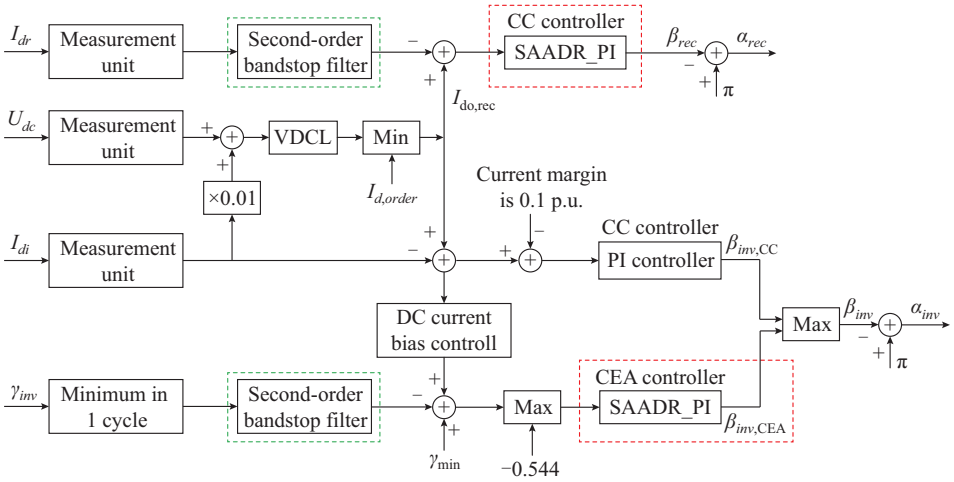

Fig. 3. Improved closed-loop control block diagram of HVDC transmission system.

IV. Simulation Analysis

The CIGRE HVDC benchmark model is built using the RTDS simulation software to verify the control method for suppressing continuous CF [25]. Figure A4 in Appendix A shows the main circuit diagram of the CIGRE HVDC benchmark model.

The main parameters of the test model are listed in Table BI in Appendix B, and the parameter settings in the control strategy are shown in Table BII.

A ground fault is applied on the inverter-side commutation bus, and the adjustable grounding inductance value L_f is used to simulate the different distances of the AC system faults from the commutation bus. The smaller the grounding inductance value is, the closer the AC system fault is to the commutation bus, and the more serious the fault will be [26]. The simulation analysis of the responses of the three control methods in different inverter-side AC system failure cases is given below.

1) Control method 1: only the original CIGRE HVDC benchmark model control block is used.

2) Control method 2: based on the control of the CIGRE HVDC benchmark model, the virtual resistance current-limiting method proposed in [10] is added.

3) Control method 3: the proposed SAADR-PI controller is used.

Control methods 1 and 2 are compared with control method 3 proposed in this paper in order to verify the effect of the proposed algorithm in suppressing continuous CF. This paper focuses on the response of physical quantities such as the extinction angle, DC current, DC voltage, and DC transmission power after failure. Among these, the extinction angle response curve is used to judge whether the DC power transmission fails to commutate. The DC current, DC voltage, and transmission power response curve are used to observe the dynamic process during the fault. To facilitate the comparison, the response curves of the above physical quantities using the three control methods are placed in the same coordinate system. In Fig. 4, the lines of green, blue, and red separately represent the results of control methods 1-3.

When there is a single ground fault at 4 s on the inverter-side converter bus, the grounding inductance $L_f = 0.89$ H, and the fault lasts for 0.5 s. Under the fault condition, the simulation results of the respective electric quantities using the three control methods are shown in Fig. 4(a). It can be seen from Fig. 4(a) that for control method 1, the extinction angle is reduced to 0° twice, corresponding to the two consecutive CFs. The existence of the second-order harmonic in the DC current is the main cause of two consecutive CFs.

With regard to the first CF, the fault time on the inverter-side AC bus is very short, and the DC system control block has limited action. After the fault, it is difficult to avoid the first CF. However, an appropriate control method such as control method 2 can effectively avoid the second CF. VDCL is activated by the virtual resistor in advance, but the first CF cannot be avoided. Control method 3 effectively avoids the first CF and continuous CF.

Since the controller does not change the original control frame, the inverter side still adopts constant extinction control during the fault. The DC voltage is always approximately 0.9 p.u. during the AC voltage drop, and the power level is also 0.9 p.u.. Moreover, it recovers to the rated operation point within 0.1 s after the fault is cleared. This shows the effective tracking capability of the SAADR-PI controller and meets the requirements of actual engineering operations.

Similarly, by applying a phase-to-phase short circuit and a two-phase grounding fault to an AC system, the fault inductance is set to be 1.12 H and 0.95 H, respectively, and the system simulation waveforms are shown in Fig. 4(b) and (c). It can be seen that similar to a single-phase ground fault, the proposed algorithm can successfully suppress the occurrence of the first CF and continuous CF. Moreover, the initial operation power is restored within 0.1 s after the fault.

As the probability of CF is closely related to the initial fault time, it is necessary to examine the impact of different initial fault times on the performance of the control strategy

under the same fault [27]. Figures C1-C3 in Appendix C show the simulated statistical results of three asymmetric faults: single-phase grounding, two-phase short-circuit, and two-phase short-circuit grounding. Table CI in Appendix C lists the critical ground impedances of the three algorithms for different faults and initial times. The initial time is 20 ms per cycle, with steps every 2 ms from 4 s to 4.018 s. The grounding reactance varies from 0.5 H to 1.5 H.

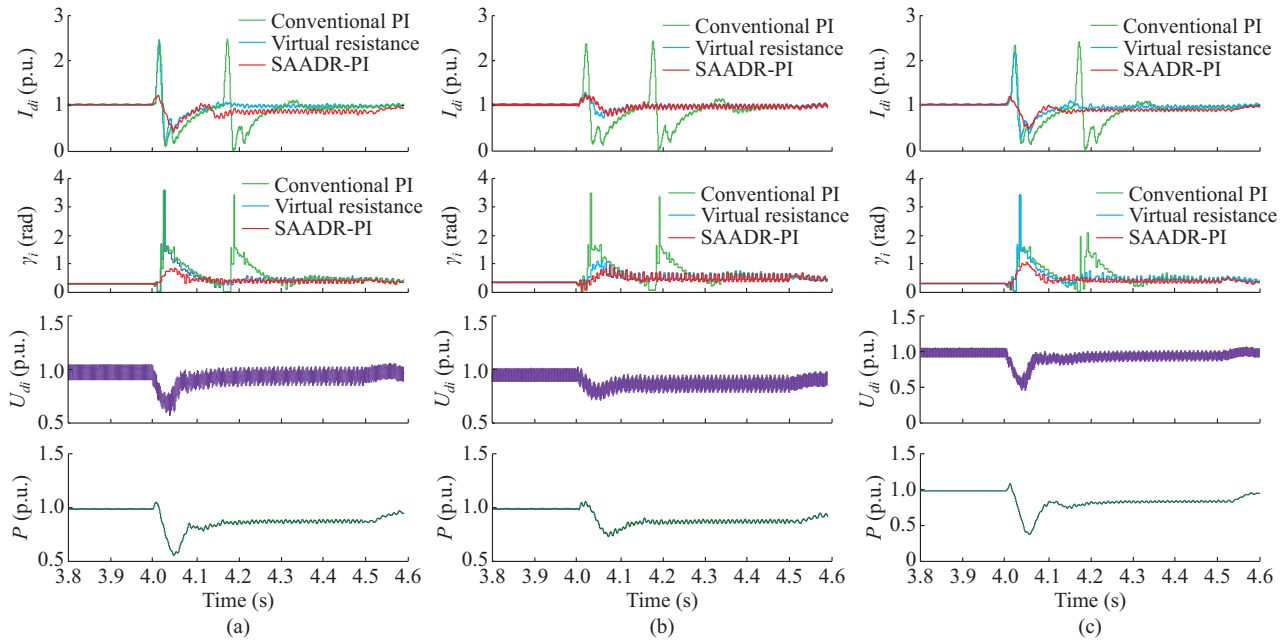

Fig. 4. DC system response curve under different asymmetric fault types. (a) Single-phase ground fault with grounding inductance L_f=0.89 H. (b) Two-phase phase-to-phase short circuit with fault inductance L_f=1.12 H. (c) Two-phase grounding short circuit with grounding inductance L_f=0.95 H.

The white marks in Figs. C1-C3 show that no CF occurs in the original CIGRE benchmark model. The green marks indicate that no CF occurs under the proposed control strategy. The yellow marks indicate that only the first CF occurs under the proposed control strategy. And the red marks indicate that a continuous CF occurs more than twice. It can be seen from the figure that continuous CF is most likely to occur between 4.006 s and 4.016 s because the valve is about to be commutated or is under the process of commutation. Therefore, the control strategy responds too late. For the rest of the time when the fault is quite severe, the voltage drop on the AC side makes it impossible to support the completion of the commutation, which will also result in the occurance of continuous CF.

V. Conclusion

This study analyzes the characteristics of electric quantity changes after asymmetrical faults such as phase-to-ground on an inverter-side AC bus. Then, a method is proposed to suppress continuous CF based on ADRC. The conclusions are as follows.

1) After a fault occurs, abundant second-order harmonic components appear in the DC current and extinction angles of the DC system, causing the trigger angle to exhibit significant periodic fluctuations. This is the main cause of continuous CF in the system.

2) A control strategy for a discrete computer simulation is designed based on the ADRC theory. By improving the response rate and enhancing the robustness under external disturbances, the system can effectively suppress continuous CF and shorten the recovery time after system failure. The simulation results verifiy the effectiveness of the proposed algorithm.

Appendix A

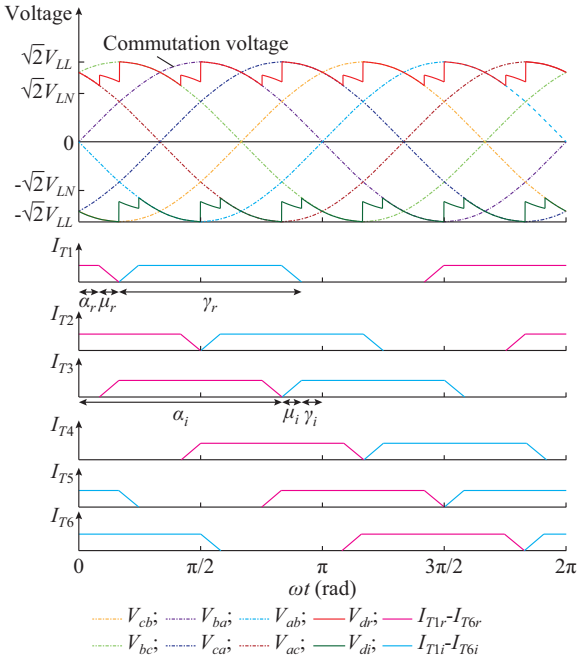

Fig. A1. Voltage and current waveforms of converter in rectifier and inverter modes.

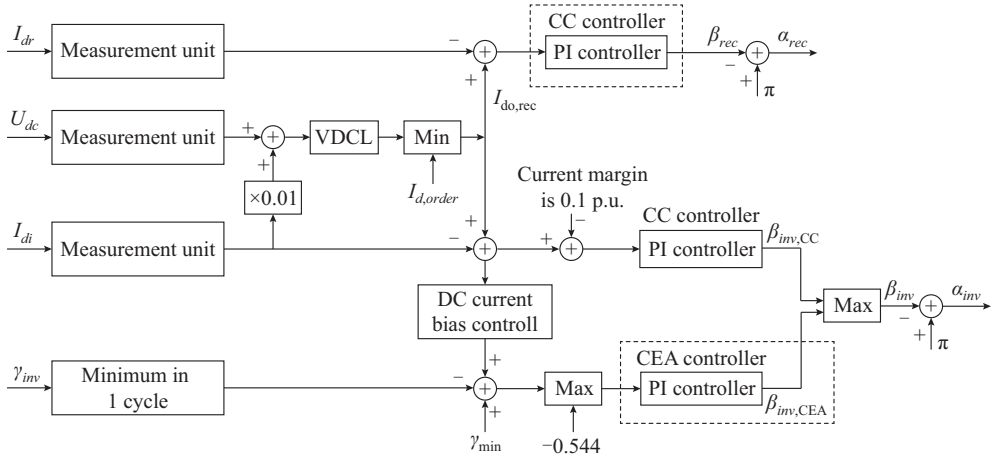

Fig. A2. Diagram of CIGRE HVDC control block.

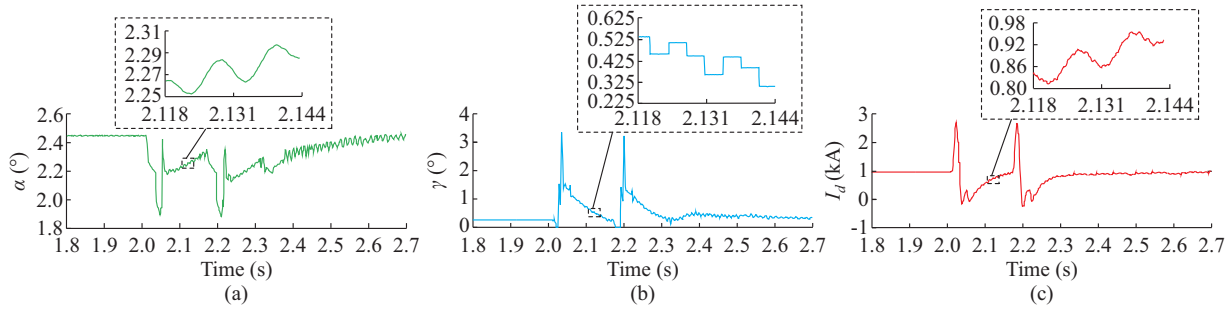

Fig. A3. Electrical quantities waveform under continuous CF. (a) α. (b) γ. (c) I_d.

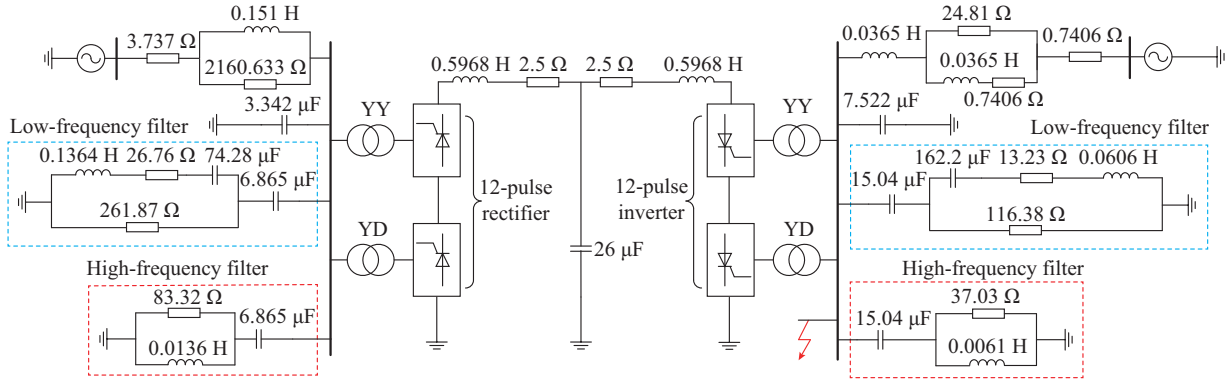

Fig. A4. Topology of CIGRE HVDC benchmark model.

APPENDIX B

The parameters of CIGRE HVDC benchmark model and SAADR-PI controller are given in Tables BI and BII, respectively.

TABLE BI
PARAMETERS OF CIGRE HVDC BENCHMARK MODEL

Parameter	Rectifier	Inverter	Parameter	Rectifier	Inverter
Rated AC voltage	345 kV	230 kV	Converter station equivalent resistance x	0.0342 p.u.	0.03247 p.u.
Benchmark capacity	100 MVA	100 MVA	Equivalent potential source impedance $(R+jL)$	$(3.737+j0)\Omega$	$(0.7406+j11.461)\Omega$
Rated DC voltage U_d	500 kV	500 kV	System frequency	50 Hz	50 Hz
Rated DC current I_d	2 kA	2 kA	Minimum trigger angle	$\alpha=15°$	$\gamma=15°$
Transformer leakage resistance	0.18 p.u.	0.18 p.u.	Time constant	0.02 s	0.05 s

TABLE BII
SELECTION OF SAADR-PI CONTROLLER PARAMETERS

Control	Controller submodule	Parameter name	Value
Constant current control	Differential tracker	r	10
		h_0	0.01
	Extended state observer	α_{01}	1
		α_{02}	0.5
		α_{03}	0.25
		b_0	–38
		β_{01}	100
		β_{02}	500
		β_{03}	1200
		δ_0	0.01
	Nonlinear feedback control law	α_1	0.75
		α_2	1.5
		k_p	0.25
		k_d	35
		δ	0.5
Constant extinction angle control	Differential tracker	r	2
		h_0	0.01
	Extended state observer	α_{01}	1
		α_{02}	0.5
		b_0	–30
		β_{01}	575
		β_{02}	1125
		δ_0	0.01
	Nonlinear feedback control law	α_1	0.75
		k_p	0.35
		δ	0.5

APPENDIX C

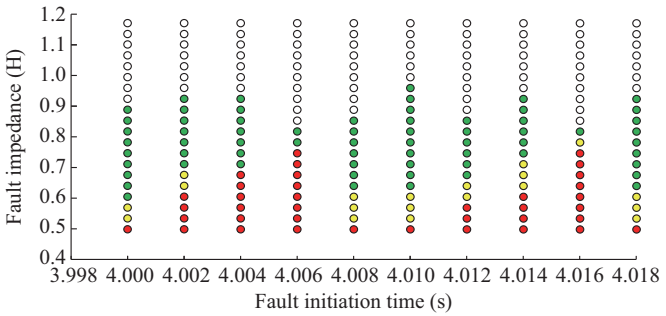

Fig. C1. Statistics of simulation results of single-line-to-ground faults under different ground reactance and fault times.

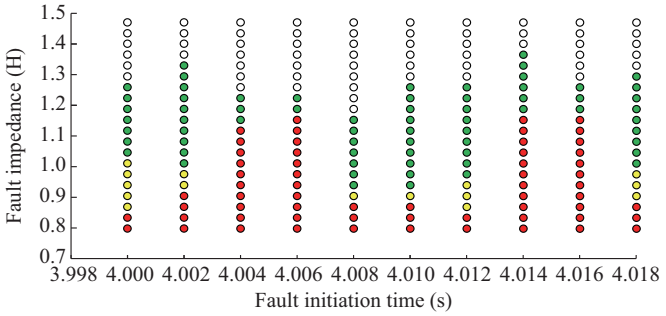

Fig. C2. Statistics of simulation results of line-to-line faults under different ground reactance and fault times.

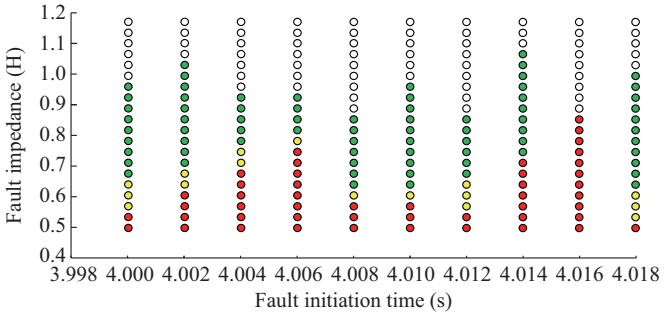

Fig. C3. Statistics of simulation results of two-line-to-ground faults under different ground reactance and fault times.

TABLE CI
CRITICAL GROUND IMPEDANCE BETWEEN ALGORITHMS FOR DIFFERENT FAULTS AND INITIAL TIMES

Initial time	Single-phase grounding fault (H)			Two-phase short-circuit fault (H)			Two-phase short-circuit grounding fault (H)		
	Traditional PI	Virtual resistance	SAADR-PI	Traditional PI	Virtual resistance	SAADR-PI	Traditional PI	Virtual resistance	SAADR-PI
4.000	0.93	0.83	0.57	1.26	1.18	1.02	0.96	0.82	0.63
4.002	0.84	0.81	0.67	1.32	1.21	0.98	1.03	0.78	0.68
4.004	0.65	0.65	0.68	1.22	1.18	1.10	0.92	0.78	0.73
4.006	0.87	0.79	0.73	1.21	1.12	1.13	0.92	0.83	0.79
4.008	0.92	0.82	0.60	1.14	1.05	0.91	0.84	0.71	0.61
4.010	0.89	0.77	0.61	1.25	1.15	0.92	0.97	0.80	0.60
4.012	0.77	0.74	0.64	1.27	1.20	0.94	0.86	0.75	0.62
4.014	0.69	0.68	0.72	1.34	1.17	1.16	1.07	0.72	0.70
4.016	0.86	0.80	0.78	1.26	1.18	1.15	0.85	0.84	0.84
4.018	0.92	0.76	0.61	1.29	1.03	0.99	0.96	0.73	0.62

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