

Optimized Protection Strategies for HVDC Grid with Fault-blocking Modular Multilevel Converters for Overhead Line Applications

Sheng Yan, Zhiyuan He, Jie Yang, Ming Kong, and Minqiang Hu

Abstract—The high-voltage direct current (HVDC) grid has been recognized as an effective solution for renewable energy integration. Currently, two main development trends for HVDC grids are being studied: a DC breaker based HVDC grid and fault-blocking converter based HVDC grid. Although the former has a perfect performance for fault clearance, its development is still highly constrained by the cost and maturity of DC breakers. The latter can extinguish DC faults by the fault-blocking converters. Without using DC breakers, there is no bottleneck in its technical feasibility. Nevertheless, in fault scenarios, such types of HVDC grids will be blocked at length for air-deionization, which is its main drawback. The aim of this paper is to minimize its power interruption time, by optimizing protection coordination strategies. To cover the most complex cases, the overhead line applications, in which the reclosure actions are required to be implemented, are considered. In this paper, the protection requirements of HVDC grids are first discussed, then the benefits of fault-blocking modular multilevel converters (MMCs) and their fault features are analyzed. Based on this, a control function is designed to reduce the air-deionization time. To minimize the influence of the DC faults, a separation methodology for restarting the system is proposed. The effectiveness of the proposed protection coordination schemes is validated by PSCAD/EMTDC simulations.

Index Terms—Modular multilevel converter (MMC), high-voltage direct current (HVDC), overhead line, fault-blocking converter, protection coordination.

I. INTRODUCTION

THE high-voltage direct current (HVDC) grid is effective for the reliable integration of large-scale renewable energy. It can be connected directly to weak power grids in renewable energy concentration areas and is far easier for realizing the optimal allocation of different energy resources [1], [2].

Nevertheless, it has been recognized that the conventional half-bridge modular multilevel converter (MMC) is vulnera-

ble to DC faults [3]–[7]. In the case of a DC fault, the converters will be subjected to serious over-current and are quickly blocked. This may result in the shutdown of the entire HVDC grid. Therefore, a method for quickly isolating DC faults has been a significant challenge for HVDC grids.

Currently, available configurations proposed for the HVDC grid can be classified into two approaches. One is to use a high-voltage DC circuit breaker (DCCB) to isolate the faulty DC lines [8]–[10]. The other is to adopt fault-blocking converters [11], [12], which prevent the continuous discharge of energy storage units by blocking the converters or changing their control modes. Then, the isolation of faulty lines is achieved by fast DC mechanical switches. It seems that the solution using a DCCB is more suitable for the MMC-based HVDC grids. However, due to the limitation of current DCCB technologies [13], [14], the latter is also deemed a suitable choice for constructing an HVDC grid. For example, Germany is planning to use fault-blocking converter technology in the ULTRANET project to forward its super-grid construction plan [15].

In terms of the fault-blocking converter based HVDC grid, the current primary concentration is focusing on the converter level. For example, several topologies are proposed with the capability of blocking fault currents, and further studies are being carried out to optimize the performance of the entire system [16]–[20]. The control and protection strategies at the converter level are also discussed [21], [22].

Regarding the protection philosophies for the entire HVDC grid, most studies primarily concentrated on the quick identification of DC line faults [23]–[31] and the coordination of main and backup protections [32].

However, in terms of DC faults, the primary bottleneck is the long-period blocking activity, which will be deteriorated, especially taking into account the reclosure requirement for overhead line applications. Currently, there is little literature to discuss this aspect further.

The primary objective of this paper is to minimize the blocking duration of the fault-blocking converter based HVDC grids. In Section II, the protection requirements of an HVDC grid are discussed, then the system configuration and the basic characteristics of the key components are briefly introduced. In Section III, the fault feature of a fault-blocking converter based HVDC grid is analyzed and the convention-

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al protection scheme is presented. In Section IV, the optimized solution is proposed, which includes a control function to reduce the air deionization time and a coordination method to manage the fault reclosure issue. In Section V, the proposed strategies are verified by simulations. Finally, the conclusions are drawn in Section VI.

II. PROTECTION REQUIREMENTS OF HVDC GRID AND BENEFITS OF USING FAULT-BLOCKING CONVERTERS

A. Protection Requirements of HVDC Grids

Typically, the protection requirements of an HVDC grid can be classified into three protective levels (PLs).

1) Normal operation of critical equipment (PL1): the critical equipment of HVDC grids is normally composed of power electronic devices such as the converters and DCCBs, whose overcurrent withstanding capabilities are strictly limited. The ideal protection objective of an HVDC grid is to ensure that all converters should not be blocked before the fault is isolated. However, due to the high fault current rising rate in the HVDC grid, the protection threshold of the converter is normally reached in several milliseconds. To achieve the objective, it requires very fast fault detection, location, and isolation speed. The protection action usually has to be done within several milliseconds, which leads to the highest requirement for the protection system.

2) Stable operation of an HVDC grid (PL2): due to the limited performance of existing protection systems and devices, it is inevitable that some of the converters are already blocked before the fault is isolated in some scenarios. However, this result can be acceptable as long as the quantity of the blocked converters will not cause the outage of the entire HVDC grid. The blocked converters can also be de-blocked and resume operation once the fault is cleared. Compared with PL1, this level has lower requirements on the capability of the key equipment and the protection time can also be prolonged to ten milliseconds.

3) Stable operation of an alternation current (AC) system (PL3): an HVDC grid is normally embedded into an AC system. Under extreme conditions, all DC converters are blocked or unable to transmit power. This may cause a significant impact on the AC system. The outage of an HVDC grid is allowed but at least cannot cause the instability of the AC system. In other words, the AC system stability becomes the design criteria. This demand has the lowest requirement for protection speed, but often causes the worst consequences. Normally, such a PL could be used for a strong AC system with an embedded small-scale HVDC grid. However, as the influencing extent strongly depends on the outage time, to extend the feasible application scope of such a solution, it is an essential issue to reduce the blocking time of the converters.

B. System Configurations and Key Components

Figure 1 shows the diagram of a four-terminal parallel HVDC grid used for demonstration in this paper.

1) Configuration based on half-bridge based MMC (HB-MMC) and DCCB: according to the aforementioned three

PLs, both PL1 and PL2 need to isolate the fault within 10 ms, and the fast DCCB is the most feasible solution to realize this. In such a case, HB-MMCs can be used to reduce the overall equipment cost. The corresponding system configuration is shown in Fig. 1(a), where CS1-CS4 are MMC stations, T12, T24, T43, and T31 are overhead lines of the HVDC grid. The DC terminals of each converter station are connected with DC lines through three sets of DCCBs.

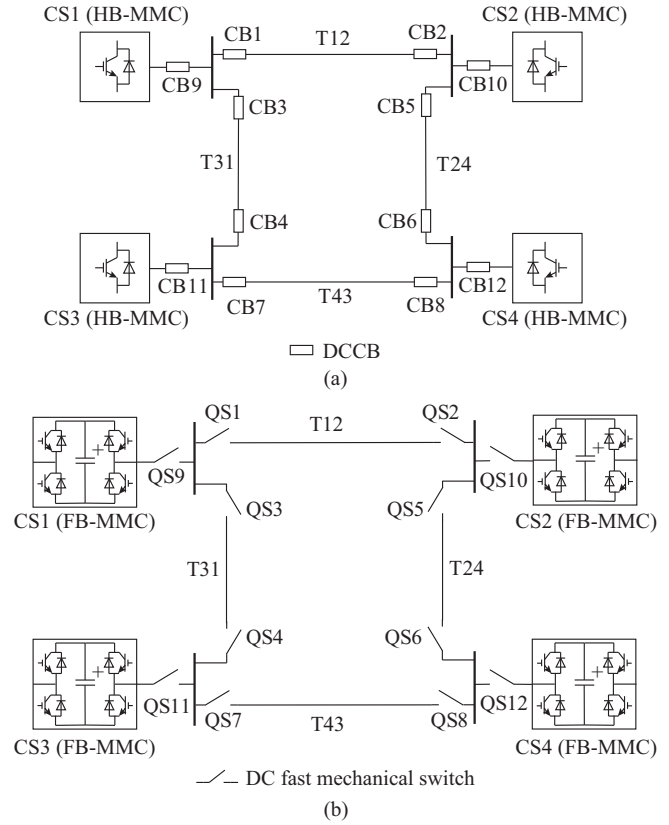


Fig. 1. Two kinds of configurations for HVDC grids. (a) Configuration based on HB-MMC and DCCB. (b) Configuration based on FB-MMC and fast DC mechanical switch.

Current feasible DCCB technologies include the mechanical type and the hybrid DCCB type which combines mechanical and semiconductor switches. This paper uses the hybrid DCCB as an example for demonstration, as shown in Fig. 2.

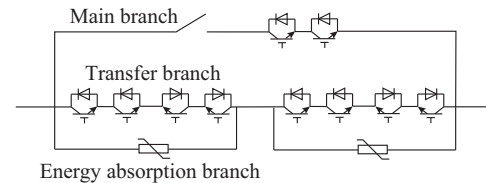


Fig. 2. Typical topology of hybrid DCCB.

2) Configuration based on full-bridge based MMC (FB-MMC) and fast DC mechanical switch: as mentioned above, PL3 has no technical requirement for cutting off large fault current in a short time. This can avoid the use of DCCBs which are normally expensive and not mature enough. However, the HB-MMC itself cannot cut off the fault current and

must rely on tripping the AC breaker. To avoid such a long fault clearance and restart time, another preferred choice which is consistent with PL3 is the configuration adopting fault-blocking converters. The system can realize the isolation of the AC and DC systems by blocking all the converters or transferring their control modes. Then, the fault line can be isolated by DC fast mechanical switches. The corresponding system configuration is shown in Fig. 1(b).

The key components related with fault clearance performance are the fault-blocking converters (CS1-CS4) and DC fast mechanical switches (QS1-QS12), which are briefly introduced below.

1) Fault-blocking Converters

Several topologies such as FB-MMC, hybrid MMC, alternate arm converter (AAC) have been proven able to realize the fault-blocking functionality [16]-[20]. Although their topologies and operation principles are different, the basic ideas used to deal with DC faults are similar, which is utilizing the negative voltage output capability of full-bridge submodules to block or control the fault current.

The blocking idea is straightforward. After blocking the converters, the fault current injected by the converters will be stopped immediately.

For the latter idea, the converter will reduce its DC voltage to zero instead of blocking the converter, to avoid further development of fault current. During this period, thanks to its negative voltage output capability, the AC voltage waveform can still be maintained and the converter can still provide reactive power for the AC grid.

For demonstration, the typical FB-MMC is used in this paper and its topology is shown in Fig. 3. As the working mechanism has been discussed in many studies [21], [22], it will not be presented in detail in this paper.

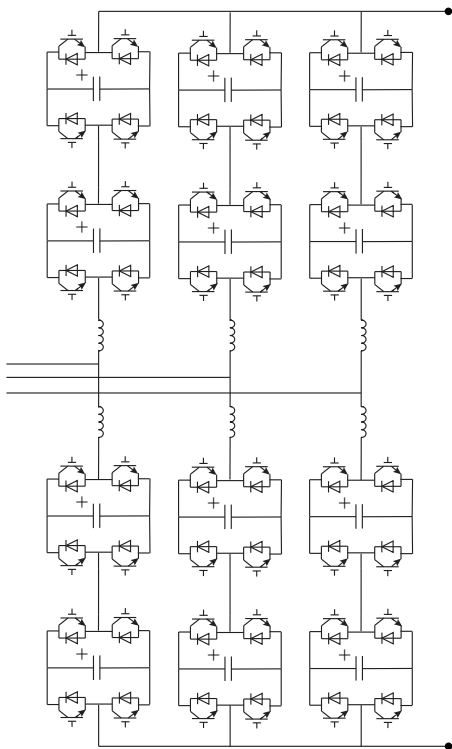


Fig. 3. Topology of FB-MMC.

2) DC Fast Mechanical Switches

The typical topology of a DC fast mechanical switch is shown in Fig. 4, where MOA stands for metal oxide arrester and CB stands for circuit breaker.

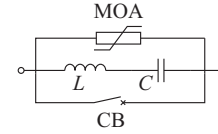


Fig. 4. Typical topology of DC fast mechanical switch.

The passive-type mechanical switch utilizes the instability and negative resistance characteristics of the arc to generate a self-excited oscillating current. A parallel conversion circuit (composed of a capacitor and a reactor) is connected across the device to cause the current to oscillate, thereby generating a zero-crossing point and forcing the zero-crossing current.

The topology of the switch is similar to those used in the neutral zone of conventional HVDC. However, the type used for an HVDC grid can withstand higher DC voltage during normal operation. Currently, the product reaching up to 200 kV has been applied in the Zhoushan five-terminal voltage source converter based HVDC (VSC-HVDC) project in China and a higher voltage rating is being further developed.

C. Technical Economy Comparison

For a quantitative description, this subsection gives a general technical economy comparison between HB-MMC with DCCB (Scheme 1) and FB-MMC with DC fast mechanical switches (Scheme 2).

The comparison is based on the four-terminal system and the detailed parameters are shown in Table I. For Scheme 1, the primary extra costs are introduced by the DCCBs, which are equipped at each terminal of the converter station. For Scheme 2, the primary costs are the DC fast mechanical switches and the extra semiconductors within the converters. It should be noted that there are two extra insulated gate bipolar transistors (IGBTs) for each full-bridge submodule.

TABLE I
ECONOMY COMPARISON BETWEEN SCHEME 1 AND SCHEME 2

Scheme	Item	Quantity	Single unit cost (M€)	Total cost (M€)
1	DCCB	12	10.5000	126.000
	Extra semiconductor	25920	0.0026	67.392
2	DC fast mechanical switch	12	0.2600	3.120

It can be seen that the extra cost of Scheme 1 is almost double that of Scheme 2. Furthermore, as other hybrid topologies for fault-blocking converters can further reduce the quantity of extra semiconductors, the cost of Scheme 2 can be further optimized.

However, it is obvious that the fault clearance performance of Scheme 1 is better than that of Scheme 2. It is also the target of this paper to promote the technical performance of Scheme 2.

III. FAULT FEATURE AND CONVENTIONAL PROTECTION SCHEME

A. Fault Features

During a DC pole-to-pole fault, the fault current is contributed by two sources. One is the energy released from overhead line, the other is the discharging current from converter stations, as shown in Fig. 5(a).

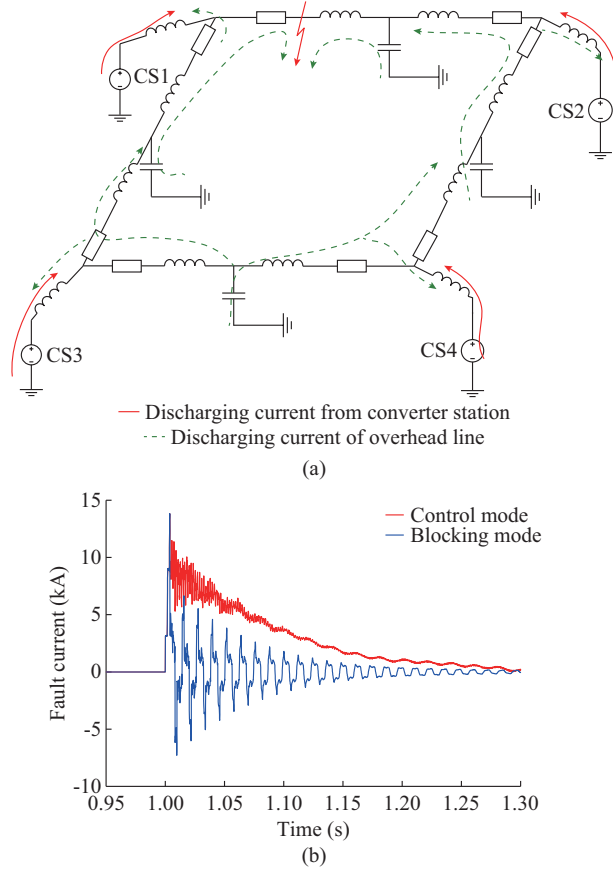


Fig. 5. Fault features for fault-blocking converter based HVDC grid. (a) Fault current sources. (b) Fault current waveforms.

The former will lead to a high-frequency oscillation current, which will be injected into the fault location. The converters can act as parallel branches to share this current with the fault location. This point can be seen as an advantage of active control compared with blocking the converters, as blocking will make the converters unable to share, thereby leading to much higher oscillation current into the fault location and hampering the air deionization, as shown in Fig. 5(b).

The fault currents contributed by converter stations are primarily caused by the discharge of internal capacitors. After the fault is detected, the converter reduces its DC output voltage to zero. The change of equivalent DC circuit configuration from the perspective of one converter station is illustrated in Fig. 6, where C_{eq} and U_0 are the equivalent capacitor of the converter and the initial voltage, respectively; L_{eq} and R_{eq} are the reactor and resistor of the equivalent circuit, respectively; i_{dc} is the fault current contributed by the converter; and T_0 is the time instant to reduce the DC voltage to zero.

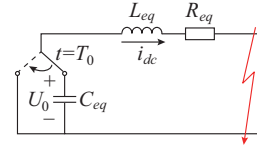


Fig. 6. Equivalent circuit of converter discharging process.

Before the DC voltage control is activated, the development of fault current is very close to that of HB-MMC. However, after blocking of the HB-MMC, the fault current is still continuously fed from the AC systems and will only decay after the AC breaker is tripped. For FB-MMC, AC output remains effectively controlled (even if the DC voltage is reduced to zero), thus it will only present a current decaying process on the DC side.

Based on the equivalent circuit above and assuming that the R_{eq} in the circuit is normally small, the fault current contributed by the converter can be expressed as:

$$i_{dc} = \begin{cases} I_0 + \frac{U_0}{\omega L_{eq}} e^{-\alpha t} \sin(\omega t) & t < T_0 \\ I_{T_0} e^{-\frac{t}{\tau}} & t > T_0 \end{cases} \quad (1)$$

where I_0 and I_{T_0} are the initial steady-state DC current and the DC current at the time instant T_0 , respectively; $\alpha = R_{eq}/(2L_{eq})$; $\omega = \sqrt{\omega_0^2 - \alpha^2}$, $\omega_0 = \sqrt{1/(L_{eq}C_{eq})}$; $\tau = L_{eq}/R_{eq}$.

To obtain the fault current distribution of the entire network, the calculation methods proposed for the HVDC grid in many studies are applicable and will not be presented in detail in this paper [33], [34].

It can be observed that the decay of fault current will normally take a lot of time and delay the fault clearance, which is an important issue to be managed.

B. Conventional Protection Sequence

Taking a fault on line T12 as an example, the overall protection sequence based on fault-blocking converters is as follows (only a one-time restart is considered).

t_1 : fault occurs.

t_1 - t_2 (several milliseconds): the fault needs to be detected quickly by the protection system, and converters need to be controlled to reduce the DC voltage.

t_2 - t_3 (several hundred milliseconds): waiting for the delay of fault current and air deionization.

t_3 - t_4 (tens of milliseconds): the DC voltages of the converters are gradually increased to restart the system. The system is restarted successfully if the DC voltage has been established and then the converter power can be gradually restored to normal operation.

t_4 - t_5 (several hundred milliseconds): if the DC voltage has not been successfully re-established, the voltage control needs to be re-activated and wait for the decay of fault current.

t_5 - t_6 (tens of milliseconds): faulty line is tripped by DC fast mechanical switches. Then the system can recover to another operation state.

The state signals of the main equipment during the entire

process are shown in Fig. 7. The duration of power interruption could reach several hundred milliseconds or even above 1 s, due to the requirement of twice air deionization. This strongly limits the performance of the entire system. To reduce the subsequent impact and accelerate the system recovery, it is essential to propose an optimized recovery strategy.

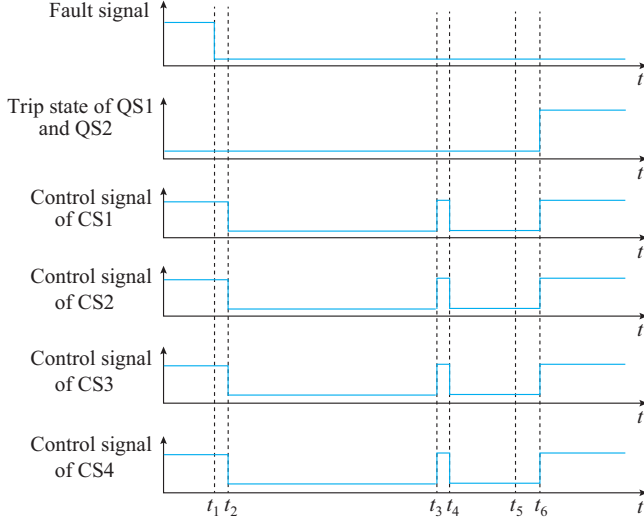


Fig. 7. State signals of main equipment during entire process.

IV. PROTECTION COORDINATION STRATEGY OPTIMIZATION

A. Acceleration of Air Deionization

It is observed that the long fault clearance time is caused by the decay of discharging current of capacitors. The decaying time relates to the resistance and reactance in the current loop, which cannot be practically controlled.

To accelerate the decaying process, the most efficient way is to utilize the active control capability of the converters. Different from the HB-MMC, the FB-MMC is capable of generating negative voltage. The basic idea is that by involving an extra voltage source, a reverse current can be generated to compensate the fault current, the equivalent circuit of which is shown in Fig. 8.

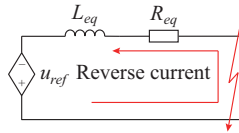


Fig. 8. Equivalent circuit after inserting negative voltage.

To generate negative voltage of the appropriate value, a controller comparing the DC terminal current with its reference value can be designed as follows:

$$u_{ref} = \left(K_p + \frac{K_i}{s} \right) (i_{ref} - i_{dc}) \quad (2)$$

where u_{ref} is the reference order of the negative voltage generated by the converter; K_p and K_i are the proportional and integral coefficients of the proportional-integral (PI) controller, respectively; and i_{ref} is the reference order of the DC current i_{dc} .

It is complex to obtain the detailed response of a fault current under the input of a four-terminal voltage source. However, it can be foreseen that the fault current is primarily influenced by the converter stations close to the fault location, thus a proximate calculation can be done by neglecting the contribution of remote stations and long circuit loops. The equivalent circuit can be simplified as Fig. 9. In Fig. 9, L_1 and L_2 are the arm reactors in the converters for CS1 and CS2, respectively; R_{f1} and R_{f2} are the equivalent resistors of the overhead line section from the faulty point to the DC terminal of converter station; L_{f1} and L_{f2} are the equivalent reactors of the overhead line section from the faulty point to the DC terminal of converter station; u_{CS1} and u_{CS2} are the equivalent DC voltages of CS1 and CS2, respectively; i_1 and i_2 are the fault currents measured at DC terminal of CS1 and CS2, respectively; i_{f1} and i_{f2} are the fault currents flowing along the overhead line connected to CS1 and CS2, respectively; and i_f is the fault current injected to the earth.

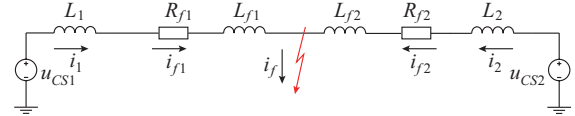


Fig. 9. Equivalent circuit after simplification.

The fault current contributed by CS1 can be expressed as:

$$\begin{cases} i_{f1}(s) = \frac{u_{CS1}(s)}{L_{1\Sigma}s + R_{f1}} = \frac{\left(K_p + \frac{K_i}{s} \right) (i_{ref}(s) - i_{f1}(s))}{L_{1\Sigma}s + R_{f1}} \\ i_{ref}(s) = \frac{K_p s + K_i}{L_{1\Sigma}s^2 + (R_{f1} + K_p)s + K_i} \end{cases} \quad (3)$$

where $L_{1\Sigma} = L_1 + L_{f1}$.

Similarly,

$$\frac{i_{f2}(s)}{i_{ref}(s)} = \frac{K_p s + K_i}{L_{2\Sigma}s^2 + (R_{f2} + K_p)s + K_i} \quad (4)$$

where $L_{2\Sigma} = L_2 + L_{f2}$.

Then, the fault current can be expressed as:

$$\frac{i_f(s)}{i_{ref}(s)} = \frac{K_p s + K_i}{L_{1\Sigma}s^2 + (R_{f1} + K_p)s + K_i} + \frac{K_p s + K_i}{L_{2\Sigma}s^2 + (R_{f2} + K_p)s + K_i} \quad (5)$$

The above result is based on the assumption that the converter stations are adopting the same control function and gains. According to (4), it can be seen that the fault current can be effectively controlled without static error.

B. Optimization of Recovery Sequence

As mentioned previously, whether the fault is cleared can be judged by re-establishing the DC voltage at a pre-determined value. Moreover, as each converter can independently complete the task, it is able to select only a single converter to distinguish the fault and this is helpful in reducing the extent of the impact on the entire grid.

Taking the fault on line T12 as an example, the state signals of the equipment are shown in Fig. 10(b), and the pro-

posed sequence is as follows.

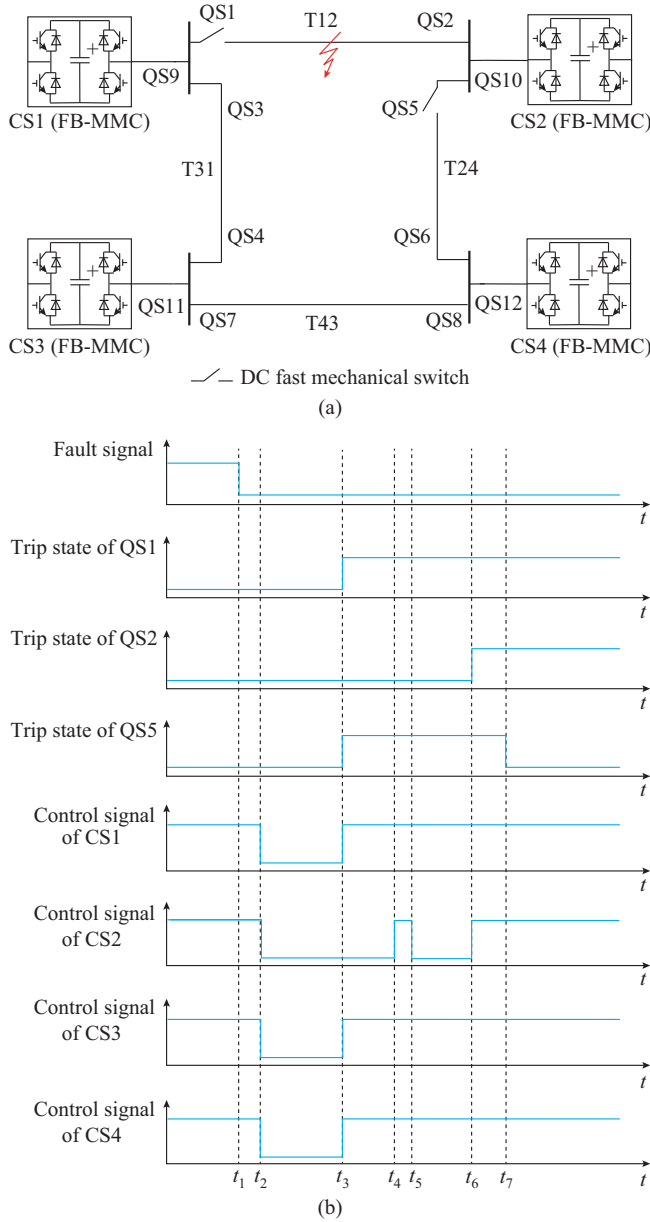


Fig. 10. Circuit during fault isolation and recovery and optimized protection sequence. (a) Circuit during fault isolation and recovery. (b) State signals of main equipment.

t_1 : the fault occurs.

t_2 : four converter stations are actively controlled.

t_3 : fault current is controlled within a certain level and DC fast mechanical switches QS1 and QS5 are opened. Simultaneously, CS1, CS3, and CS4 are deblocked and recover normal operation.

t_4 – t_5 : CS2 attempts to re-establish the DC voltage. If no protection action occurs, the fault is identified to be temporary. Then, QS1 and QS5 can be closed to reconnect CS2 with the other stations. Otherwise, CS2 will be actively controlled again.

t_6 : after the fault current decays, the DC fast mechanical switch QS2 is opened.

t_6 – t_7 : CS2 controls its DC voltage to its rated level.

t_7 : QS5 is reclosed to connect CS2 with the other stations.

It can be seen from Fig. 10(b) that the optimized recovery strategy avoids the long-term overall power interruption. Most of the converters can be deblocked quickly and this reduces the system stability risk caused by the power interruption compared with the conventional strategies.

V. SIMULATION VERIFICATION

To verify the proposed protection strategies, the four-terminal meshed HVDC grid model with FB-MMCs and DC fast mechanical switches is established in PSCAD/EMTDC.

In the model, the AC systems are equivalent ideal voltage sources with an impedance shown in Table II. The details of converter parameters are shown in Table III. The DC overhead lines adopt frequency-dependent models, and the parameters of DC overhead lines are shown in Table IV.

TABLE II
MAIN PARAMETERS OF AC SYSTEMS

Item	Value
AC system voltage V_s (kV)	500
Equivalent inductance L_s (mH)	18
Equivalent resistance R (Ω)	0.9

TABLE III
MAIN PARAMETERS OF CONVERTER STATIONS

Item	Value			
	CS1	CS2	CS3	CS4
Nominal capacity (MVA)	1600	1600	3200	3200
Transformer ratio	1.05	1.05	1.05	1.05
Transformer reactance (p.u.)	0.15	0.15	0.15	0.15
Rated DC voltage (kV)	± 500	± 500	± 500	± 500
Arm inductance (mH)	50	50	50	50
Rated voltage of submodule (kV)	2	2	2	2
Submodule quantity per arm	540	540	540	540
Capacitance of submodule (μ F)	8000	8000	3200	3200

TABLE IV
MAIN PARAMETERS OF DC OVERHEAD LINES

Overhead line	Length (km)	DC resistance (Ω /km)
T12	500	0.0135
T23	400	0.0135

The DC voltage of entire HVDC grid is controlled by CS4 whereas all the other converter stations (CS1–CS3) operate in active power control mode whose values are set as +1.0, –1.0, and +0.5 p.u., respectively (positive means operating as a rectifier).

A. Case 1: Conventional Protection Sequence

As shown in Fig. 11, a permanent pole-to-pole fault is applied in the middle of the line T12 at $t_1 = 1$ s. As the waveforms of all stations are similar, the waveforms of CS1 and CS2 are presented in Fig. 11. In Fig. 11, E_{dep1} , E_{den1} , E_{dep2} , E_{den2} are the positive and negative DC voltages measured at

DC terminals of CS1 and CS2, respectively.

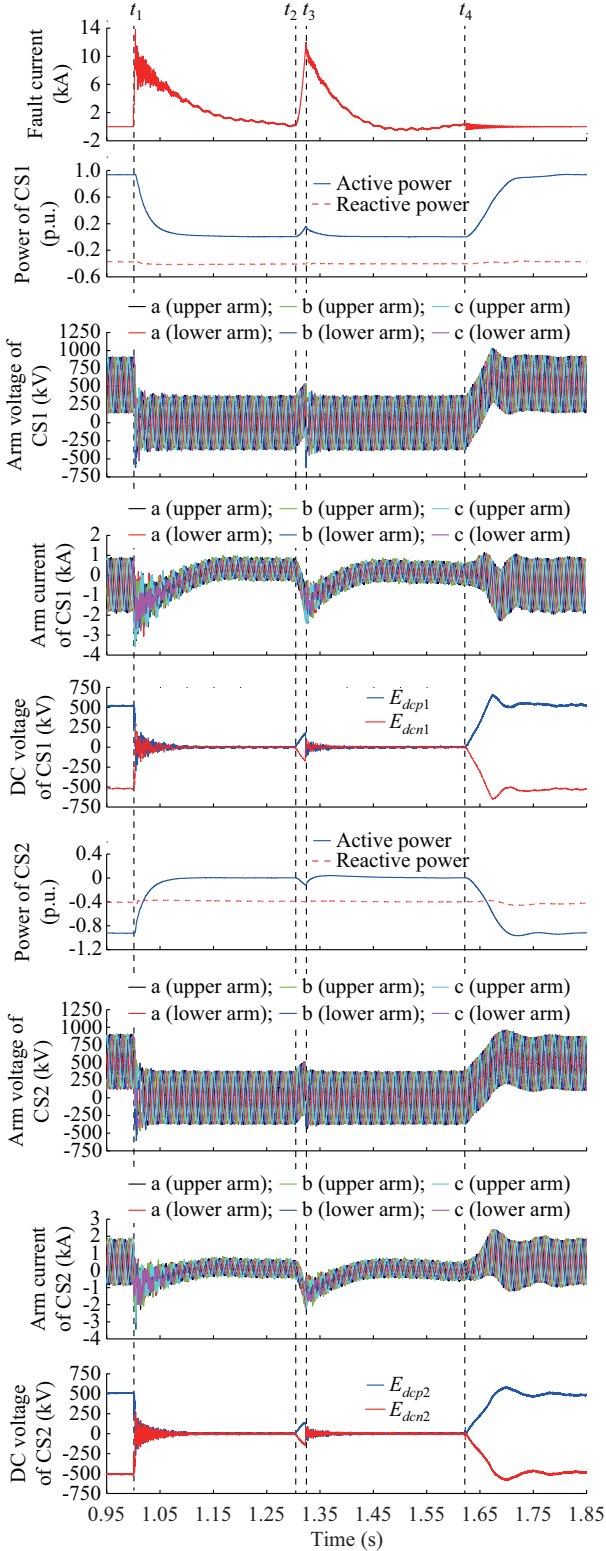


Fig. 11. Waveforms of a conventional protection scheme under a permanent fault.

The protection system detects the fault in 3 ms after the fault occurrence and immediately reduces the DC voltage.

After that, the DC current starts to slowly decay and after almost 300 ms, it is close to zero and the air deionization is

deemed to be completed.

It is observed that during this period, the converters can still generate 0.4 p.u. reactive power to the AC system. Additionally, the high-frequency oscillation current appears in all bridge arms of each converter station, sharing the discharging current of overhead lines with the fault point, which accelerates the decay of high-frequency current.

At 1.3 s, the converter stations try to recover the DC voltage gradually but fails at 1.32 s, as high impulse current presents again. The converters implement the active voltage control once more after another 300 ms, and the switches QS1 and QS2 are opened as the fault is identified as permanent. Then, the converter stations can be quickly recovered to normal operation. It is observed that nearly 600 ms of power interruption occurs due to the fault. This is not acceptable for an HVDC grid and may cause the instability of the corresponding AC system.

B. Case 2: Optimized Protection Sequence

Waveforms based on the optimized solution are given in Fig. 12, where E_{dep3} , E_{dep3} , E_{dep4} , E_{dep4} are the positive and negative DC voltages measured at DC terminals of CS3 and CS4, respectively. The fault occurs at 1.0 s. After 3 ms, the DC voltage is controlled to be zero and to further suppress the fault current, and a certain opposite DC voltage is generated by the extra current controller, as shown in Fig. 12(c), (d), (e), (f). Thanks to these current-driven DC voltages, the fault current decreases to zero within 50 ms.

With QS1 and QS5 opened, the CS2 can perform the fault distinguishing activity independently. However, after the failure of restart, the fault is deemed as permanent, then the QS2 is opened at t_6 . The CS1, CS3, and CS4 can be quickly recovered to normal operation after the fault is isolated by the switches QS1 and QS5 at $t_3 = 1.07$ s, assuming that mechanical switches can be opened in 20 ms.

During t_6 and t_7 , a certain time is reserved between the open of QS2 and the close of QS5. The period is used for the re-establishment of DC voltage of CS2, thus it can connect with the other stations without significant disturbance.

During the entire process, the power interruption of CS1, CS3, and CS4 only lasts within 100 ms. The CS2 can also recover to normal power transmission within 400 ms after the fault. When CS2 is absent from the grid, the power balance is maintained by CS4, absorbing the power injected by both CS1 and CS3. After CS2 is reconnected and participates in the power balance, the power level of CS4 recovers to a normal state.

To demonstrate the effectiveness of the current controller further, the main parameters of the case are substituted in (4) to obtain a quantitative calculation result of the fault current, which is then compared with the simulation results.

The calculated results are shown in (6), where $K_p = 50$, $K_i = 1000$, $R_{f1} = R_{f2} = 4.43 \Omega$, $L_{1\Sigma} = L_{2\Sigma} = 0.3$ H. It should be noted that the resistance is mainly contributed by the overhead line, while the reactance is contributed by both the overhead line and converter reactors.

$$\frac{i_f(s)}{i_{ref}(s)} = 2 \times \frac{50s + 1000}{0.3s^2 + (4.43 + 50)s + 1000} \quad (6)$$

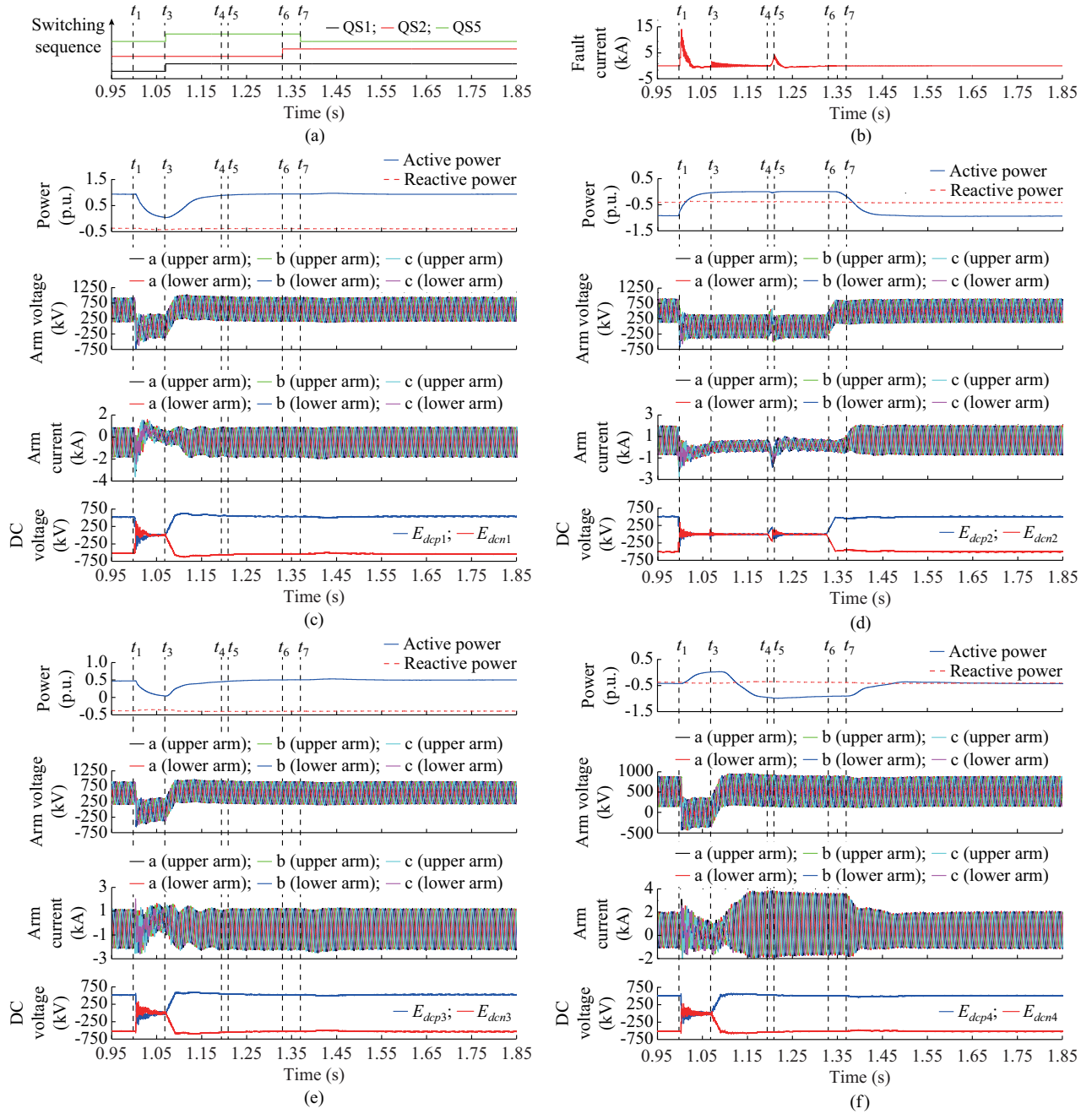


Fig. 12. Waveforms of optimized protection scheme under a permanent fault. (a) Switching sequences of QS1, QS2, and QS5. (b) Fault current. (c) Waveforms of CS1. (d) Waveforms of CS2. (e) Waveforms of CS3. (f) Waveforms of CS4.

Based on (5), the calculation and simulation results are constructed in Fig. 13. The simulation results are composed of both high-frequency and low-frequency components. Besides the high-frequency components, it is observed that the main trend is similar between the calculation and simulation results, which can prove the effectiveness of the current controller.

VI. CONCLUSION

Aimed at improving the DC fault performance for the HVDC grid based on fault-blocking converter, the optimized protection strategies with special consideration on the reclosure issue are proposed in this paper.

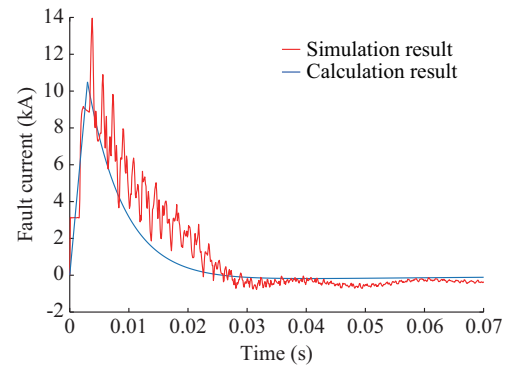


Fig. 13. Comparison between calculation and simulation results.

Based on the proposed current damping control strategy, the decay of fault current can be accelerated and controlled within 50 ms. Combined with the proposed fault reclosure methodology, most converters can be isolated from the fault and recovered to normal operation within 100 ms, leading to less impact on the HVDC grid and AC system.

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