A DC Chopper Topology to Mitigate Commutation Failure of Line Commutated Converter Based High Voltage Direct Current Transmission

Chunyi Guo, Bo Liu, and Chengyong Zhao

***Abstract*—To reduce the probability of commutation failure (CF) of a line commutated converter based high-voltage direct current (LCC-HVDC) transmission, a DC chopper topology composed of power consumption sub-modules based on thyristor full-bridge module (TFB-PCSM) is proposed. Firstly, the mechanism of the proposed topology to mitigate CF is analyzed, and the working modes of TFB-PCSM in different operation states are introduced. Secondly, the coordinated control strategy between the proposed DC chopper and LCC-HVDC is designed, and the voltage-current stresses of the TFB-PCSMs are investigated. Finally, the ability to mitigate the CF issues and the fault recovery performance of LCC-HVDC system are studied in PSCAD/EMTDC. The results show that the probability of CF of LCC-HVDC is significantly reduced, and the performances of fault recovery are effectively improved by the proposed DC chopper.**

***Index Terms*—Line commutated converter based high-voltage direct current (LCC-HVDC) transmission, DC chopper, power consumption sub-module based on thyristor full-bridge module (TFB-PCSM), commutation failure (CF), fault recovery capability.**

I. Introduction

LINE commutated converter based high-voltage direct current (LCC-HVDC) transmission is widely utilized for bulk-power and long-distance transmission [1]. However, due to the utilization of the thyristors, commutation failure (CF) may occur when the AC busbar voltage drops due to disturbances, which will deteriorate the system transient stability, increase the DC current, reduce the operation life of the converter valve and bring risks to the normal operation of the system [2], [3].

Currently, the solutions to mitigate CF can generally be classified into three categories: ① the improvement of control system; ② the utilization of reactive power compensators to regulate the AC bus voltage; ③ the enhancement of the converter topology.

As for control system improvement, [4] presents a DC predictive control strategy to mitigate CF. Reference [5] uses the *abc*-$\alpha\beta$ transformation and zero-sequence voltage for detection of three-phase and single-phase faults. In [6], by advancing the firing angle at the inverter after detection of AC voltage disturbance, a larger commutation margin can be provided. However, the advancement of the firing angle will increase reactive power consumption. Another commonly used method is the voltage dependent DC order limiter (VDCOL). However, the change of current order is restricted by communication delay. Reference [7] presents an improved current order limiter control and a power-component detection (PCD) method to mitigate CF, but it is difficult to select the introduced parameters.

The utilization of reactive power compensators to regulate the AC bus voltage can deduce the CF probabilities of LCC-HVDC systems. In China Southern Power Grid, the static synchronous compensator (STATCOM) devices have been installed close to LCC-HVDC links to regulate the AC voltage and improve the CF immunity. In State Grid Corporation of China, the transmission operators adopt synchronous condenser (SC) devices to mitigate the CF probability for several LCC-HVDC projects. References [8] and [9] study the CF mitigation effects by static var compensator (SVC), STATCOM and SC. However, it will increase the capital cost by installing additional reactive power compensators.

Some enhanced converter topologies with additions of capacitive component electronic devices are also proposed to mitigate CF [10] - [13]. A capacitor commutated converter (CCC) can offer an improved power factor and lower CF probability [10]. However, the voltage stress of the converter valve will increase because of the inserted capacitors. Reference [11] studies the controlled series capacitor converter (CSCC), which connects the capacitors in series between the AC bus and the converter transformer. However, the harmonic characteristics of this topology are complex. In [12], a LCC-HVDC system with controllable capacitors is proposed. But there is a power rating mismatch issue between insulated gate bipolar transistors (IGBTs) in the controllable capacitors and thyristors in the converter valve. Recently, an evolved capacitor commutated converter (ECCC) embedded with an anti-parallel thyristor based dual-directional full-bridge module (APT-DFBM) is proposed in [13], which can

Manuscript received: May 16, 2019; accepted: November 21, 2019. Date of CrossCheck: November 21, 2019. Date of online publication: March 9, 2020.

This work was supported by National Natural Science Foundation of China (No. 51877077).

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DOI: 10.35833/MPCE.2019.000327

effectively reduce CF risks of LCC-HVDC and improve the dynamic responses of CCC-HVDC, but the coordinated control becomes more complex.

In [14], a DC chopper is used to suppress the DC-side over-voltage by consuming the power transmitted from the rectifier. Similarly, DC current can also be reduced by the utilization of a DC chopper to consume the real power under fault conditions, which could be an option to reduce the CF probability. In this paper, a DC chopper topology composed of power consumption sub-modules based on thyristor full-bridge module (TFB-PCSM) is proposed, which is installed at the DC terminal of the inverter station, and can reduce the DC current and enhance the CF immunity of a LCC-HVDC system. Then, the coordinated control strategy between the proposed DC chopper and LCC-HVDC is presented and the voltage-current stresses of the TFB-PCSMs are investigated. Finally, the effectiveness of the proposed DC chopper is validated by various simulations in PSCAD/EMTDC. By comparing the dynamic responses of LCC-HVDC, CCC-HVDC and the proposed method under fault conditions, it can be concluded that the probability of CF is significantly reduced, and the fault recovery performances are effectively improved by the proposed DC chopper.

The rest of the paper is organized as follows. Section II presents the DC chopper topology composed of TFB-PCSM. Section III presents the coordinated control strategy and introduces the working modes of TFB-PCSM in different operation states. Section IV presents the parameter selection approach of TFB-PCSM. Section V investigates the dynamic performances of LCC-HVDC with the proposed DC chopper topology. Section VI concludes the paper.

II. Circuit Configuration of DC Chopper

A. Proposed Configuration of DC Chopper

Figure 1(a) shows the structure of the LCC-HVDC system.

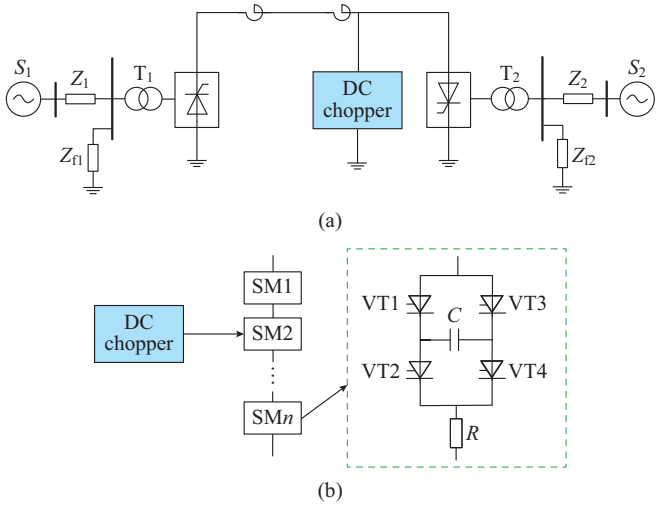

Fig. 1. System configuration. (a) LCC-HVDC. (b) TFB-PCSM.

In Fig. 1(a), S_1 and S_2 are the equivalent sources for AC systems; Z_1, Z_2, Z_{f1}, Z_{f2} are the equivalent impedances for AC systems and filters, respectively; and T_1 and T_2 are the transformers. The DC chopper is connected in parallel with the DC terminal of the inverter, consisting of a certain number of TFB-PCSMs. Figure 1(b) shows the configuration of one TFB-PCSM module. In Fig. 1(b), C is the capacitor; R is the resistor; SMn is the sub-module; and each thyristor element VTi (i=1, 2, 3, 4) can also be a unit with a certain number of series-connected thyristors.

B. Mechanism of DC Chopper to Mitigate CF

In an LCC-HVDC system, according to Kirchhoff's voltage law and Kirchhoff's current law, the commutation process can be written as:

$$L_{\mathrm{r}}\frac{\mathrm{d}i_{\mathrm{op}}(t)}{\mathrm{d}t}-L_{\mathrm{r}}\frac{\mathrm{d}i_{\mathrm{cl}}(t)}{\mathrm{d}t}=\sqrt{2}\,U_{\mathrm{L}}\sin\omega t \tag{1}$$

$$i_{\mathrm{op}}(t)+i_{\mathrm{cl}}(t)=I_{\mathrm{d}} \tag{2}$$

where $i_{\mathrm{op}}(t)$ and $i_{\mathrm{cl}}(t)$ are the on-going current and off-going current of the valve, respectively; U_{L} is the root-mean-square (RMS) value of commutation voltage; L_{r} is the commutation inductor; ω is the angular frequency; and I_{d} is the DC current.

From (1) and (2), I_{d} and γ can be obtained as:

$$I_{\mathrm{d}}=\frac{\sqrt{2}\,U_{\mathrm{L}}}{2\omega L_{\mathrm{r}}}(\cos\gamma-\cos\beta) \tag{3}$$

$$\gamma=\arccos\left(\frac{2\omega L_{\mathrm{r}}I_{\mathrm{d}}}{\sqrt{2}\,U_{\mathrm{L}}}+\cos\beta\right) \tag{4}$$

where γ is the extinction angle; and β is the advanced firing angle. As can be seen from (4), the extinction angle is influenced by the AC voltage, the DC current, the commutation reactor and the firing angle. When the AC voltage of the system descends, the DC current rises or the firing angle decreases, γ will decrease, which may cause CF of the inverter. When a fault occurs, the DC chopper can be put into use to reduce the DC current, which can increase an extra margin for the extinction angle, thus reducing the probability of CF.

When the system operates normally, the thyristors in the DC chopper are all in the off-state, and there is no current passing through the resistor. When a fault occurs, the thyristors in the DC chopper can be controlled following the strategy in Section III, and the current will flow through the resistor, which can reduce the DC current by consuming power and improve the CF immunity.

III. Coordinated Control Strategy of DC Chopper

The core of the control strategy in the DC chopper is as follows. When the system operates normally, the thyristors in TFB-PCSM are all turned off, the resistor is not put into operation and the capacitor is bypassed. When a fault is detected, the resistor in TFB-PCSM will be put into operation, thus the DC current during the fault can be reduced to a certain extent through power consumption. Therefore, the probability of CF of the inverter can be reduced. The approaches for fault detection can adopt the methods in [5] such as the *abc*-$\alpha\beta$ transformation for three-phase fault detection and the zero-sequence voltage for single-phase fault detection. Fig-

ure 2 shows the current paths of TFB-PCSM by the arrow and the bold thyristors in 6 different modes, when the current flows through the TFB-PCSM. The other modes without current flow, i.e., all the thyristors of TFB-PCSMs are in the off-state, are not shown. Table I shows the working state of the four groups of thyristors in TFB-PCSM, where "1" means the valve is in the on-state and "0" means the valve is in the off-state. The polarities of the capacitors in modes 1, 2, 3 and modes 4, 5, 6 are opposite. When the TFB-PCSM works in modes 1 and 4, the capacitor voltage is charged; when in modes 2 and 5, the system operates normally; when in modes 3 and 6, the DC chopper is consuming power. In the following section, the control strategy is introduced for modes 1, 2 and 3. Similar analysis can also be readily obtained for modes 4, 5 and 6.

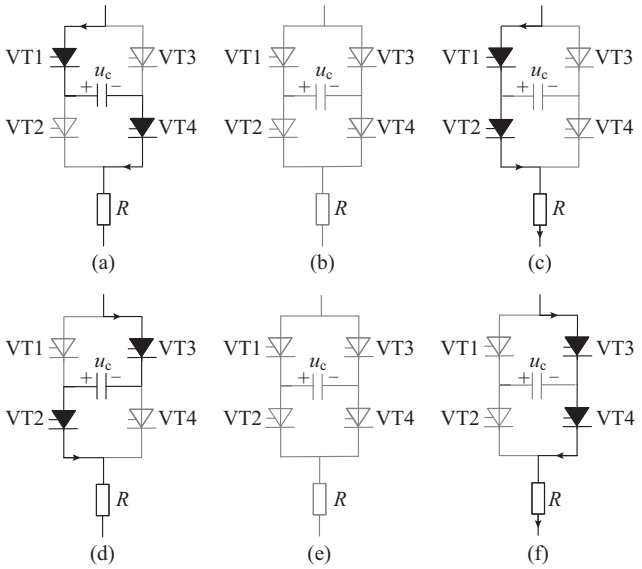

Fig. 2. Current path of TFB-PCSM. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6.

TABLE I
CONDUCTION MODE OF TFB-FBSM

Mode	VT1	VT2	VT3	VT4	Working state
1	1	0	0	1	Charging state
2	0	0	0	0	Normal operation
3	1	1	0	0	Power consumption
4	0	1	1	0	Charging state
5	0	0	0	0	Normal operation
6	0	0	1	1	Power consumption

The coordinated control approach of TFB-PCSMs in the DC chopper and converter arms includes: ① charging control of TFB-PCSMs; ② normal operation control under a steady-state condition; ③ power consumption control under fault conditions. The detailed coordinated control approach is illustrated as follows.

A. Charging Control of TFB-PCSMs

During the start-up process of the LCC-HVDC system, the capacitors of TFB-PCSMs are required to be precharged. As shown in Fig. 2(a), by triggering VT1 and VT4, the capacitor is charged, and TFB-PCSM works in mode 1. During this process, the current flows through VT1, the capacitor, and VT4. The resistor capacitor voltage is positive. When the sum of the capacitor voltages in all the TFB-PCSMs of the DC chopper is equal to the DC voltage, the charging process will be completed and the current will no longer flow through the capacitor. VT1 and VT4 will be turned off due to no current passing through the loop.

B. Normal Operation Control Under Steady-state Condition

When the system operates normally, VT1-VT4 are all in the off-state and TFB-PCSM works in mode 2, as shown in Fig. 2(b). No current is flowing through the resistor, thus the DC chopper will not consume the real power.

C. Power Consumption Control of TFB-PCSMs

When the AC fault occurs at the inverter side, the resistor is required to consume power to reduce the DC current, and the power consumption control can be activated by an AC fault detect [5]. As shown in Fig. 2(c), VT1 and VT2 are triggered and the TFB-PCSM works in mode 3. Then, the current flows through VT1, VT2 and the resistor in turn. Due to the power consumption, the DC current is reduced, thus the CF probability is also reduced. In this working state, the capacitor is bypassed.

Note that three factors need to be considered when blocking the power consumption branch: ① since LCC-HVDC takes a 6-pulse converter as a basic unit and its commutation period for one 6-pulse unit is one cycle (0.02 s), the DC chopper power consumption branch plays the most significant role in the first cycle after the fault; ② the DC chopper should not over-consume DC power and interfere with the power recovery of the LCC-HVDC system, thus the power consumption time should not be too long; ③ the main protection of high-voltage lines generally operates within 20-25 ms to isolate the fault [15], which leaves a feasible time-window for the DC chopper to be put into use. Considering the above three factors, the recommended power consumption time is 0.02 s. As shown in Fig. 2(c), when the power consumption branch is required to be blocked, VT3 is triggered. When VT3 is turned on, VT1 will be turned off gradually by the reverse bias voltage of the capacitor. In this stage, the capacitor of the TFB-PCSM will be charged reversely. Finally, the polarity of the capacitor voltage will be reversed as shown in Fig. 2(d). When the sum of the capacitor voltages in all the TFB-PCSMs of the DC chopper is equal to the DC voltage, the reversed charging process is finished, and VT2 and VT3 are turned off due to no current passing through the loop. Finally, the system returns to its normal operation state, i.e., mode 5 as shown in Fig. 2(e).

In addition, due to the symmetrical structure of the TFB-PCSM, there are two ways (mode 3 or mode 6) to consume power. The selection of mode 3 or mode 6 is determined by the capacitor voltage polarity. If the system operates normally in mode 2 and the polarity of the capacitor voltage is positive, VT1 and VT2 will be triggered and TFB-PCSM works in mode 3 to consume power. Similarly, if the system operates normally in mode 5, the polarity of the capacitor volt-

age is reversed, VT3 and VT4 will be triggered and TFB-PCSM works in mode 6 to consume power as expected.

IV. Theoretical Analysis and Parameter Selection for TFB-PCSM in DC Chopper

The success of the proposed method depends on the selection of parameters including resistor value, capacitor value and thyristor types. In this section, the parameter selection approaches for resistor and capacitor values are given and the voltage-current stresses are analyzed to select the suitable thyristor types.

A. Selection of Resistors in TFB-PCSMs

The resistor R of the TFB-PCSM has a great influence on the effect of CF mitigation. When R is small, the current flowing through the resistor is relatively large and may exceed the current limit of the thyristors. When R is large, the current flowing through the resistor is relatively small, thus the amount of power consumption is reduced which weakens the CF mitigation effect. Therefore, it is quite important to choose a proper resistor size. An approach to select the resistor is given below.

Assuming a three-phase grounding fault occurs at the AC busbar at the inverter side, the commutation voltage is reduced to U_{L}', the corresponding DC voltage is U_{d}', DC current is I_{d}', and the extinction angle changes to γ'. Considering that there is a certain delay in the control system, β is kept constant for a very short time after the fault. The dynamic equations during this period can be written as:

$$I_{\mathrm{d}}' = \frac{\sqrt{2}\,U_{\mathrm{L}}'}{2\omega L_{\mathrm{r}}}(\cos\gamma' - \cos\beta) \tag{5}$$

$$\frac{I_{\mathrm{d}}'}{I_{\mathrm{d}}} = \frac{U_{\mathrm{L}}'}{U_{\mathrm{L}}}\frac{\cos\gamma' - \cos\beta}{\cos\gamma - \cos\beta} \tag{6}$$

Since the transient real power delivered from the rectifier side during the very short period after fault does not have big differences compared to that before the fault, the following equation can be obtained:

$$\frac{I_{\mathrm{d}}}{I_{\mathrm{d}}'} = \frac{U_{\mathrm{d}}'}{U_{\mathrm{d}}} \tag{7}$$

$$U_{\mathrm{d}} = \frac{3\sqrt{2}}{2\pi}U_{\mathrm{L}}(\cos\gamma + \cos\beta) \tag{8}$$

$$\frac{U_{\mathrm{d}}'}{U_{\mathrm{d}}} = \frac{U_{\mathrm{L}}'}{U_{\mathrm{L}}}\frac{\cos\gamma' + \cos\beta}{\cos\gamma + \cos\beta} \tag{9}$$

where U_{d} is the DC voltage of the system.

By solving (5)-(9), the relationship of the DC voltage and extinction angle can be obtained as:

$$\frac{U_{\mathrm{d}}'}{U_{\mathrm{d}}} = \sqrt{\frac{\cos\gamma' + \cos\beta}{\cos\gamma' - \cos\beta}\frac{\cos\gamma - \cos\beta}{\cos\gamma + \cos\beta}} \tag{10}$$

When the extinction angle is less than its allowable minimum value of $\gamma_{\min}$, CF will occur. Taking $\gamma' = \gamma_{\min} = 7°$ into (10), the critical DC voltage U_{d}' when CF occurs can be obtained.

The selection principle of R is:

$$R = \frac{U_{\mathrm{d}}'}{I_{\mathrm{d}}''} \tag{11}$$

where I_{d}'' is the allowable overcurrent for a short period, and 1.5 times of the rated current is adopted for I_{d}'' in this paper.

Assuming that DC chopper adopts n TFB-PCSMs, by solving (10) and (11), the resistor in one module can be obtained as:

$$R = \frac{1}{n}\sqrt{\frac{\cos\gamma' + \cos\beta}{\cos\gamma' - \cos\beta}\frac{\cos\gamma - \cos\beta}{\cos\gamma + \cos\beta}}\frac{U_{\mathrm{d}}}{1.5I_{\mathrm{d}}} \tag{12}$$

B. Selection of Capacitors in TFB-PCSMs

The aim of the capacitor in the TFB-PCSM is to force certain thyristors to turn off reliably during the blocking process of the power consumption branch. As shown in Fig. 2(c) and (d), taking mode 3 and mode 4 as an example, when the power consumption branch is required to be blocked, VT3 is triggered. When VT3 is turned on, VT1 will be turned off gradually by the reverse bias voltage of the capacitor. If the reverse blocking recovery time of the thyristor is t_{rr} and the forward blocking recovery time is t_{gr}, the total turn-off time t_{q} of the thyristor is the sum of t_{rr} and t_{gr}. The time constant τ of the capacitor-resistor branch is equal to RC. When the discharging time t of the capacitor is larger than 4τ, it can be considered that the capacitor voltage roughly drops to 0. Assume that when the capacitor voltage drops to 0, VT1 will be turned off. Given t_{q} and R, the capacitor size C can be obtained as:

$$t_{\mathrm{q}} = t_{\mathrm{rr}} + t_{\mathrm{gr}} = 4RC \tag{13}$$

C. Selection of Thyristors in TFB-PCSMs

To select the thyristors in TFB-PCSMs, it is necessary to analyze the voltage-current stresses of the thyristors in different operation states. The parameters of the TFB-PCSM need to be reasonably designed so that the voltage-current stresses are within the allowable range.

1) Voltage Stress of TFB-PCSMs

When the TFB-PCSM works in modes 1, 3, 4 and 6, some thyristors of the TFB-PCSM are turned on, the voltage of the thyristors in the on-state is 0, and the maximum voltage of other sub-module thyristors in the off-state is capacitor voltage u_{c}.

When the TFB-PCSM works in modes 2 and 5, the thyristors of the TFB-PCSM are all turned off. The thyristors will not only bear the capacitor voltage u_{c}, but also bear the DC voltage U_{d}. The off-state equivalent circuit of TFB-PCSM is shown in Fig. 3 where u_{VT1}, u_{VT2}, u_{VT3}, u_{VT4} are the voltages of four groups of thyristors in TFB-PCSMs; r is the voltage-balance resistor for a thyristor element in TFB-PCSMs; and m is the number of thyristors in VTi of TFB-PCSMs.

Assuming that the capacitor voltage is kept constant when the capacitor is bypassed, the voltage of the thyristors can be written as:

$$\begin{cases} u_{\mathrm{VT1}} = u_{\mathrm{VT4}} = \dfrac{1}{2} - \left(u_{\mathrm{c}} + \dfrac{mr}{R+mr}\dfrac{U_{\mathrm{d}}}{n}\right) \\ u_{\mathrm{VT2}} = u_{\mathrm{VT3}} = \dfrac{1}{2}\left(u_{\mathrm{c}} + \dfrac{mr}{R+mr}\dfrac{U_{\mathrm{d}}}{n}\right) \end{cases} \tag{14}$$

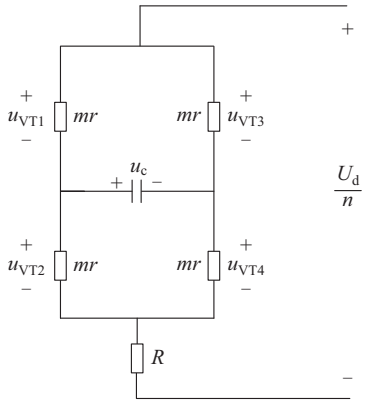

Fig. 3. Off-state equivalent circuit.

In summary, comparing all different operation modes, the maximum voltage of the thyristor in the TFB-PCSM is:

$$U_{\mathrm{VTmax}} = \max\left\{u_c, \frac{1}{2}\left(u_c + \frac{mr}{R+mr}\frac{U_d}{n}\right)\right\} \tag{15}$$

2) Current Stress of TFB-PCSMs

Considering all working modes of the TFB-PCSM, the maximum current flowing through the thyristors in TFB-PCSMs is the peak value of the DC current under fault conditions. Therefore, the selection of the thyristor of the TFB-PCSM can refer to the design principle of the thyristors in the converter station.

In conclusion, the parameter design process of TFB-PCSMs is as follows.

1) Firstly, n TFB-PCSMs in the DC chopper are selected, and R of one module can be obtained by (12) according to the values of U_d, I_d, γ, β in a normal operation state.

2) According to n, R, U_d and u_c, the maximum voltage of VTi in one TFB-PCSM is calculated by (15), and then the appropriate thyristor type and the number m of the series-connected thyristors in each thyristor element are selected to make sure that the voltage stress of each thyristor in TFB-PCSMs is within the allowable range.

3) According to t_q and R, the capacitor size C in each TFB-PCSM can be obtained by (13).

V. Simulation Studies

A. Test System

Based on the CIGRE benchmark model, a test system applying the proposed DC chopper of Fig. 1 is developed. The parameters of LCC-HVDC system are the same as the CIGRE benchmark model as shown in Table II. The basic control is the same as that of the CIGRE benchmark model [16], where the constant DC control and constant extinction angle control are utilized for the rectifier and inverter, respectively. In addition, the VDCOL and current error control (CEC) are also utilized. The coordinated control approach between the presented DC chopper and LCC-HVDC applies the control strategy in Section III. The DC chopper is connected to the DC terminal of the inverter and its parameters are given as follows.

TABLE II
Parameters of LCC System

Parameter	Rectifier side	Inverter side
AC system voltage	345 kV	230 kV
Direct voltage	505 kV	495 kV
Direct current	2 kA	2 kA
Transformer ratio	345 kV/213.5 kV	230 kV/209.2 kV
Leakage inductance	0.18 p.u.	0.18 p.u.

The number of TFB-PCSMs in the DC chopper is related to many factors such as the thyristor type, the number of series-connected thyristors, the resistor of the power consumption branch, capacitor voltage, etc. In the tested system, n = 16 is taken as an example for analysis. When the system operates normally, I_d = 2 kA, γ = 15° and β = 38°. According to (12), R = 10 Ω can be obtained. Since the charged capacitor voltage in one TFB-PCSM is equal to U_d/n, and the voltage-balance resistor of each thyristor is much larger than the resistor in the power consumption branch, the U_{VTmax} of each sub-module is calculated as 32 kV from (15). Thus, the thyristor valve VTi in TFB-PCSMs can be composed of 7 thyristors with rated voltage of 7.2 kV and rated current of 4.84 kA in series. In addition, 1200 μs is taken as t_q for the thyristor, and C = 30 μF can be obtained from (13).

B. Investigation of DC Chopper Under Fault Conditions

In this section, the transient performances under fault conditions and the ability of the proposed DC chopper to mitigate the CF are investigated in PSCAD/EMTDC. The CF probability of the following three cases are compared.

Case 1: LCC-HVDC (CIGRE benchmark model).

Case 2: CCC-HVDC.

Case 3: LCC-HVDC with the proposed DC chopper.

The parameters of LCC-HVDC are shown in Table II. The CCC-HVDC is also developed by modifying the CIGRE benchmark model, in which the capacitor size of 400 μF is selected as given in [13]. The LCC-HVDC system with the proposed DC chopper model is the same as that in Section V-A.

1) Single-phase Grounding Fault of a Single-infeed System

This section compares the LCC-HVDC, CCC-HVDC and LCC-HVDC with DC chopper with a single-phase fault. The simulation results are given in 2 scenarios.

Scenario 1: single-phase fault with 0.3 H inductance grounded. LCC-HVDC (Case 1) and CCC-HVDC (Case 2) systems experience CF but no CF occurs in LCC-HVDC with DC chopper (Case 3).

Scenario 2: single-phase fault with 0.2 H inductance grounded. LCC-HVDC, CCC-HVDC and LCC-HVDC with DC chopper all experience CFs.

1) Dynamic performance comparison

The faults are applied at t = 1.0 s and last for 50 ms. The dynamic performances in Scenarios 1 and 2 are shown in Fig. 4 and Fig. 5, respectively.

From Fig. 4, LCC-HVDC and CCC-HVDC systems experience CF, but the LCC-HVDC with DC chopper (Case 3) mitigates the CF successfully by reducing DC current during

the fault. From Fig. 4(a), the DC current in LCC-HVDC rises to 2.53 p.u. and the DC current in CCC-HVDC rises to 1.86 p.u., while the DC current in LCC-HVDC with DC chopper is lower than the rated value. From Fig. 4(b), the DC voltage of LCC-HVDC drops to 0 and the DC voltage of CCC-HVDC drops to 0.23 p.u., while the DC voltage of LCC-HVDC with DC chopper drops to 0.41 p.u. The maximum power losses in LCC-HVDC and CCC-HVDC are 0.84 p.u. and 0.77 p.u., respectively, while the maximum power loss in LCC-HVDC with DC chopper is 0.61 p.u.. If the fault recovery time is defined as the time taken for the HVDC link to accomplish 90% of its pre-fault power after the fault is cleared [13], the fault recovery time for the LCC-HVDC, CCC-HVDC and LCC-HVDC with DC chopper is 105, 103 and 79 ms, respectively, as can be seen from Fig. 4(c). It can be seen that the utilization of the proposed DC chopper can suppress the over-current, accelerate the recovery process and improve the dynamic performances of the LCC-HVDC system under the given fault conditions.

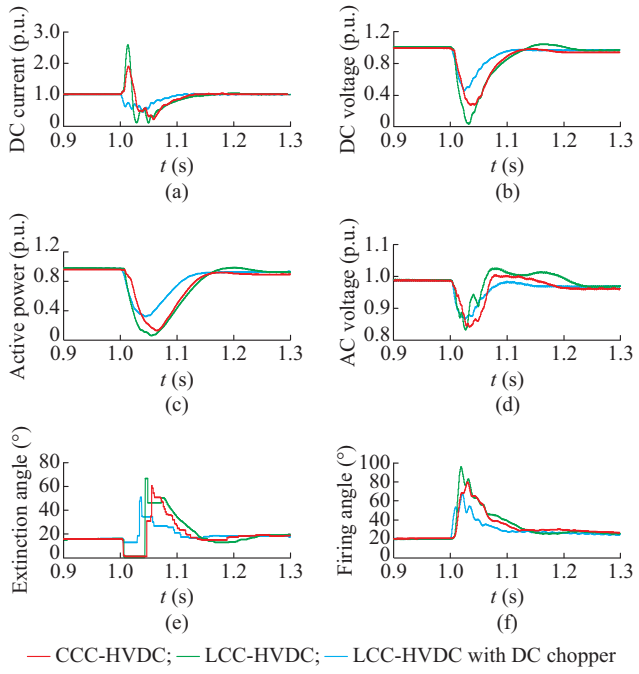

Fig. 4. Transient response comparison of LCC-HVDC, CCC-HVDC and LCC-HVDC with DC chopper under single-phase grounding fault in Scenario 1. (a) DC current. (b) DC voltage. (c) Active power. (d) AC voltage. (e) Extinction angle. (f) Firing angle.

From Fig. 5, when a more severe fault of Scenario 2 occurs, all the three cases experience the CF. From Fig. 5(a), the DC currents in LCC-HVDC and CCC-HVDC rise to 2.56 p.u. and 2.48 p.u., respectively, while the DC current in LCC-HVDC with DC chopper only increases to 1.17 p.u.. Compared to LCC-HVDC and CCC-HVDC systems, the peak value of the DC current in LCC-HVDC with DC chopper reduces significantly. From Fig. 5(b), the DC voltages of LCC-HVDC and CCC-HVDC all drop to 0, while the DC voltage of LCC-HVDC with DC chopper drops to 0.3 p.u.. The fault causes a large loss of DC power. The maximum power losses in LCC-HVDC and CCC-HVDC are 0.87 p.u. and 0.85 p.u., respectively, while the maximum power loss in LCC-HVDC with DC chopper is 0.75 p.u.. After the fault is cleared, the fault recovery time for the LCC-HVDC, CCC-HVDC and LCC-HVDC with DC chopper is 106, 120 and 80 ms, respectively, as can be seen from Fig. 5(c). It can be seen that the utilization of the proposed DC chopper can improve the dynamic performances of the LCC-HVDC system under the given fault conditions.

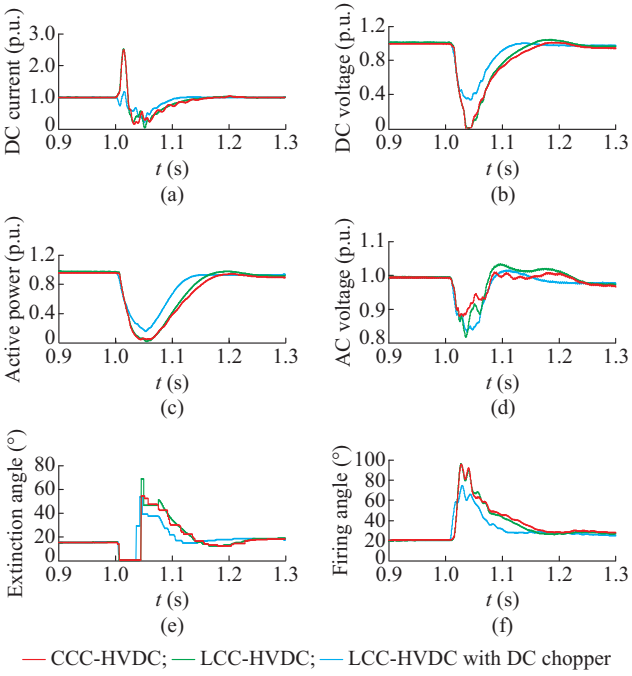

Fig. 5. Transient response comparison of LCC-HVDC, CCC-HVDC and LCC-HVDC with DC chopper under single-phase grounding fault in Scenario 2. (a) DC current. (b) DC voltage. (c) Active power. (d) AC voltage. (e) Extinction angle. (f) Firing angle.

2) Investigation of voltage-current stresses

The voltage-current stresses of TFB-PCSMs are given in Fig. 6 and Fig. 7 for Scenario 1 and Scenario 2, where u_{VT1}-u_{VT4} and i_{VT1}-i_{VT4} are voltages and currents of 4 group thyristors in TFB-PCSMs.

In Scenario 1, the system successfully mitigates the CF. The voltage and current waveforms of thyristor valve VT*i* are shown in Fig. 6. According to the simulation results, the maximum voltage on the thyristor valve is about 30.21 kV, and the voltage of each thyristor is 30.21 kV/7=4.31 kV. The maximum current is about 2.86 kA, which is within the allowable range.

In Scenario 2, the system experiences the CF even with the DC chopper due to the occurrence of the more severe fault. The simulation results are shown in Fig. 7. The maximum voltage across the thyristor valve VT*i* reaches to 30.23 kV, and the voltage of each thyristor is 4.32 kV. During the fault period, the peak current is 2.86 kA, which is still within the allowable range.

3) CF immunity comparison

In this section, the CF immunity index (CFII) is used to evaluate the ability to mitigate the CF of LCC-HVDC [3], and the expression of CFII is shown as:

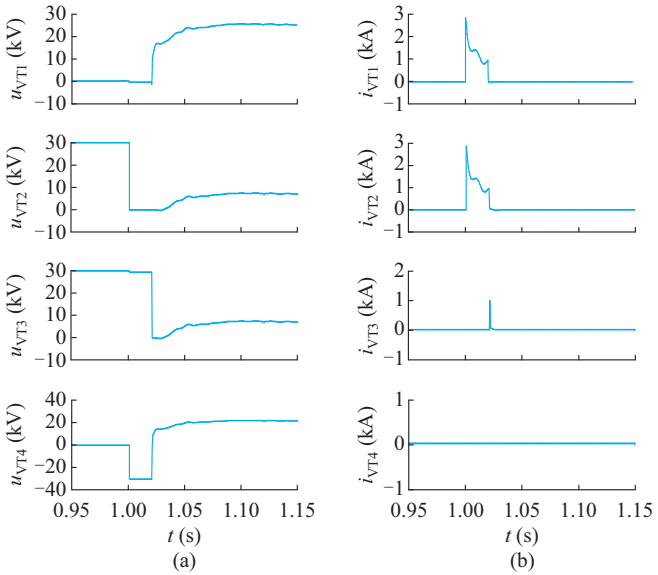

Fig. 6. Voltage-current stresses of TFB-PCSMs with single-phase grounding fault in Scenario 1. (a) Voltage stress. (b) Current stress.

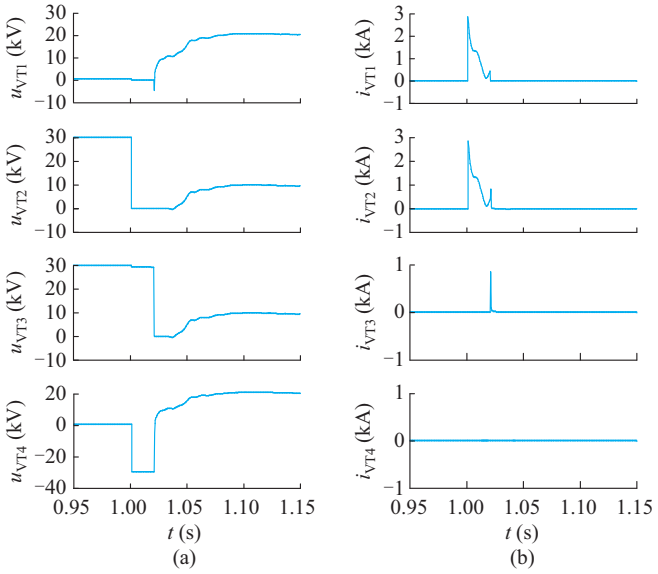

Fig. 7. Voltage-current stresses of TFB-PCSM with single-phase grounding fault in Scenario 2. (a) Voltage stress. (b) Current stress.

$$CFII = \frac{V_{ac}^2}{\omega L_{min} P_{dc}} \times 100\% \tag{16}$$

where V_{ac} is the AC bus voltage on the inverter side; P_{dc} is the DC power; and L_{min} is the critical inductance which is determined by conducting a sequence of electromagnetic transients (EMT) simulations. The larger CFII value indicates the stronger CF immunity of the system.

Single-phase grounding fault with inductance grounded are applied at t = 1.0 s and last for 50 ms in LCC-HVDC, CCC-HVDC and LCC-HVDC with DC chopper systems. Here, the fault angle is defined as the angle interval between fault occurring time and the reference point (the zero-crossing point from negative to positive of phase A voltage). By gradually reducing the fault inductance and observing whether the CF occurs, the critical inductance at different fault angles can be obtained and the corresponding CFII values can be calculated, which are shown in Fig. 8.

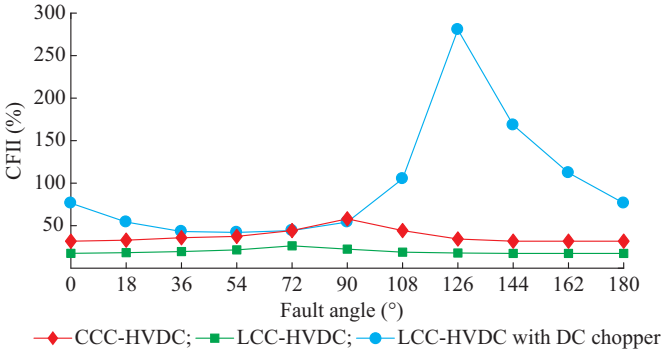

Fig. 8. CFII results with single-phase grounding fault.

Figure 8 shows the CFII curves of LCC-HVDC, CCC-HVDC and LCC-HVDC with DC chopper with single-phase grounding fault. From Fig. 8, the CFII curve of Case 3 (with DC chopper) is higher than those of Case 1 (LCC) and Case 2 (CCC), thus the proposed DC chopper can effectively improve the ability to mitigate the CF. It also can be observed that, the immunity of the CF in LCC-HVDC with DC chopper can be greatly improved at certain fault angles, e. g., from 108° to 162° in Fig. 8, the similar phenomenon also appears in [17]. In [17], it is presented that under single-phase grounding fault conditions, the CFs are determined by the joint effects of the magnitude drop and the zero-crossing advancement of the AC voltage, thus the anomalous CF performance will occur under single-phase grounding fault.

2) Three-phase Grounding Fault in Single-infeed System

This section compares the LCC-HVDC, CCC-HVDC and LCC-HVDC with DC chopper under three-phase grounding fault conditions. The simulation results are provided in 2 scenarios.

Scenario 1: three-phase fault with 0.65 H inductance grounded. LCC-HVDC (Case 1) and CCC-HVDC (Case 2) systems experience CF but no CF occurs in LCC-HVDC with DC chopper (Case 3).

Scenario 2: three-phase fault with 0.5 H inductance grounded. LCC-HVDC, CCC-HVDC and LCC-HVDC with DC chopper all experience CFs.

1) Comparison of dynamic performances

Both faults are applied at t = 1.0 s and last for 50 ms. The results of dynamic performances in Scenarios 1 and 2 are shown in Fig. 9 and Fig. 10, respectively.

From Fig. 9, both LCC-HVDC and CCC-HVDC systems experience CF, however the LCC-HVDC with DC chopper (Case 3) mitigates the CF successfully by reducing DC during the fault. From Fig. 9(a), the DC currents in LCC-HVDC and CCC-HVDC rise to 2.56 p.u. and 2.31 p.u., respectively, while the DC current in LCC-HVDC with DC chopper is lower than the rated value. From Fig. 9(b), the DC voltage of LCC-HVDC and CCC-HVDC all drop to 0, while the DC voltage of LCC-HVDC with DC chopper drops to 0.39 p.u.. The maximum power loss in LCC-HVDC and CCC-HVDC are 0.84 p.u. and 0.81 p.u., respectively,

while the maximum power loss in LCC-HVDC with DC chopper is 0.64 p.u.. The fault recovery time for the LCC-HVDC, CCC-HVDC and LCC-HVDC with DC chopper is 105, 122 and 70 ms, respectively, as can be seen from Fig. 9 (c). Thus, the dynamic performances of the LCC-HVDC link can be greatly improved by the presented DC chopper.

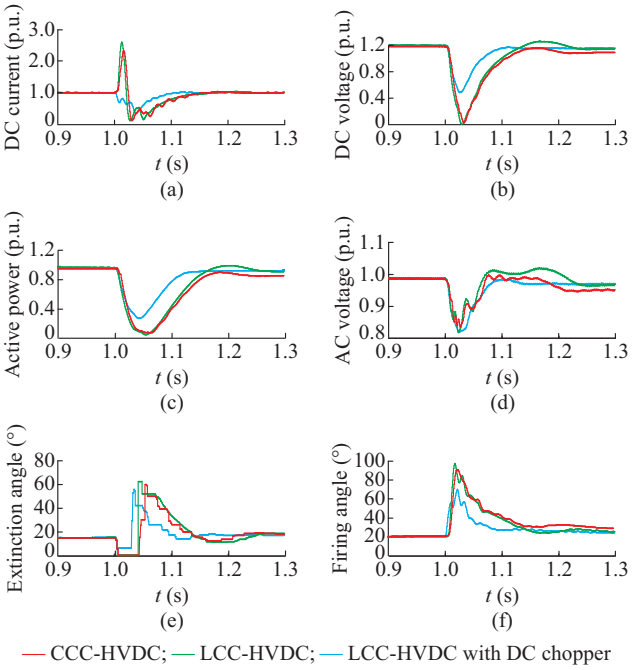

Fig. 9. Transient response comparison of LCC-HVDC, CCC-HVDC and LCC-HVDC with DC chopper with three-phase grounding fault in Scenario 1. (a) DC current. (b) DC voltage. (c) Active power. (d) AC voltage. (e) Extinction angle. (f) Firing angle.

From Fig. 10, when a more severe fault in Scenario 2 occurs, all the three cases experience CFs. From Fig. 10(a), the DC currents in LCC-HVDC and CCC-HVDC rise to 2.57 p.u. and 2.28 p.u., respectively, while the DC current in LCC-HVDC with DC chopper only increases to 1.2 p.u.. Compared to LCC-HVDC and CCC-HVDC, the peak value of the DC current in LCC-HVDC with DC chopper reduces significantly. From Fig. 10(b), the DC voltages of LCC-HVDC and CCC-HVDC all drop to 0, while the DC voltage of LCC-HVDC with DC chopper drops to 0.3 p.u.. The fault causes a large loss of DC power. The maximum power losses in LCC-HVDC and CCC-HVDC are 0.84 p.u. and 0.82 p.u., respectively, while the maximum power loss in LCC-HVDC with DC chopper is 0.74 p.u.. After the fault is cleared, the fault recovery time for the LCC-HVDC, CCC-HVDC and LCC-HVDC with DC chopper is 106, 124 and 76 ms, respectively, as can be seen from Fig. 10(c). It can be seen that the utilization of the proposed DC chopper can improve the dynamic characteristics of the LCC-HVDC system, especially in enabling the whole system to rapidly restore itself to its normal operation state.

2) Investigation of voltage-current stresses

The voltage-current stresses of TFB-PCSMs under three-phase fault conditions are given in Figs. 11 and 12 for Scenarios 1 and 2, respectively.

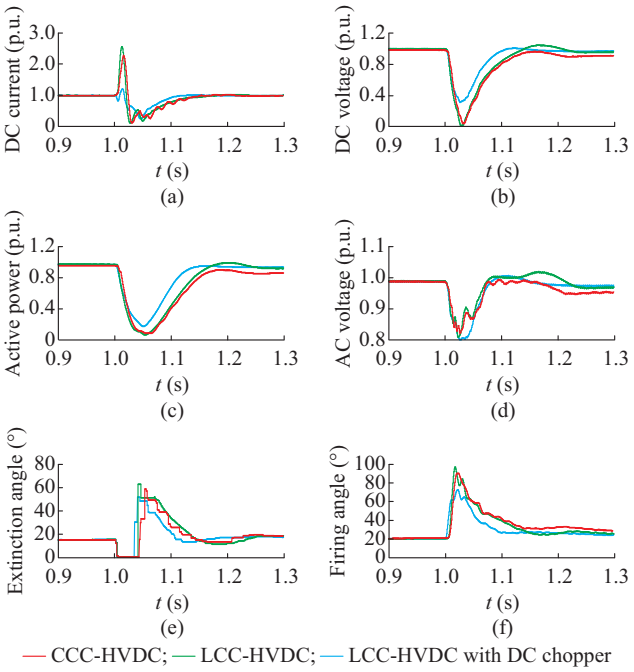

Fig. 10. Transient response comparison of LCC-HVDC, CCC-HVDC and LCC-HVDC with DC chopper with three-phase grounding fault in Scenario 2. (a) DC current. (b) DC voltage. (c) Active power. (d) AC voltage. (e) Extinction angle. (f) Firing angle.

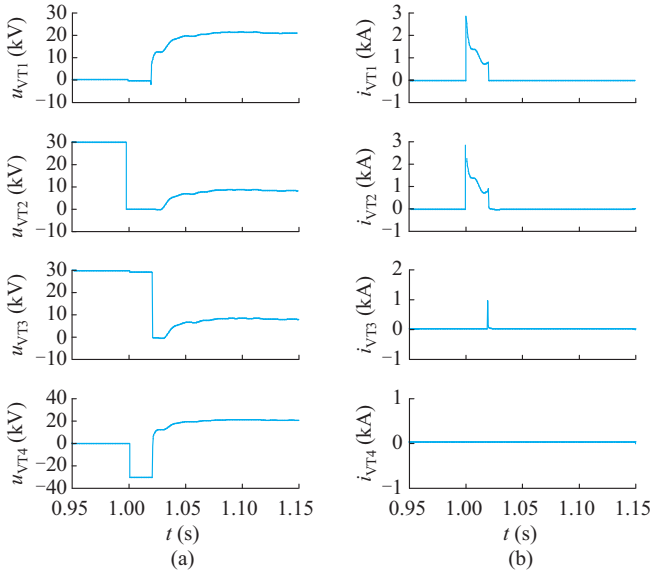

Fig. 11. Voltage-current stresses of TFB-PCSMs with three-phase grounding fault in Scenario 1. (a) Voltage stress. (b) Current stress.

In Scenario 1, the system successfully mitigates the CF. The voltage and current waveforms of the thyristor valve VT*i* in each TFB-PCSM are shown in Fig. 11. According to the simulation results, the maximum voltage on the thyristor valve VT*i* is about 30.18 kV, and thus the voltage of each thyristor is about 30.18 kV/7=4.31 kV. The maximum current is about 2.85 kA, which is within the allowable range.

In Scenario 2, the system fails to mitigate CF. The simulation results are shown in Fig. 12. The maximum voltage on the thyristor valve VT*i* in each TFB-PCSM reaches to 30.23

kV, and the voltage of each thyristor is 4.32 kV. During the fault, the peak current is 2.86 kA, which is also within the allowable range.

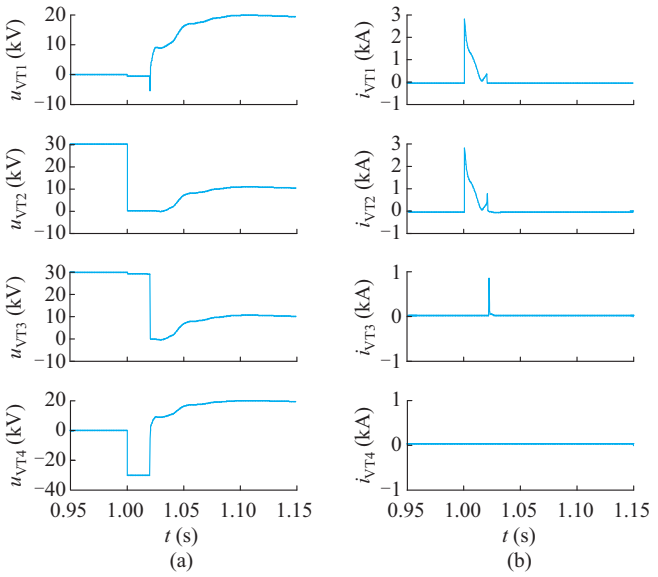

Fig. 12. Voltage-current stresses of TFB-PCSMs with three-phase grounding fault in Scenario 2. (a) Voltage stress. (b) Current stress.

3) CF immunity comparison

Three-phase fault with inductance grounded is applied at t = 1.0 s and lasts for 50 ms in LCC-HVDC, CCC-HVDC and LCC-HVDC with DC chopper. Similarly, by gradually reducing the fault inductance and observing whether the CF occurs, the critical inductance at different fault angles can be obtained and the corresponding CFII values can be calculated, which are shown in Fig. 13.

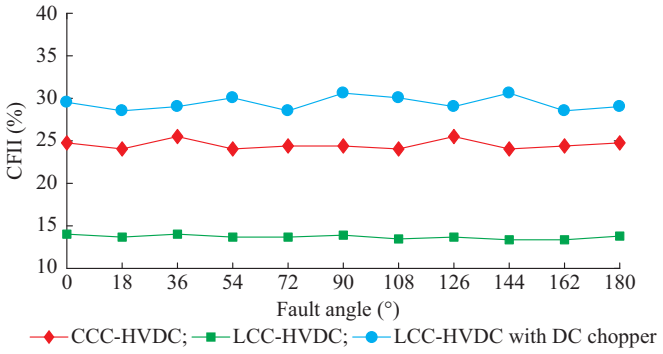

Fig. 13. CFII results with three-phase fault.

Figure 13 shows the CFII curves of LCC-HVDC, CCC-HVDC and LCC-HVDC with DC chopper with three-phase fault. From Fig. 13, the CFII curve of Case 3 (with DC chopper) is higher than those of Case 1 (LCC) and Case 2 (CCC), and thus, with three-phase grounding fault, the proposed DC chopper can effectively improve the CF immunity of LCC-HVDC.

3) CF Probability Investigation in Dual-infeed HVDC System

This section investigates the CF probability of the proposed DC chopper in a dual-infeed system. The probability of CF under a given fault condition is calculated as the fraction of faults that resulted in CF of a certain amount N_{total} applied at different points on the wave within a cycle [13]. In this paper, the value of N_{total} is selected as 100, and the interval time between two adjacent fault points is 20/100 ms = 200 μs. Based on the CIGRE benchmark model, a dual-infeed HVDC model is developed in which LCC-HVDC1 and LCC-HVDC2 are both rated at 500 kV and 1000 MW and connected by a 100 km transmission line. The parameter of the transmission lines is (0.028+j0.271) Ω/km [7]. Z_{tie} is the impedance for transmission line; E_1 and E_2 are the equivalent sources for AC systems of LCC-HVDC1 and LCC-HVDC2, respectively; Z_{s1}, Z_{s2}, Z_{c1}, Z_{c2} are the equivalent impedances for AC systems and filters of LCC-HVDC1 and LCC-HVDC2, respectively; P_{d1} and P_{d2} are the DC power of LCC-HVDC1 and LCC-HVDC2, respectively; I_{d1} and I_{d2} are the DC currents of LCC-HVDC1 and LCC-HVDC2, respectively; U_{d1} and U_{d2} are the DC voltages of LCC-HVDC1 and LCC-HVDC2, respectively; U_1 and U_2 are the AC voltages of LCC-HVDC1 and LCC-HVDC2, respectively; and z_f is the fault impedance. Here, the CF probability of the following two cases is compared.

Case 1: dual-infeed HVDC with two LCC-HVDC links.

Case 2: dual-infeed HVDC, where only LCC-HVDC1 installs the proposed DC chopper at the DC side, as shown in Fig. 14.

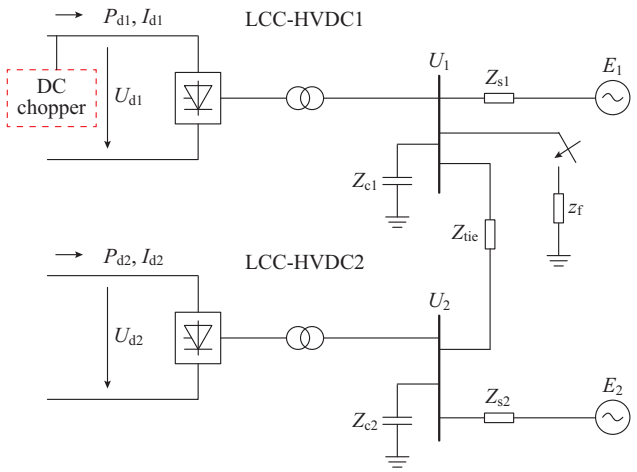

Fig. 14. Dual-infeed HVDC system.

The inductive fault is applied on the bus of LCC-HVDC1 and the CF probability curves of LCC-HVDC1 and LCC-HVDC2 with single-phase and three-phase faults are shown in Figs. 15 and 16. Figures 15 and 16 show that with the decrease of the grounded inductance, the faults are getting more serious and the CF probability of both HVDC links increases gradually. The curve of higher CF probability indicates that the CF is more likely to occur at the same fault level. As can be seen, the curves of CF probability of both LCC-HVDC links in Case 2 (with DC chopper) are lower than those in Case 1 (without DC chopper) with both single-phase grounding fault and three-phase grounding fault. Thus, it can be concluded that the presented DC chopper can greatly reduce the probability of CF for both a local HVDC link

with DC chopper at the DC-side and the adjacent HVDC link in the dual-infeed HVDC system.

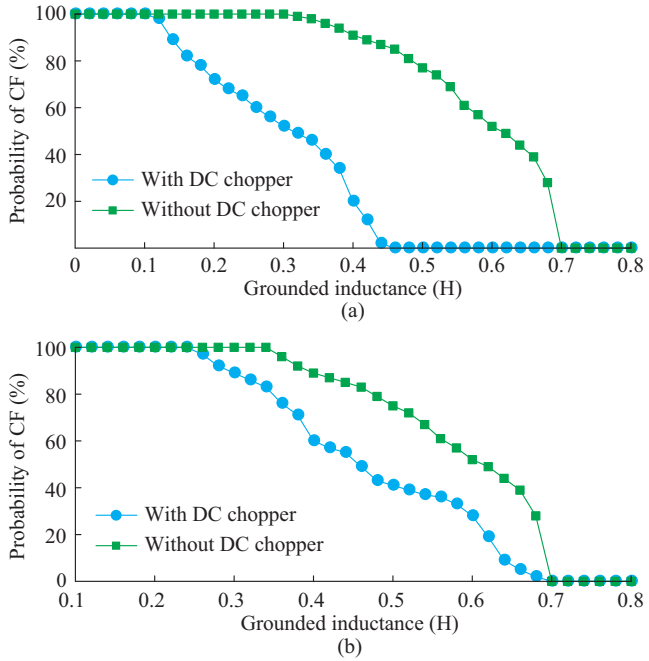

Fig. 15. CF probability comparison of two HVDC links with single-phase grounding fault. (a) LCC-HVDC1. (b) LCC-HVDC2.

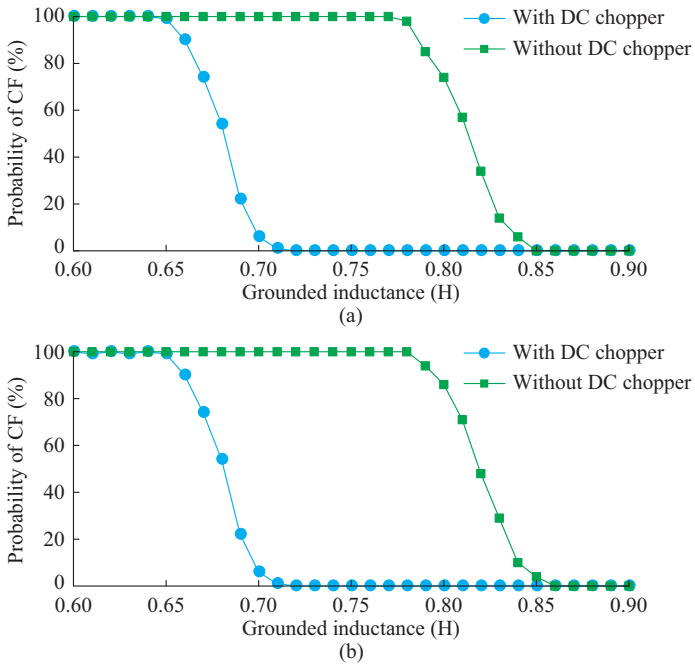

Fig. 16. CF probability comparison of two HVDC links with three-phase grounding fault. (a) LCC-HVDC1. (b) LCC-HVDC2.

C. Discussion for Capital Cost of DC Chopper

As described in Section V-A, for one TFB-PCSM, the maximum voltage for each thyristor unit (each unit can be composed of a certain number of series-connected thyristors) in Fig. 1(b) is set as 32 kV in the studied case, which is about 15.3% of the RMS value or 10.8% of the peak value of the line-to-line commutation voltage. The capital costs of the DC chopper are mainly subject to the four arms, capacitors and resistors of Fig. 1(b). Considering that the number of series connected thyristors in each arm of the LCC converter is proportional to the peak value of the line-to-line commutation voltage, the thyristor cost of each TFB-PCSM is $0.108\times4=0.432$ based on the thyristor cost in each arm of the LCC converter. Since LCC-HVDC adopts a 12-pulse converter which totally has 12 arms, the thyristor cost of each TFB-PCSM will be $0.432/12=0.036$ based on the thyristor cost in a 12-pulse LCC converter. In the studied case, there are 16 TFB-PCSMs embedded in the presented DC chopper, so the total thyristor cost is $0.036\times16=0.576$ based on the thyristor cost in a 12-pulse LCC converter. As for the conventional LCC-HVDC, the thyristor group cost accounts for about 25% of the total capital cost of the LCC station. Thus, the total thyristor group cost of the presented DC chopper is $0.25\times0.576=0.144$ based on the capital cost of the LCC station. To simplify the cost calculation, the capacitor and resistor costs in the TFB-PCSM can be conservatively estimated as 5% of the thyristor group cost [18], then the total capital cost of the DC chopper can be obtained as $0.144\times(1+0.05)=0.151$ based on that of the LCC station. It should be noted that the cost estimation is conservative. When the maximum withstand voltage of thyristor U_{VTmax} is analyzed, the maximum value under fault conditions and normal operation is taken as the selection criterion, thus a certain margin is added during the design process. In fact, the maximum withstand voltage of the thyristor could be slightly smaller than U_{VTmax}. If 0.9 times of U_{VTmax} is taken, according to the calculation method, the increased converter cost will be about 13%.

Although the proposed DC chopper will increase the capital cost to some extent, the CF mitigation effect is quite significant, which could also provide some economic benefits. Firstly, the proposed method improves the availability of the HVDC system by mitigating the CFs, and the system could transmit more power under the fault condition which could provide some economic benefits. Secondly, the proposed method can suppress the overcurrent issue and thus improve the fault recovery characteristics for HVDC links. The suppression of the overcurrent means that the service life of the converter valve can be prolonged, and that the cost of the converter valve can be saved to some extent. From the above analysis, the increased capital cost could be reasonable considering the bought advantages.

The proposed method can greatly reduce the probability of CF for both the local HVDC link and the adjacent HVDC link in a dual-infeed HVDC system. With the increasing number and rating of ultra HVDC systems, the risks of AC system instability and blackout are also increasing. Considering the potential huge economic losses caused by these risks, the savings of the presented method could be significant.

VI. Conclusion

This paper proposes a DC chopper topology composed of a TFB-PCSM to mitigate CF of the LCC-HVDC system.

The operation modes of TFB-PCSMs and the coordinated control approach of the DC chopper are presented. Then, the voltage-current stresses of TFB-PCSMs under different conditions are studied, and the parameter selection approach is provided. Based on the simulation results in PSCAD/EMTDC, the following conclusions are obtained.

1) By comparing the transient performances of LCC-HVDC, CCC-HVDC and LCC-HVDC with DC chopper under fault conditions, it can be concluded that the proposed DC chopper can effectively reduce the probability of CFs and improve the fault recovery characteristics for the LCC-HVDC links.

2) The presented DC chopper can greatly reduce the probability of CF for both the local HVDC link with DC chopper at the DC-side and the adjacent HVDC link in the dual-infeed HVDC system.

3) By the presented parameter selection approach, the voltage-current stresses of TFB-PCSMs could be regulated within the allowable range.

4) The capital cost of the proposed DC chopper is assessed. Considering the greatly improved CF mitigation ability and favorable option in HVDC areas, the capital cost is potentially acceptable.

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