

Evaluation of Feasible Interlinking Converters in a Bipolar Hybrid Microgrid

Parviz Najafi, Abbas Houshmand Viki, and Mahdi Shahparasti

Abstract—A bipolar hybrid microgrid is a new topology which benefits from the advantages of both alternating current (AC) and direct current (DC) microgrids. Interlinking AC/DC converter is the key of this topology which has the following characteristics: being able to provide two equal pole voltages in DC side; complying with the standards of current quality at AC side; being able to control active and reactive power independently in AC side, and transmitting bidirectional power. In this paper, two categories of power converters including single-stage and two-stage converters are proposed for this topology. A new cost-effective control strategy is added to the control of general grid-connected converter for each interlinking converter, and the control of autonomous DC-link pole voltage for both candidates is achieved. Detailed simulations based on the designed control strategies are conducted to validate the function of control strategies under the operation conditions of different DC sides. The performances of two selected interlinking converters with balanced and unbalanced DC loads are analyzed. Suggested power quality of microgrid and total harmonic distortion (THD) analysis are demonstrated in grid-tied and islanded modes. Eventually, semiconductor power loss simulations based on a closed-loop thermal network simulation are conducted. Thereby, the mutual effects of power loss and initial junction temperature are investigated.

Index Terms—Bipolar hybrid microgrid, interlinking converter, DC-link voltage balancing, power loss distribution.

I. INTRODUCTION

DISTRIBUTED generation has been a key solution to the unquenchable worldwide thirst for energy in the past decade. Distributed generation in microgrids offers efficient power for remote areas and presents a flexible power to the grid. Microgrids containing distributed generation systems have been utilized globally in many forms [1]. Alternating current (AC) and direct current (DC) microgrids are widely investigated in [2], and neither can be considered superior to the other. A bipolar hybrid microgrid is a type of microgrid that advantages from both mentioned types and owns a three-wire DC side with two levels. Significant advantages of bipolar feature are: ① providing two voltage lev-

els to loads and sources in DC side; ② increasing efficiency and reliability due to bipolar three-wire system; ③ avoiding unnecessary voltage conversions [3].

DC loads and sources that demand a lower voltage level than total DC-link voltage are connected to one pole of bipolar DC side, which contributes to the downsizing of the power structure and power losses [4]. Figure 1 shows a bipolar hybrid microgrid which has a bidirectional interlinking converter (IC), where V_{LL} is the line to line voltage of AC bus and V_{dc} is the DC-link voltage of DC bus. The primary responsibility of this IC is facilitating a smooth bidirectional power flow between AC and DC buses. Other important factors in selecting an IC for a bipolar hybrid microgrid include the ability to act in an appropriate power range, low harmonic distortion operation and adjustable power factor to interact with reactive power to the grid.

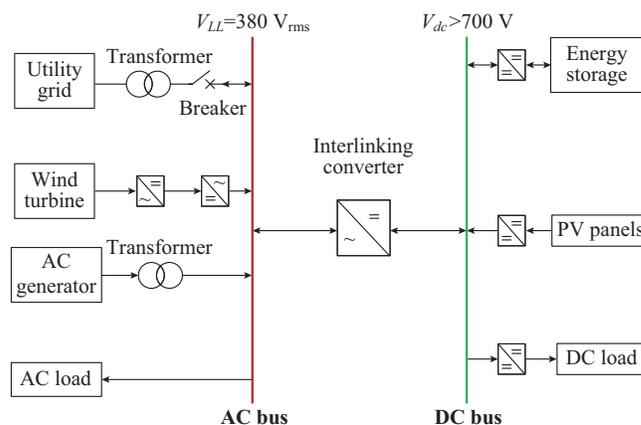


Fig. 1. Bipolar hybrid microgrid concept with multiple DC and AC loads and resources.

Researches on microgrids are mostly dedicated to AC and DC types individually, and their contributions are mainly about central controllers and power-sharing and management strategies [5]-[11]. There are few pieces of research on the structure of ICs in DC bipolar microgrids [3], [4], [12], and the least attention is dedicated to the feasible applicable structure of ICs employed in bipolar hybrid microgrids. The main challenge in selecting an IC for bipolar hybrid microgrid application is its power quality, efficiency, costs in AC and DC side and the performance at severe unbalances in DC side when unequal loads or resources are connected to each pole of the DC link.

Manuscript received: October 7, 2018; accepted: September 5, 2019. Date of CrossCheck: September 5, 2019. Date of online publication: February 28, 2020.

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P. Najafi (corresponding author) and A. H. Viki are with the Department of Electrical Engineering, K. N. Toosi University of Technology, Tehran, Iran (e-mail: parviz.najafi@ee.kntu.ac.ir; hooshmand@eetd.kntu.ac.ir).

M. Shahparasti is with the Department of Electrical Engineering, Polytechnic University of Catalonia, Barcelona, Spain (e-mail: mahdi.shahparasti@upc.edu).

DOI: 10.35833/MPCE.2018.000665

The ICs applied to bipolar hybrid microgrids have a broader application range in comparison to converters used in photovoltaic field, e.g., these ICs transmit bidirectional power and require a DC-link pole voltage balancing system to feed the DC loads with proper nominal voltage under unbalanced DC-link conditions. Applicable IC structure for bipolar networks can be divided into two major structures: single-stage and two-stage structures. Previous works on bipolar DC microgrids use the two-stage structure in which multiple converters are joined, and their combination provides three-wire bipolar at DC side and three-phase at AC side. Reference [3] is an example of two-stage structure. A voltage balancer converter is added to a three-phase two-level voltage source converter (VSC) to build a bipolar DC side. This structure has its downsides such as separate control structure for the balancer converter, extra cost and sizing. And the power capacity of the balancer converter has to be the same as the IC. In [4], an AC-side grounding inductor is added to a three-phase two-level VSC in a bipolar DC microgrid which is another example of the two-stage structure. Full operation test of this structure is investigated. However, the total harmonic distortion of the currents which is directly related to the power quality is not evaluated. Also, adding passive components to the structure of IC raises some problems such as additional costs and volume, and it will narrow down the operation power range of the system.

Single-stage structure is mainly multi-level converter with the lowest voltage levels such as neutral pointed clamped (NPC) converter to prevent extra costs and volume. In [13], NPC converter with a balancer converter is proposed. The balancer converter is used only when there are unbalances in DC bus which overcomes a part of the mentioned obstructions. However, the sizing, cost and power range of balancer converter still exist. Reference [13] uses an auxiliary converter to balance the pole voltages of NPC converter. However, a controller is designed in [14] to prevent the unbalances in DC-link pole voltages without using a voltage balancer converter. In this paper, a single-stage structure with an internal voltage balancing capability for bipolar hybrid microgrid is proposed. The proposed embedded control system of voltage balancing for NPC converter provides the feasibility of balancing the DC-link pole voltages. The system also provides higher power quality at both AC and DC sides, lower transformer ratio, ability to work on medium voltage and high power operation and efficiency. In this paper, two IC candidates of single-stage and two-stage structures are selected for this type of microgrid, and a new modified control strategy for both structures is presented to overcome the problem of balancing DC-link pole voltages. Also, the studied IC candidates are evaluated from different aspects to analyze their positive and negative effects. This paper is organized as follows. Section II presents the feasible structures in bipolar hybrid microgrid and two selected IC candidates are introduced. Section III gives the detailed general control strategy of converters in grid-tied and islanded modes, followed by the new modified control strategy of ICs. Efficiency evaluation of control strategy, power quality of ICs and loss analysis are presented in the simulation results in Section IV. Fi-

nally, the conclusions are presented in Section V.

II. FEASIBLE INTERLINKING CONVERTER STRUCTURES OF BIPOLAR HYBRID MICROGRID

In this section, the topologies of single-stage and two-stage structures are presented, and one candidate for each structure type is selected to be evaluated in a bipolar hybrid microgrid.

A. Topology of Single-stage Structure

The single-stage structure employs a converter that already owns a bipolar DC side, e.g., multi-level converters. NPC converter is the simplest three-phase multi-level converter that has an inherent bipolar DC side and higher AC power quality compared to the three-phase two-level VSC.

Figure 2 shows an NPC converter as a representative of multi-level group utilization in a bipolar hybrid microgrid. NPC converter is selected as the representative of this group since using a multi-level with higher voltage levels leads to extra semiconductors and capacitors. Therefore, the cost and volume of the structure will be enhanced accordingly. The control strategy of this structure type has more complexity than that of the two-stage structure since voltage balancing strategy has to be embedded in the central control scheme of IC, and there are limitations in the unbalances of DC loads.

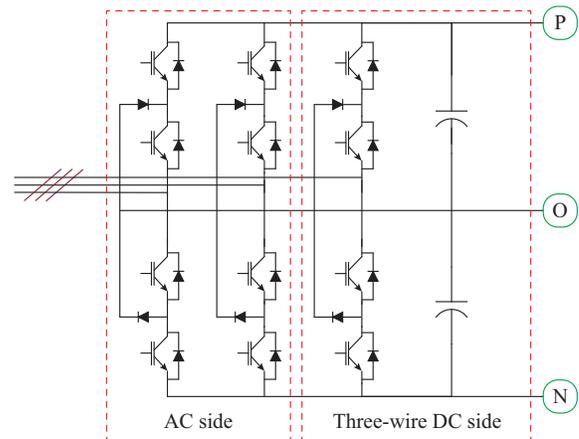


Fig. 2. Topology of NPC converter as a candidate of single-stage structure.

B. Topology of Two-stage Structure

Multiple topologies for two-stage structure have been proposed but the idea behind this structure is that one converter does the power inversion task and the other one provides the bipolar DC feature. The most commonly used two-stage structure is shown in Fig. 3, where SB_1 and SB_2 are two switches. It is a joined combination of three-phase two-level VSC named B6, and a DC/DC voltage balancer converter which is named B6-Balancer. The balancer converter is added to a B6 converter to create a bipolar DC side. This structure is selected as a typical model of a two-stage structure working as IC in a bipolar hybrid microgrid because of its widespread application in researches.

This structure is formerly investigated in [3] and is applied to a DC microgrid. The balancer circuit of structure

can be replaced by four-switch voltage balancer which is used in [13].

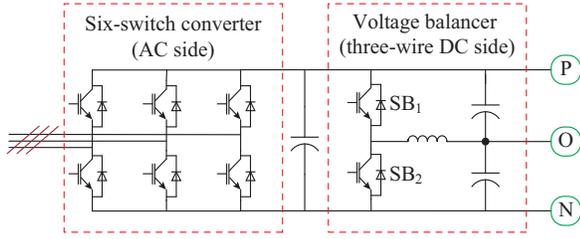


Fig. 3. Topology of B6-Balancer structure as a candidate of two-stage structure.

The control strategy of the balancer converter in the two-stage structure is entirely separated from the three-phase converter and relatively straightforward.

However, the power rating of balancer converter has to be the same as the three-phase VSC, which is a remarkable drawback that affects the costs and size of the converter.

III. CONTROL STRATEGY OF SELECTED ICs IN A BIPOLAR HYBRID MICROGRID

In this section, the general control strategy of both selected ICs in grid-tied and islanded modes are investigated. These control strategies have certain mutual points which are surveyed in the first case followed by their differences in balancing the DC-link poles studied in the second case. Three different control strategies can be suggested for an IC in either grid-tied or islanded mode [15]: ① AC grid forming and DC grid feeding; ② DC grid forming and AC grid feeding; ③ DC grid forming and AC grid supporting.

In the first case, the IC injects or receives active power from DC bus based on AC bus demand. In this control strategy, another converter located in DC bus is in charge of controlling DC bus voltage while IC may have the role of balancing the pole voltages. In the second case, on the AC bus, a diesel generator, a microturbine, or another inverter is responsible for controlling the voltage and frequency at AC side. IC is only in charge of injecting active or reactive power to AC bus, and its primary objective is to control and balance the pole voltages of DC bus. In the last case, the priority of IC is to control and balance the DC bus and the rest of its capacity is assigned to support the AC bus. The suggested control strategy in this paper benefits from the second case in which the total capacity of IC is assigned to form DC bus voltage, and the state of AC bus does not have any effects on the performance of IC.

In a grid-tied system which is shown in Fig. 4, the general control principles of ICs are the same [16], [17]. In Fig. 4, i_{dc1} and i_{dc2} are the currents which are passed through the DC-link capacitors. The ultimate purpose of IC is injecting or receiving a low total harmonic distortion (THD) high-quality AC current from the grid and thereby feeding the loads without any interruptions. Voltage equations of grid filters in Fig. 4 are in (1), which is transformed to synchronous reference frame by park equations, which is upgraded to (2).

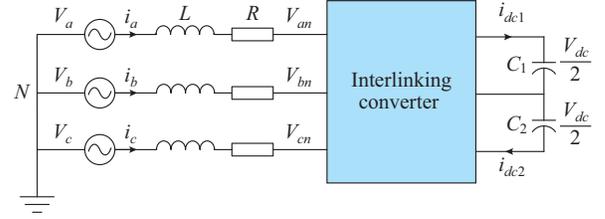


Fig. 4. Model of a grid-connected interlinking converter.

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = R \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + L \frac{d}{dt} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = R \begin{bmatrix} i_d \\ i_q \end{bmatrix} + L \frac{d}{dt} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \omega_s L \begin{bmatrix} -i_q \\ i_d \end{bmatrix} + \begin{bmatrix} V_{dn} \\ V_{qn} \end{bmatrix} \quad (2)$$

where V_a, V_b, V_c, V_d, V_q are the grid phase voltages; i_a, i_b, i_c, i_d, i_q are the grid injected AC currents; R and L are the line resistance and inductance, respectively; ω_s is the speed; and $V_{an}, V_{bn}, V_{cn}, V_{dn}, V_{qn}$ are the voltages across each phase of the converter.

Under the steady-state condition, (2) transforms to (3) which represents the relationship of grid voltage, grid current and output voltage of the converter. If the d -axis in the rotating reference frame at ω_s speed is aligned on the grid voltage vector, $v_q = 0$. The control strategy of both IC candidates has a current and DC-link voltage control loop, and the model of the current control loop is achieved by (3). The separated items in the equation are considered as a state equation between the output voltage and input currents, and other items are compensation items. The same procedure can be followed by writing power balance equations between DC and AC buses to reach the DC-link control loop.

$$V_{dn} = - \left(R i_d + L \frac{di_d}{dt} \right) + \omega_s L i_q + V_d V_{qn} = - \left(R i_q + L \frac{di_q}{dt} \right) - \omega_s L i_q \quad (3)$$

Figure 5 shows a standard control strategy of an IC connected to the grid that contains an inner current loop and an outer DC-link voltage control loop. In Fig. 5, V_{abc} is the three-phase AC-side voltage and i_{abc} is the three-phase currents; θ is the angle calculated by the phased locked loop (PLL) from the three-phase AC-side voltages; P and Q are the active and reactive power in AC side, and the starred variables in this paper are the reference value of the mentioned variable; V_{ref} is the reference values of pulse width modulation (PWM) carrier signals in rotating reference frame which is obtained by reference values of d -axis and q -axis variables $V_{d,ref}$ and $V_{q,ref}$ respectively.

The output of these two control loops is the reference voltages in the $dq0$ reference frame, which is transformed into the abc reference frame where V_{dq0} and i_{dq0} are produced. In this paper, the reference value of the q -axis current is considered as zero to obtain a unity power factor. The three-phase reference is generated, and it is typically compared to carrier wave to generate pulses of converter switches. The control strategy discussed in Fig. 5 is conventional, and for brevity, the mathematical derivation of conventional method is omitted. Figure 5 is also not robust for DC load unbalanced con-

ditions. Unequal DC loads make one pole voltage from set-point voltage reference to V_{dc} and the other one to zero. In order to overcome this challenge, modifications have to be performed on control strategy or converter topology to reach a steady and stable DC-link pole voltage which is proposed in the next sections.

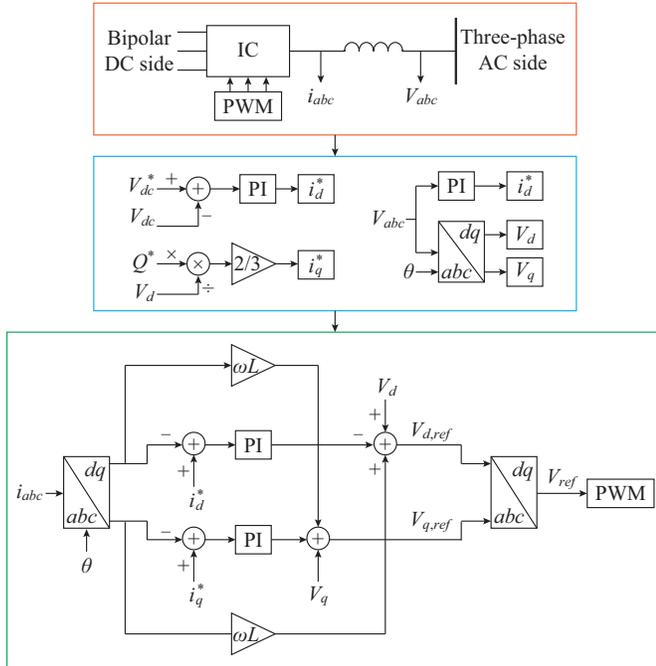


Fig. 5. Standard control strategy of a grid-connected IC.

A. Proposed Control Strategy of NPC Converter to Balance DC-link Pole Voltage

As discussed earlier, unequal loads in DC bus results in unbalanced DC-link pole voltage which causes an interruption in feeding loads that are connected to one pole and destructing of IC semiconductors since it doubles their voltage stress. In [18], a method is introduced for balancing the DC voltages of NPC converter under unbalance condition. However, it needs coupling neutral point of DC side in NPC to the neutral point of the transformer at AC side. In this paper, this method is upgraded to a level that the coupling of neutral points is not required, and it carries all the benefits of the previous method. Also, in this method, additional passive components are eliminated which result in a decrease of costs and volume and an increase of reliability since all the passive and active items have a mean time to failure (MTTF). By omitting these items, the reliability of the whole system will be enhanced. Figure 6 shows the novel upgraded design to control DC-link voltage of NPC converter, which will be an extension to the standard control strategy of grid-tied ICs shown in Fig. 5. In order to create a controllable zero component current, upper and lower pole voltages are compared in Fig. 6, where $V_{dc,1}$, $V_{dc,2}$ are the DC-link voltages of each pole and $V_{dc,total}$ is the whole voltage of the DC-link. Their errors are passed through a divider to make voltage error based on total DC-link voltage. Then, the per unit voltage error passes through a proportional integral

(PI) controller, and the outcome is counted as a reference value of zero component current which is known as i_0^* . The value i_0^* is then evaluated by zero current feedback that is depicted in Fig. 6, and the result is fed to a PI controller to generate the zero component of the reference voltage. Components of d and q axes of reference voltage are obtained earlier in standard control strategy of grid-tied converters, so that abc to $dq0$ conversion gives out the three-phase reference signals.

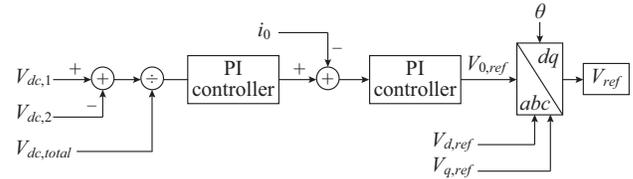


Fig. 6. Proposed balancing control strategy of NPC converter.

The main reason that zero component of current and voltage (V_0 , i_0) is engaged in this control strategy is that, when an unbalanced condition happens in DC loads, (4) and (5) detect this difference and start to act correspondingly. In (4) and (5), K_p is the proportional gain and K_i is the integral gain of PI controller. Moreover, the balancing strategy has to be inverted for reverse power flow which is determined by a simple sign block through power flow.

$$i_0^* = (V_{dc,1} - V_{dc,2}) \left(K_p + \frac{K_i}{s} \right) \quad (4)$$

$$V_{0,ref} = -(i_0^* - i_0) \left(K_p + \frac{K_i}{s} \right) \quad (5)$$

B. Modified Control Strategy of B6-Balancer Structure to Balance DC-link Voltages

In this section, balancing control strategy of a two-stage structure candidate is explained. The general control strategy of the grid-connected B6 converter is based on Fig. 5. Figure 7 demonstrates an independent control scheme of balancer converter. In this method, upper and lower DC-link voltages are compared, and the result is divided by total DC-link voltage to obtain the error signal per unit. The per unit error signal in comparison to a triangle carrier wave generates pulses of two switches in the balancer converter. The carrier wave frequency is the same as the switching frequency of the B6 converter.

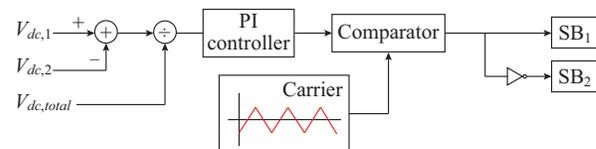


Fig. 7. Modified balancing control strategy of B6.

The previous methods in this balancer converter have extra blocks for realizing the best outcome for controlling the converter without any current feedbacks, which is eliminated in the proposed strategy. The unbalances in DC loads deter-

mine which switch has the major duty cycle, and the two switch pulses are complementary. Stress voltage on the switches is equal to the DC-link total voltage, which is a drawback in comparison to NPC converter. Thus, higher rate switches and passive elements have to be chosen for this balancer converter.

IV. SIMULATION RESULTS AND DISCUSSION

In order to study the effectiveness of the proposed single-stage and two-stage IC candidates, NPC and B6-Balancer as IC in a bipolar hybrid microgrid are simulated in two case scenarios. A bipolar hybrid microgrid model, as shown in Fig. 8, is designed and a detailed time domain simulation is conducted in MATLAB/Simulink. In the first case, the grid-tied mode of the microgrid is simulated, and DC loads are connected to DC bus to investigate the DC voltage balancing capability of ICs. In the second case, DC loads are disconnected, and a three-phase linear AC load is connected to the AC bus.

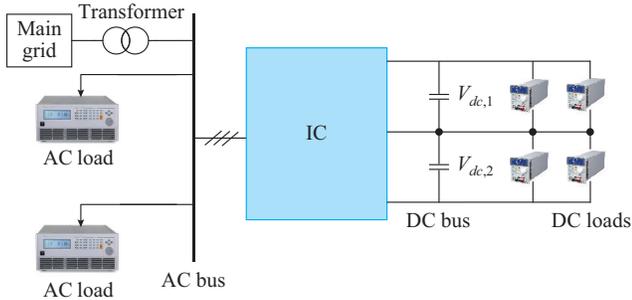


Fig. 8. Simulated model of bipolar hybrid microgrid.

One of the main goals in hybrid microgrids is feeding the local loads by local DERs since it reduces unnecessary voltage conversions and transmission losses. Therefore, in the first case, the worst case has been considered. When the whole power has to be transmitted by IC, all sources on DC bus are disconnected so that the whole power needed for DC loads is supplied by the grid. The grid in this simulation is regarded as an infinite bus which has a 380 V line-to-line voltage and 50 Hz frequency. The IC reference power is defined as 100 kW. The DC-link reference value is set to 800 V. Therefore, wind energy conversion system can be connected to DC bus. Detailed system parameters used in the modeling and simulation are listed in Table I.

TABLE I
SIMULATION PARAMETERS OF SIMULATED MODEL

Parameter	Value
Switching frequency	5 kHz
Grid voltage and frequency	380 V, 50 Hz
AC filter	$L = 400 \mu\text{H}$, $R = 0.01 \Omega$
AC load	$L_1 = 25 \text{ kW}$, $L_2 = 25 \text{ kW}$
Rated voltage of DC bus	800 V
DC loads	50 kW for each pole

A. Simulation Results Under DC Load Balanced and Unbalanced Conditions in Grid-tied Mode

The devised case scenario in this section evaluates the efficiency of single-stage and two-stage IC candidates and their proposed control scheme under the balanced and unbalanced DC load conditions in grid-tied mode. The total DC-link voltage, DC-link voltage of each pole, output voltage quality of converter, output currents quality, THD value of injected current from the grid, and power delivered from the grid to the DC loads are the main factors that have been studied and evaluated in this section. The model is simulated under normal conditions followed by two unbalances in DC loads.

The performance of investigated ICs in the steady state during the injection of power from the grid to DC loads is surveyed. And simulation results are in steady-state mode until $t = 1$ s when the first additional load is added to the upper DC-link pole and causes unbalances in DC loads.

Under the first unbalanced condition, a sudden DC load equal to 50% of nominal upper DC load is added to the upper pole at $t = 1$ s. The second change occurs in DC loads at $t = 1.5$ s, when DC load of upper pole raises to 100 kW which is twice higher than that of the lower pole. The 100% difference in DC poles creates a severe condition. Therefore, voltage balancer strategy is studied under the extreme condition, and the efficiency and limitations of the proposed balancing strategy are tested.

Simulation results related to NPC structure are gathered in Fig. 9 to Fig. 12, and the results for B6-Balancer structure are demonstrated in Fig. 13 to Fig. 16. Exchanged power of NPC and B6-Balancer structure is displayed in Fig. 9(a) and Fig. 13(a), which indicates that selected ICs under both balanced and unbalanced conditions are able to transmit stabilized power to loads accurately.

As unbalanced condition happens in DC poles, it is comprehended from Fig. 9(c) and Fig. 13(c) that B6-Balancer structure is able to damp unbalance in DC load and deliver more higher-quality DC-link voltage with lower DC ripple, even though the NPC structure provides sufficient standard DC-link voltage under both balanced and unbalanced conditions. Total DC-link voltage has acceptable DC-link ripple in both ICs which is represented in Fig. 9(b) and Fig. 13(b).

Another remarkable note which can be observed from Fig. 9(b)-(c) and Fig. 13(b)-(c) is that the pole and total DC-link voltage variation around reference value in both cases is in the acceptance criteria. However, in B6-Balancer case, voltage ripple is considerably lower than that in NPC case. The reason behind the difference of voltage ripple is that in B6-Balancer, there are passive elements which make the balancing operation more straightforward despite their adverse effect on the costs and volume of the structures.

In Fig. 10 and Fig. 14, the current injected from the grid to loads under balanced and unbalanced conditions is reviewed. It is concluded that sinusoidal form of currents in NPC case is better than B6-Balancer case not only in the steady state but also under unbalanced conditions. THD of injected currents is calculated, and the results are shown in Fig. 11 and Fig. 15.

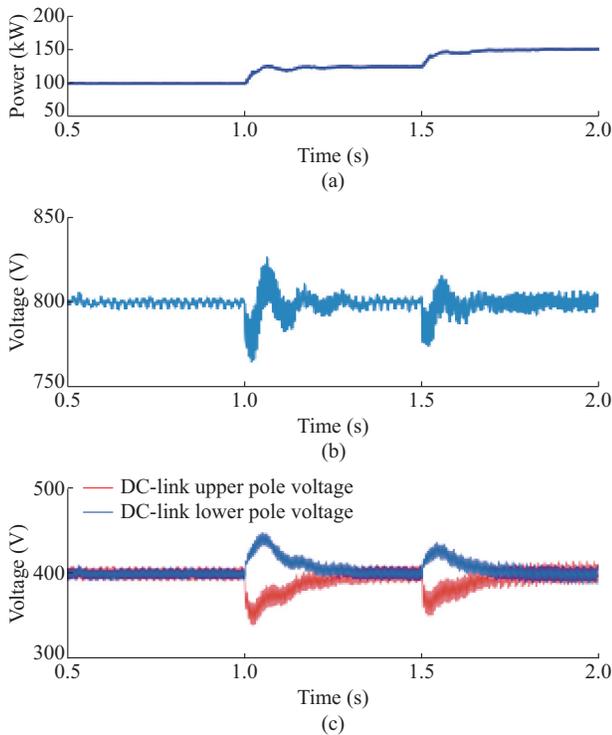


Fig. 9. NPC operation as IC in bipolar hybrid microgrid in balanced and unbalanced DC loads. (a) Active power injected from grid. (b) Total DC-link voltage. (c) DC-link upper and lower pole voltage.

Injected AC currents to NPC converter in the simulated model of bipolar hybrid microgrid has 3.78% THD in worst-case scenario, whereas injected current in B6-Balancer structure has 7.78% THD that is twice as high as NPC structure. The 105% increase in the current THD validates the improved outcomes when the single-stage IC is applied.

The quality of the line-to-line voltage of the compared ICs are illustrated in Fig. 12 and Fig. 16. These figures show a giant gap between THD levels of the output line-to-line voltage in the selected ICs. And it shows another advantage of the multi-level use since NPC has a three-level voltage rather than the two-level voltage of B6-Balancer. The results of the simulations show that B6-Balancer structure produces 94.02% voltage THD in comparison to NPC structure that has 42.44% voltage THD, which means the THD level of output AC voltage is reduced by 55% when the single-stage IC structure is utilized. The three-level output voltage that NPC structure produces lead to an increase in power quality and the reduction of filter size, costs, and space.

However, THD of injected currents in two-stage structure has exceeded the allowed 5% standard amount. The B6-Balancer structure has better ability to damp and equalize DC-pole voltage rather than NPC structure, while the THD level of injected currents in this structure is too high in light loads. Therefore, stronger filters with higher rate passive elements are needed to help this structure lower the THD level and limit it to the authorized zone. This defect leads to higher costs, volume, size and more importantly, reduces the level of the controllability of IC. Since it will be dependent on passive elements and when the DC loads are changed, passive elements may not be compatible with different loads.

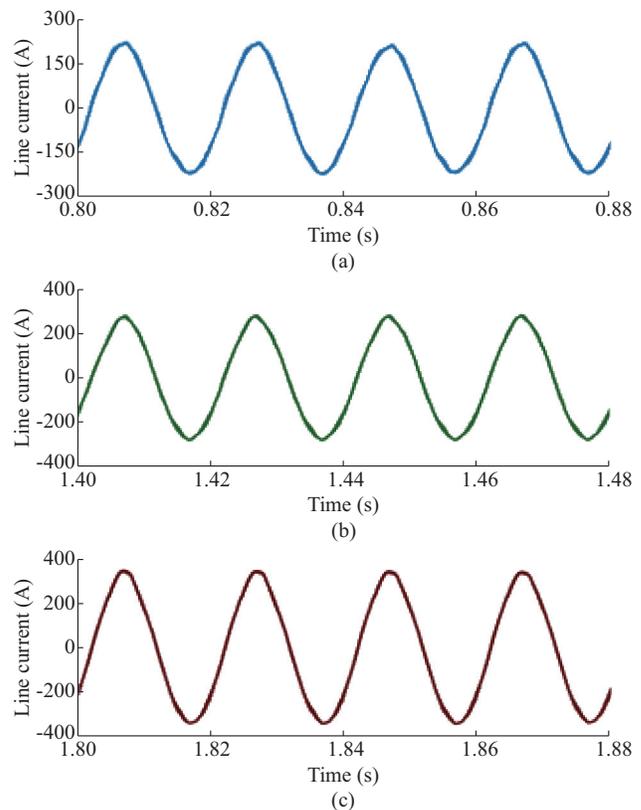


Fig. 10. Injected currents from grid to NPC as IC in balanced and unbalanced modes. (a) Phase A of line current in steady state. (b) Phase A of line current under the first unbalanced condition. (c) Phase A of line current under the second unbalanced condition.

B. Simulation Results of Microgrid Operation in Islanded Mode

The simulation of the bipolar microgrid operation in islanded mode employing the selected ICs is based on the first method described in Section III. In this case, DC loads are disconnected, and it is assumed that a 50 kW three-phase resistive load is connected to AC bus besides multiple DC resources that are linked to the DC bus. The AC load is supplied through the utility grid in grid-tied mode until the islanding operation is activated, and then the AC load is fed by the resources on DC bus. When $t = 0.5$ s, the three-phase breakers disconnect the connection of utility grid between the microgrid and the grid, which results in an activation of the islanded mode.

Figures 17 and 18 show the operation of the microgrid in grid-tied and islanded modes using NPC and B6-Balancer structures as IC, respectively. Figure 17(a) and Fig. 18(a) demonstrate phase-to-ground voltage of three-phase load, and Fig. 17(b) and Fig. 18(b) depict three-phase AC currents of utility grid. The results show that the transition from grid-tied to islanded mode occurs smoothly, and sudden inrush current or voltage peaks are entirely avoided with the help of designed control methods. From the perspective of power quality, inherent superiority of NPC structure at AC side leads to better current and voltage waveforms with lower THD levels in comparison to B6-Balancer structure.

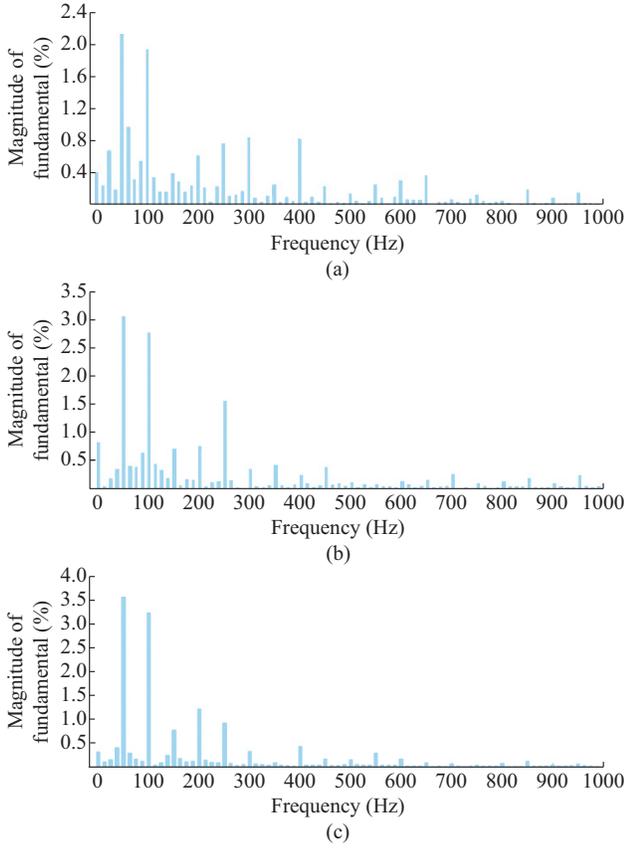


Fig. 11. FFT analysis of injected current in NPC structure. (a) THD analysis of AC current in steady state (fundamental is 216.7 A and THD is 3.79%). (b) THD analysis of AC current under the first unbalanced condition. (fundamental is 269.8 A and THD is 4.10%). (c) THD analysis of AC current under the second unbalanced condition (fundamental is 334.3 A and THD is 4.14%).

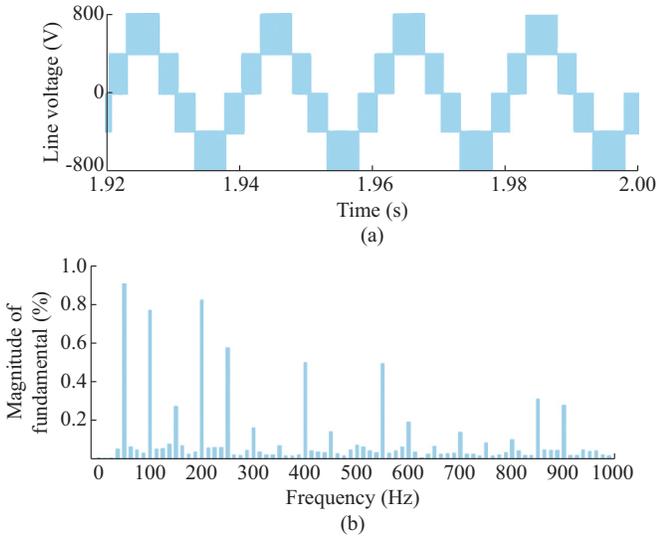


Fig. 12. AC line voltage of NPC structure and its FFT analysis. (a) Three-level output voltage of converter. (b) Output voltage THD of converter (fundamental is 334.3 V and THD is 4.14%).

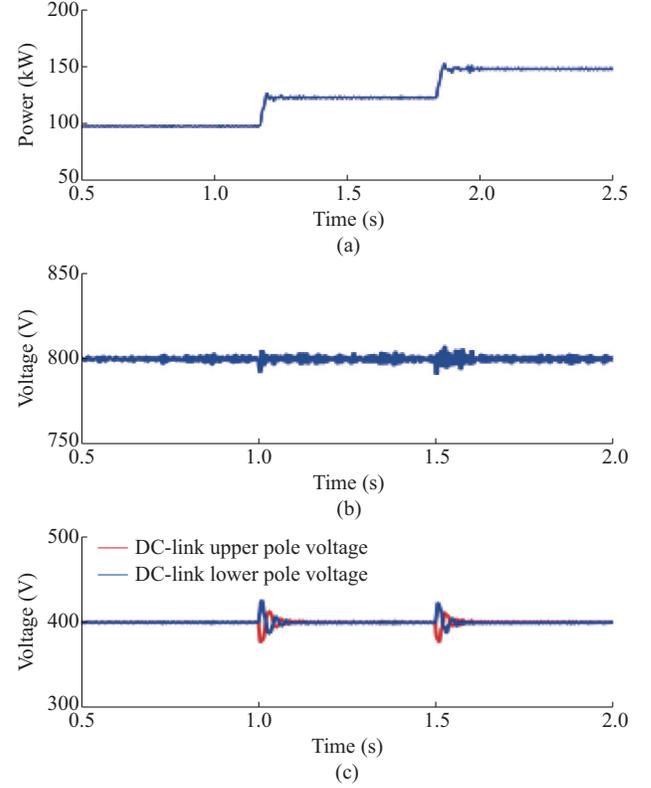


Fig. 13. B6-Balancer operation as IC in bipolar hybrid microgrid in balanced and unbalanced DC loads. (a) Active power injected from grid. (b) Total DC-link voltage. (c) DC-link upper and lower pole voltage.

C. Semiconductor Power Loss Comparison of Selected ICs

The power loss of a converter is one of the main factors to show the efficiency of the structures [14]. Two main categories of semiconductor power losses $P_{ave,loss}$ shown in (6) consist of conduction and switching losses.

$$P_{ave,loss}(n) = \frac{1}{T_{sw}} (E_{cond,loss}(n) + E_{sw}(n)) \quad (6)$$

where n is for the n^{th} switching cycle; $E_{cond,loss}$ is the conduction energy loss; T_{sw} is the switching time period; and E_{sw} is the switching energy losses of semiconductors. The conduction energy loss of semiconductors can be expressed as:

$$E_{cond,loss}(n) = \int_{T_{on}(n)} V_{ce}(t) i_c(t) dt \quad (7)$$

where T_{on} is the on time period of the device; and V_{ce} and i_c are forward saturation voltage and collector current of the semiconductor, respectively. These parameters are dependent on semiconductor current, voltage and junction temperature T_j , which is indicated in (8).

$$V_{ce}(t) = f_1(i_c(t), T_j(t)) \quad (8)$$

In a transient period of turning-off and turning-on of a semiconductor, switching energy loss occurs which is a summation of turn on and off switching energy losses, and it is demonstrated in (9).

$$E_{sw}(n) = E_{sw,on}(n) + E_{sw,off}(n) \quad (9)$$

where $E_{sw,on}$ is switch-on energy losses and $E_{sw,off}$ is switch-off energy losses.

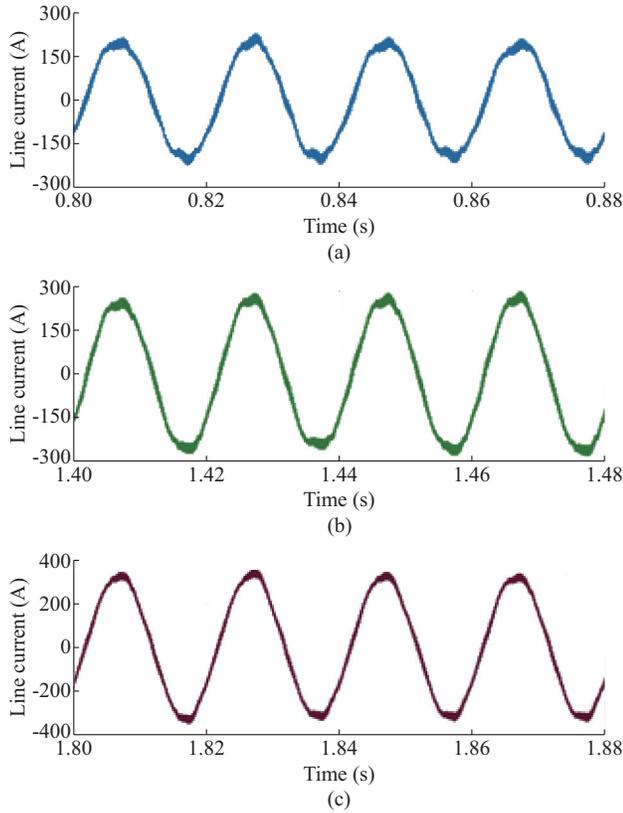


Fig. 14. Injected currents from grid to B6-Balancer as IC in balanced and unbalanced modes. (a) Phase A of line current in steady state. (b) Phase A of line current under the first unbalanced condition. (c) Phase A of line current under the second unbalanced condition.

Switch-on and switch-off energy losses are also related to semiconductor current and T_j , which is explained in (10).

$$\begin{cases} E_{sw,on}(n) = f_{sw,on}(i_c(n), T_j(n)) \\ E_{sw,off}(n) = f_{sw,off}(i_c(n), T_j(n)) \end{cases} \quad (10)$$

where $f_{sw,on}$ and $f_{sw,off}$ are the switching frequency in switch-on period and switch-off period of the device.

As it is noted in (7), (8) and (10), semiconductor junction temperature has an extreme effect on energy loss. Therefore, in addition to power loss simulations, a closed loop thermal simulation is modeled to calculate the power loss of selected ICs. F3L400R07ME4_B23 insulated gate bipolar transistor (IGBT) module and A397M-ND fast diode are selected for NPC structure, and FF450R12ME4P_B11 IGBT modules which have higher rates are selected for B6-Balancer structure. The mentioned power modules have built-in freewheeling diodes which also have conduction and switching losses calculated based on the modeled scheme in Fig. 19. In this diagram, v is the voltage across the device; T_{off} is the turn-off energy, E_{rr} is the reverse recovery energy; v_f is the reverse recovery diode voltage drop with the rated current; v_{ce} is the saturation collector emitter voltage of the semiconductor; and f_1 to f_5 shows that these variables are the functions which are dependent on the introduced parameters. IGBT modules in NPC structure endure half of the voltage stress in comparison to B6-Balancer structure.

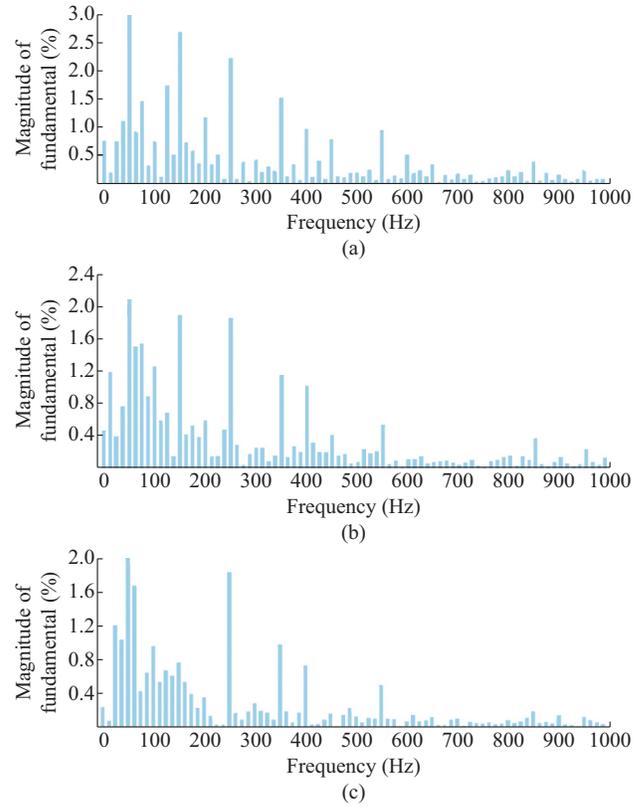


Fig. 15. FFT analysis of injected currents in B6-Balancer structure. (a) THD analysis of AC current in steady state (fundamental is 203.6 A and THD is 7.78%). (b) THD analysis of AC current under the first unbalanced condition (fundamental is 264.6 A and THD is 6.2%). (c) THD analysis of AC current under the second unbalanced condition (fundamental is 329 A and THD is 4.95%).

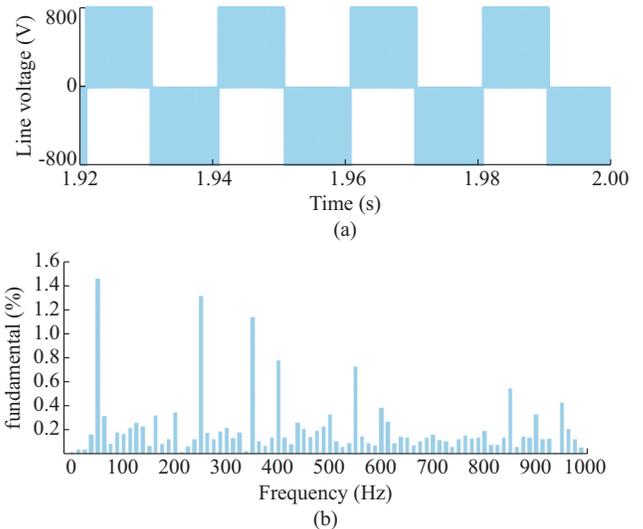


Fig. 16. B6-Balancer structure AC line voltage and its FFT analysis. (a) Two-level output voltage of converter. (b) Output voltage THD of converter (fundamental is 542.5 V and THD is 94.02%).

This leads to the selection of lower rate IGBT modules for this structure and results in the reduction of loss calculation parameters like E_{on} , and E_{off} since these parameters are almost reduced to half of their initial values in lower rate semiconductor.

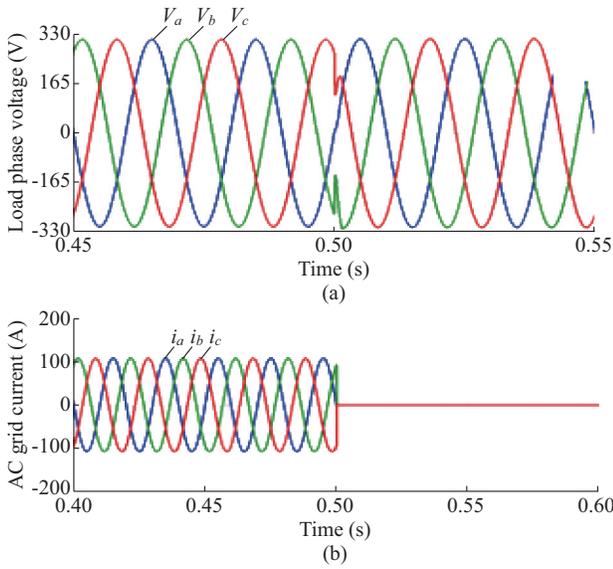


Fig. 17. Bipolar hybrid microgrid operation in a grid-tied and islanded mode using NPC structure as IC. (a) Three-phase to ground voltages of resistive load. (b) Three-phase currents of AC grid.

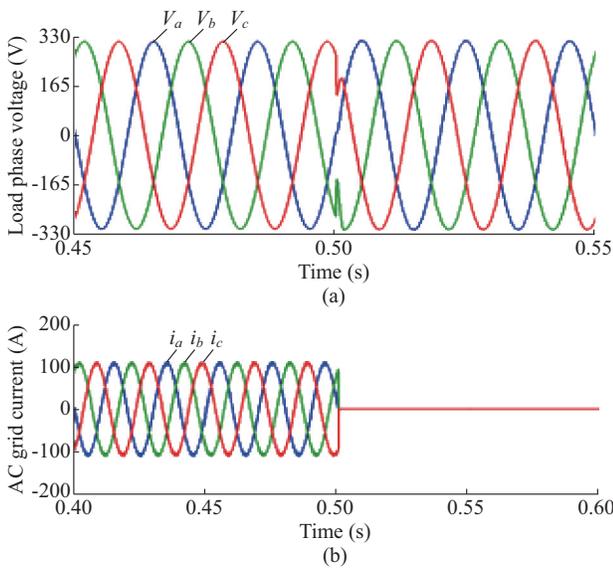


Fig. 18. Bipolar hybrid microgrid operation in the grid-tied and islanded modes using B6-Balancer as IC. (a) Three-phase to ground voltages of resistive load. (b) Three-phase currents of AC grid.

In Fig. 19, the required input parameters of the lookup table are gathered by manufacturer’s datasheets. The designed model in Fig. 19 shows that at first, conduction and switching losses are calculated. Then, the effect of their losses is studied on initial T_j by the thermal network. In the next step, an updated T_j is generated by the thermal network to be used in the calculation of power losses in the next time step.

Based on the above discussion and the described procedure of calculating power loss, power loss simulations have been done for two selected IC candidates in a bipolar hybrid microgrid under the same simulation conditions. The simulation results for selected ICs are demonstrated in Fig. 20 and Fig. 21.

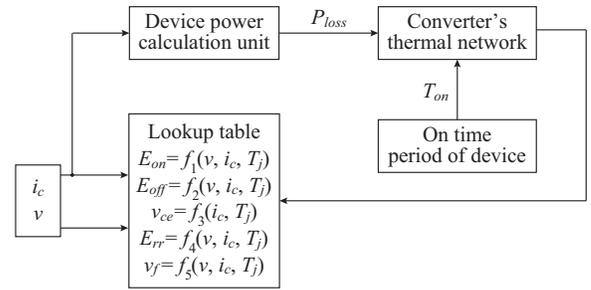


Fig. 19. Closed-loop block diagram of power loss calculation and its thermal simulation model.

Power loss simulations are conducted in rectifier mode in which the grid injects 100 kW power to the DC loads. Figure 20 and Fig. 21 represent loss distribution of NPC and B6-Balancer structure at 5 kHz frequency.

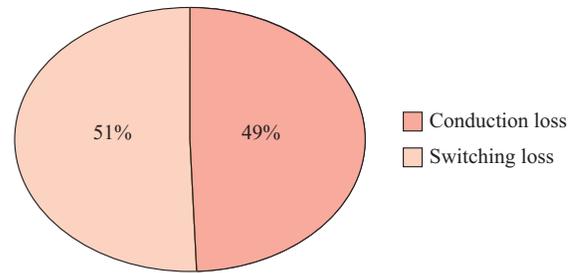


Fig. 20. NPC structure power loss distribution at 5 kHz switching frequency in rectifier mode.

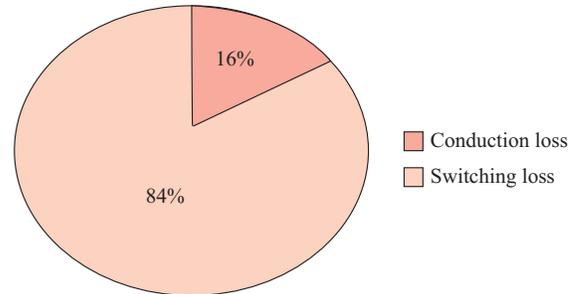


Fig. 21. B6-Balancer structure power loss distribution at 5 kHz switching frequency in rectifier mode.

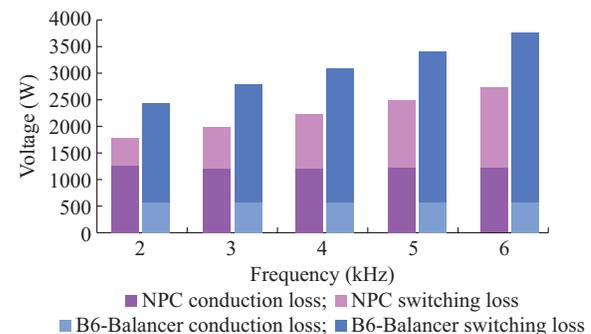


Fig. 22. Power loss simulation results of NPC and B6-Balancer structures in detail for several switching frequencies.

The total power loss of IC is reduced by 27% when the single-stage IC is used. That means two-stage IC has a low-

er efficiency in comparison to the single-stage structure. In NPC structure, the conduction and switching losses at the investigated frequency are split equally.

However, in B6-Balancer structure, the switching loss has the most proportion of the power loss and is almost five times greater than the conduction loss. The reason is that in every moment, one of the two switches in balancer converters turns on, and the other one turns off which causes the power loss of switching energy increasing to the top.

Power loss simulation in various switching frequencies is demonstrated in Fig. 22, revealing that conduction losses are almost kept the same for both structures. However, this is different for switching losses. As the switching frequency decreases, switching loss of both structures drops but the reduction of B6-Balancer switching loss is higher than NPC structure. Therefore, in low switching frequencies (2 kHz), the total semiconductor power loss of B6-Balancer has the lowest difference with NPC converter. Although reducing the switching frequency may be the solution for high power loss in B6-Balancer structure, it will raise another significant value, which is THD of AC current.

Decreasing the switching frequency may solve the switching power loss problem, but it will increase THD of AC current and therefore decrease the power quality. It means an additional active or passive filter is needed for the B6-Balancer structure in low switching frequencies. Figures 20 to 22 show that the NPC structure is superior to B6-Balancer in the simulated power scale, regarding their power loss.

V. CONCLUSION

In this paper, a two-stage IC structure suitable for a new topology bipolar hybrid microgrid has been investigated and a new single-stage IC is proposed. Two candidates of both single-stage and two-stage structures are selected to be compared and tested in this newly presented microgrid. The B6-Balancer control strategy is updated to a simpler cost-effective model to balance DC-link pole voltages. A new control strategy for NPC converter to balance DC-link pole voltages is designed in which zero component of current is controlled without grounding the DC side of the converter. In the designed controlled strategy of NPC converter, the controlling of zero component of the current overcomes the limitation in DC load unbalance, which has been demonstrated in simulation results by increasing DC load of one pole up to 100%. Results show that B6-Balancer structure has a better outcome in balancing DC-link voltage, while NPC structure shows a better AC power quality in both grid-tied and islanded modes. Semiconductor power loss simulation with a flexible junction temperature of semiconductors based on the thermal network simulation is conducted. It shows that the power loss in B6-Balancer structure is higher than NPC structure, and the loss of B6-Balancer raises rapidly by increasing switching frequency.

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Parviz Najafi received the B.S. degree in electrical engineering from Amir Kabir University of Technology, Tehran, Iran, in 2011 and M.S. degree in power electronics from Tarbiat Modares University Tehran, Iran, in 2013. He is currently a Ph.D. candidate in power electronics at K. N. Toosi University of Technology, Tehran, Iran. For the last 5 years, he was working as a substation automation expert. His current research interests include topologies of interlinking converters in AC and DC microgrids, renewable energy resources, and protection system of microgrids.

Abbas Houshmand Viki is an associate professor at K. N. Toosi University of Technology, Tehran, Iran. His current research interests include power electronics converters, AC/DC microgrids, renewable energy systems and flexible AC transmission systems.

Mahdi Shahparasti received the Ph.D. degree in electrical engineering specializing in power electronics from Tarbiat Modares University, Tehran, Iran. He was a Research and Development Researcher with JDEVS Co. designing medium and high power converters. During 2015 and 2017-2019, he was a Postdoctoral Researcher with the UPC Barcelona, Spain, where he was involved in the control of high power grid-connected converters. He is currently a postdoc at the University of Southern Denmark, Denmark. His current research interests include control standalone and grid-connected inverters, renewable energy resources, and motor drive systems.

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